



Radxa XpressReal

schematic

V1.2

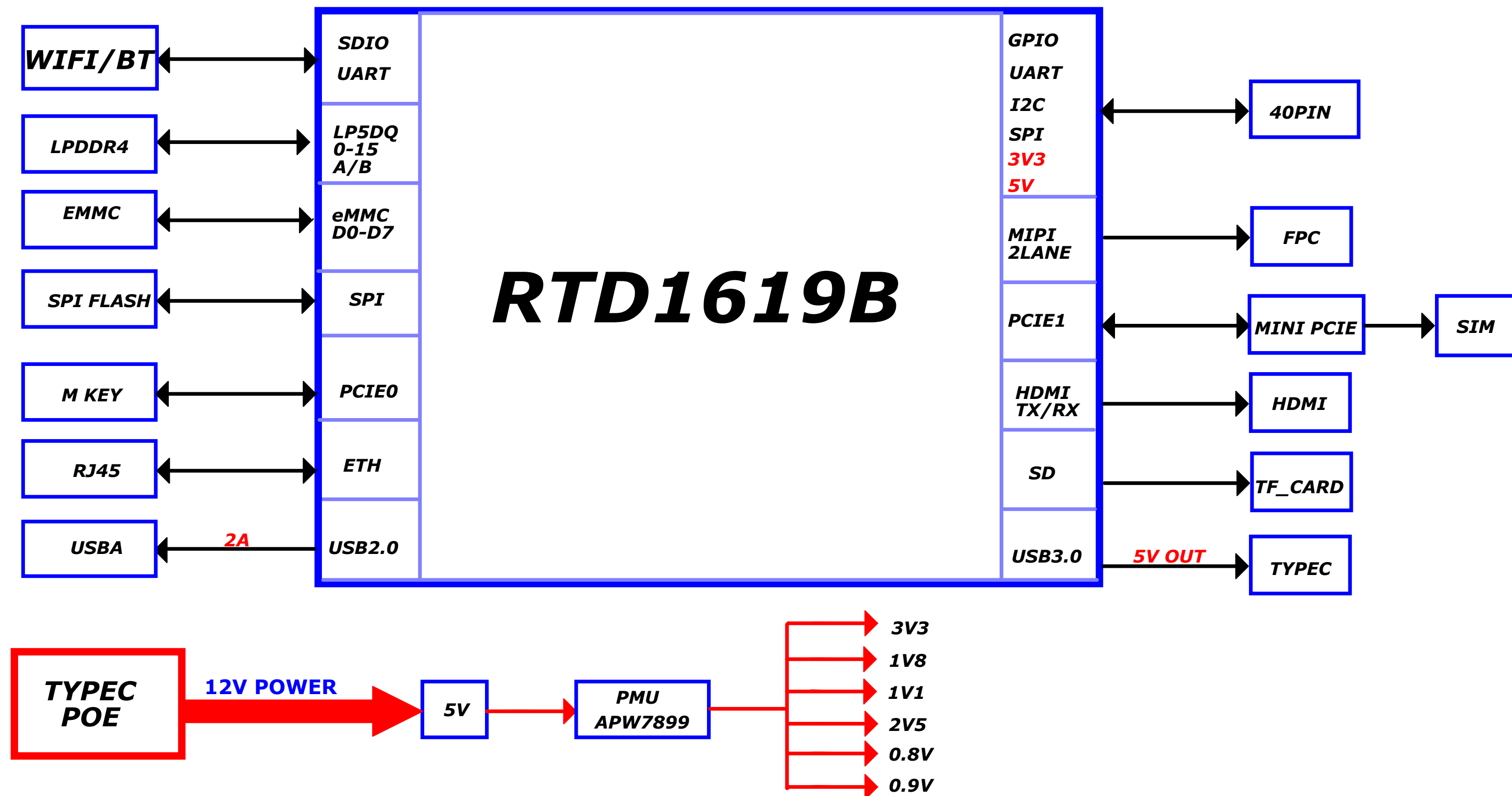


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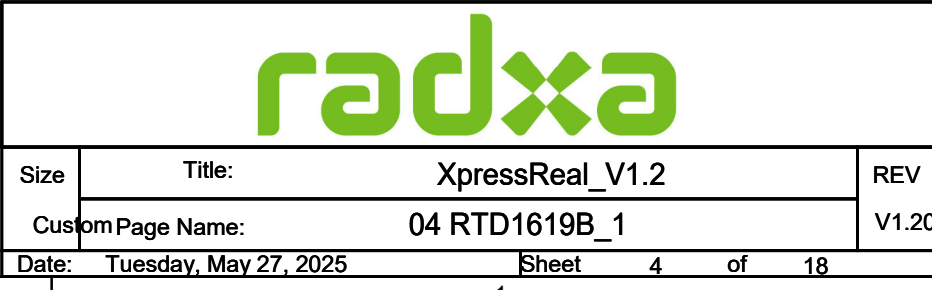
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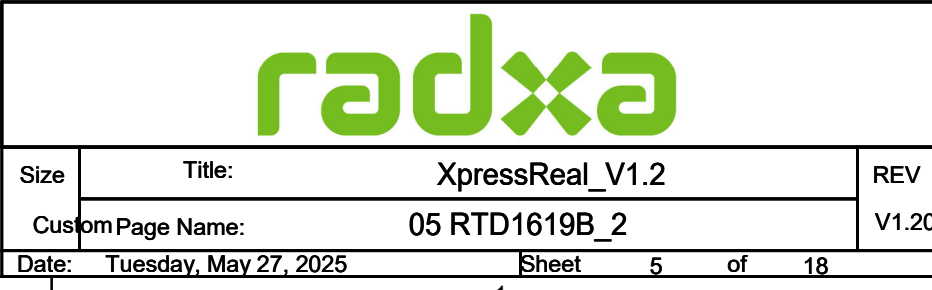


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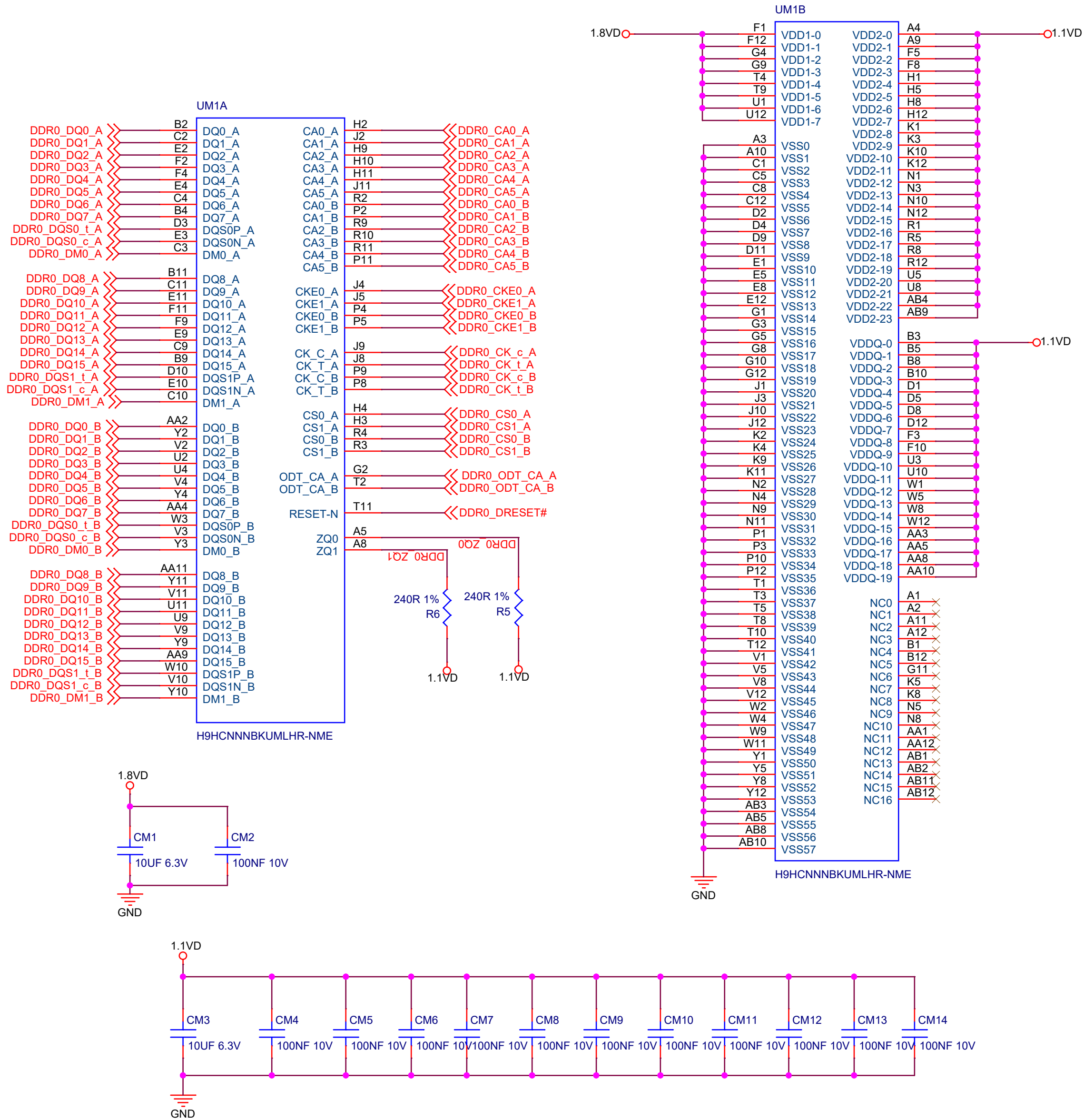


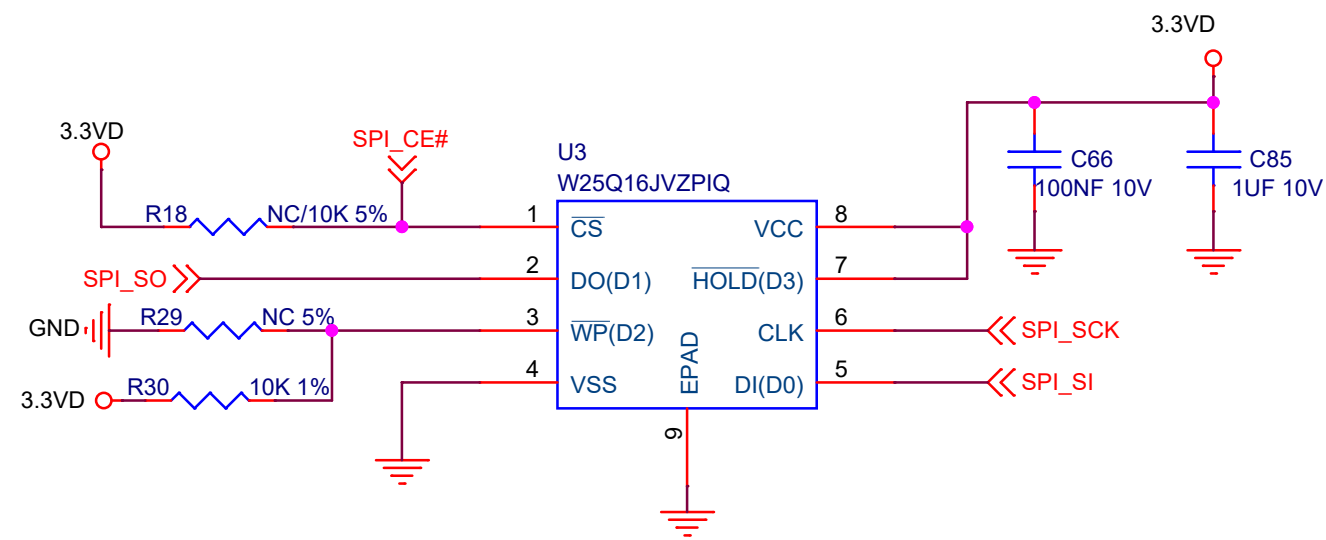
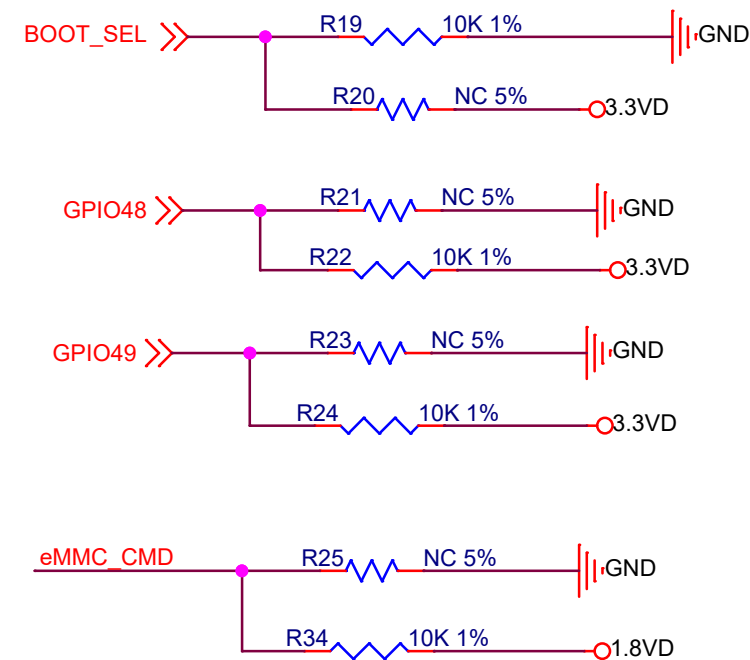
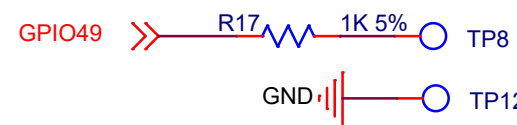
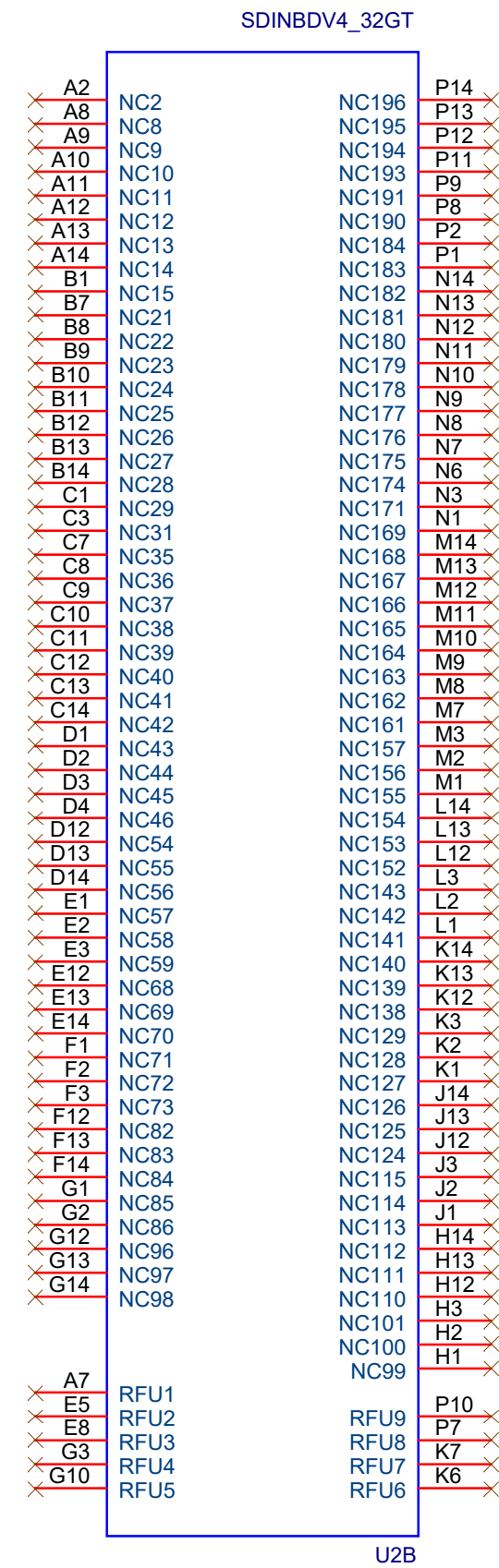
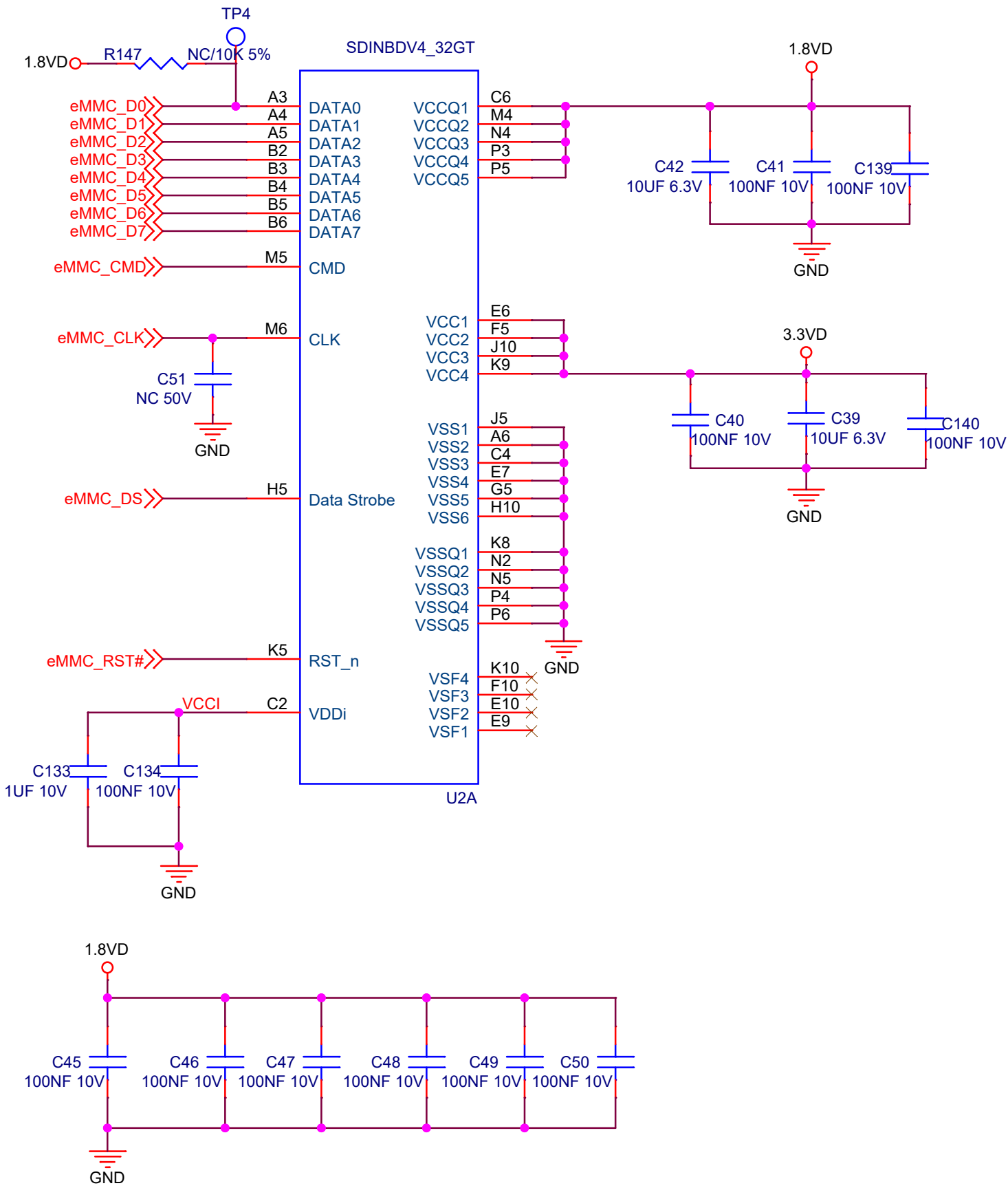
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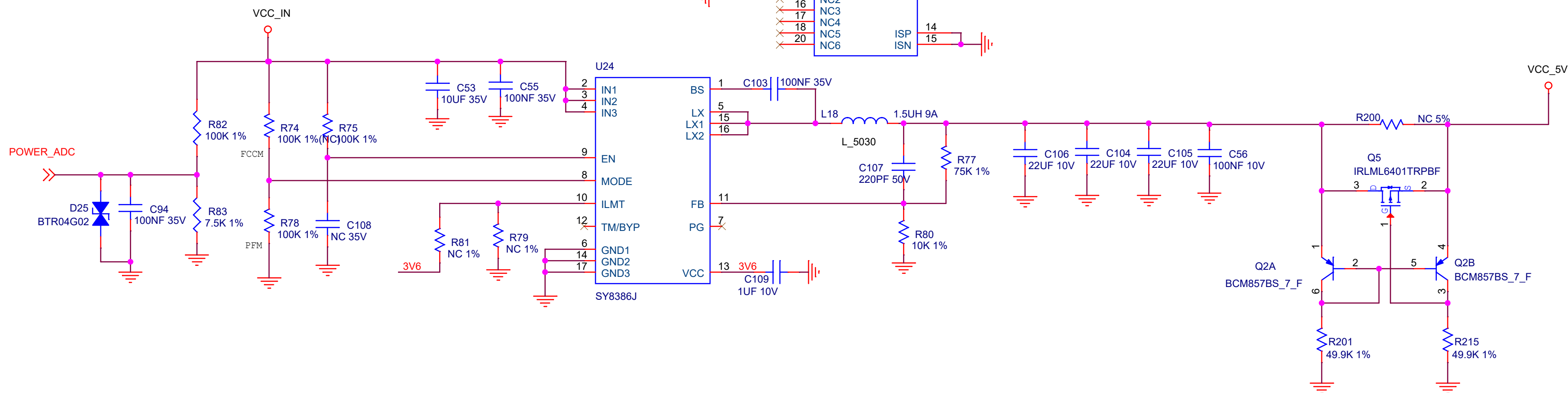
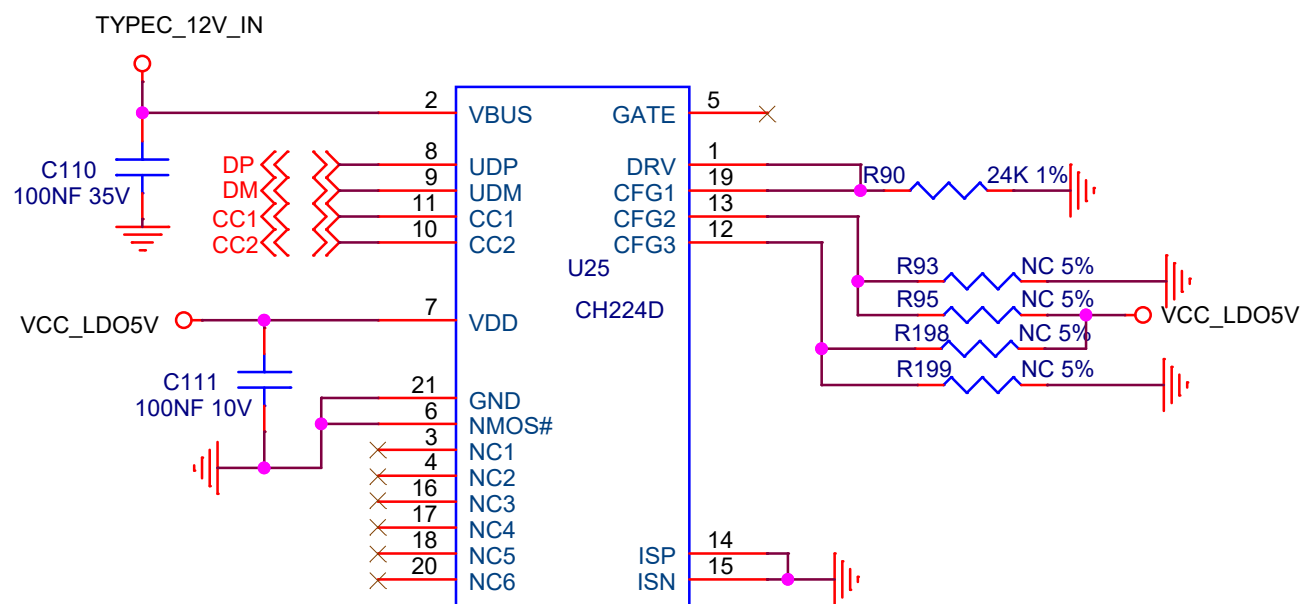
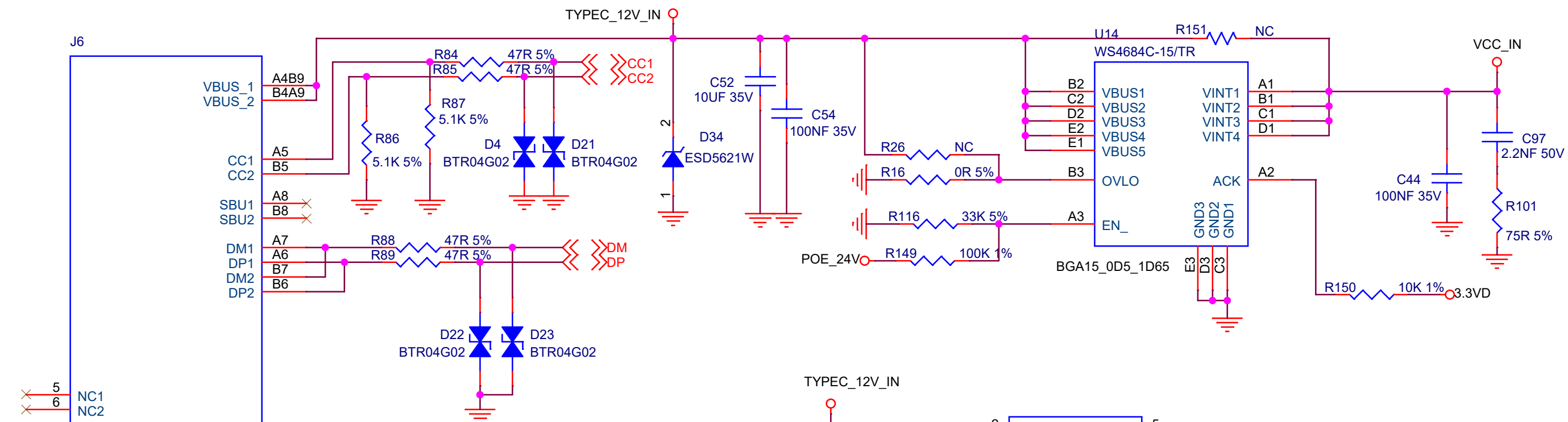


LPDDR4



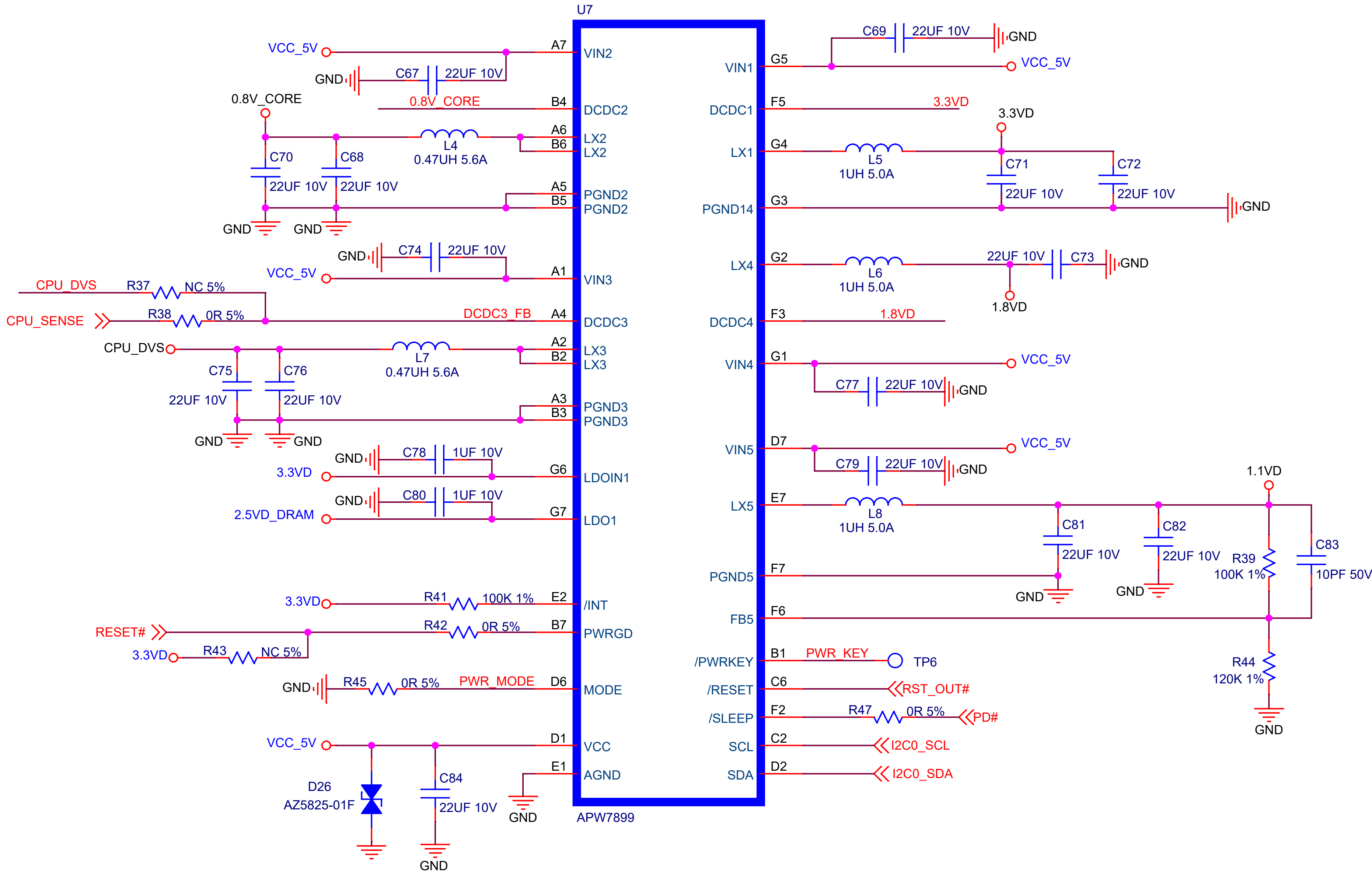


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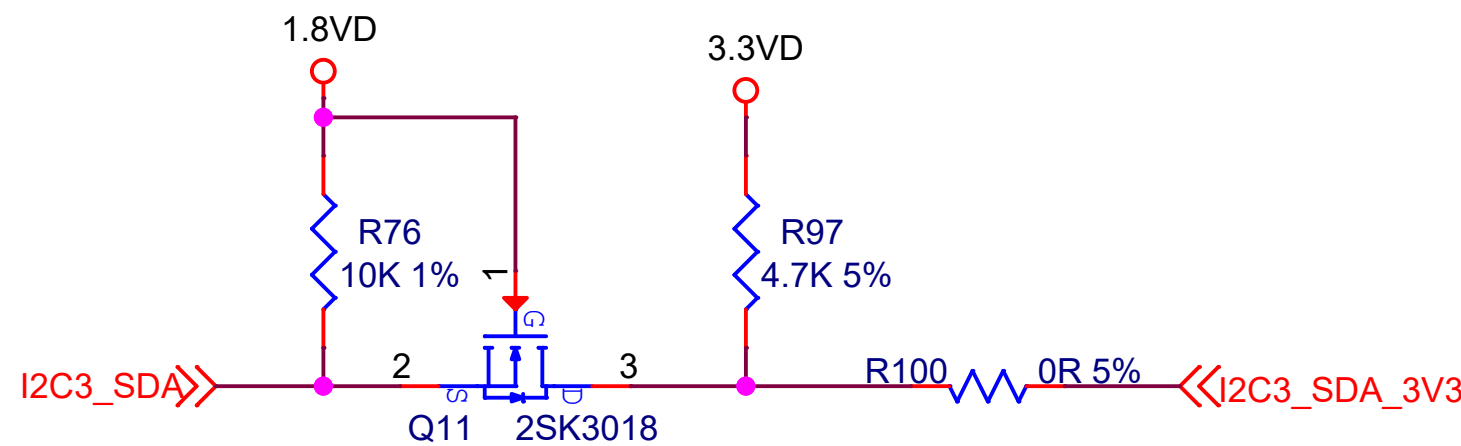
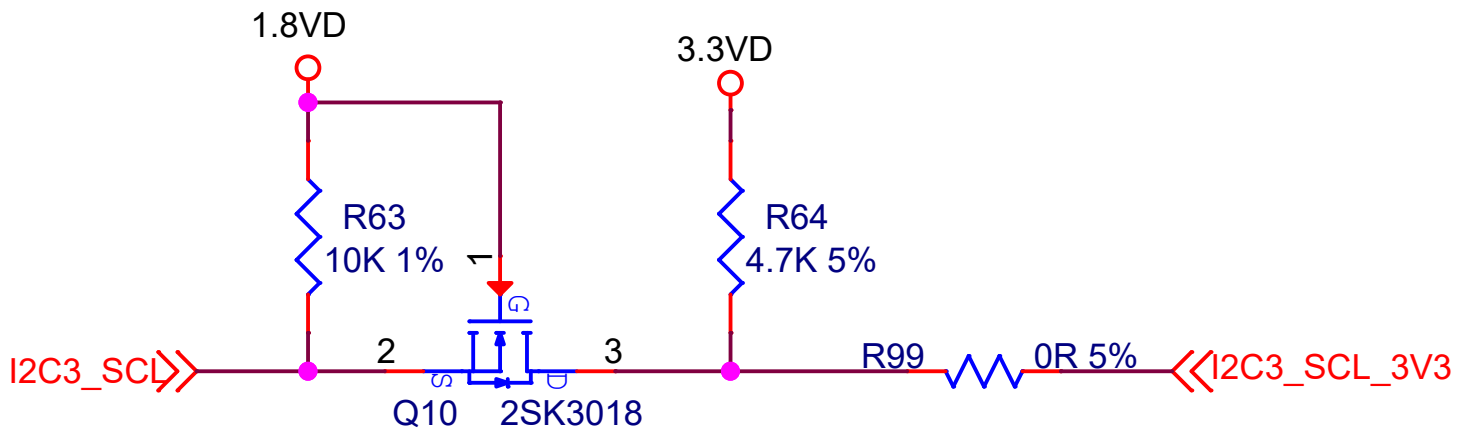
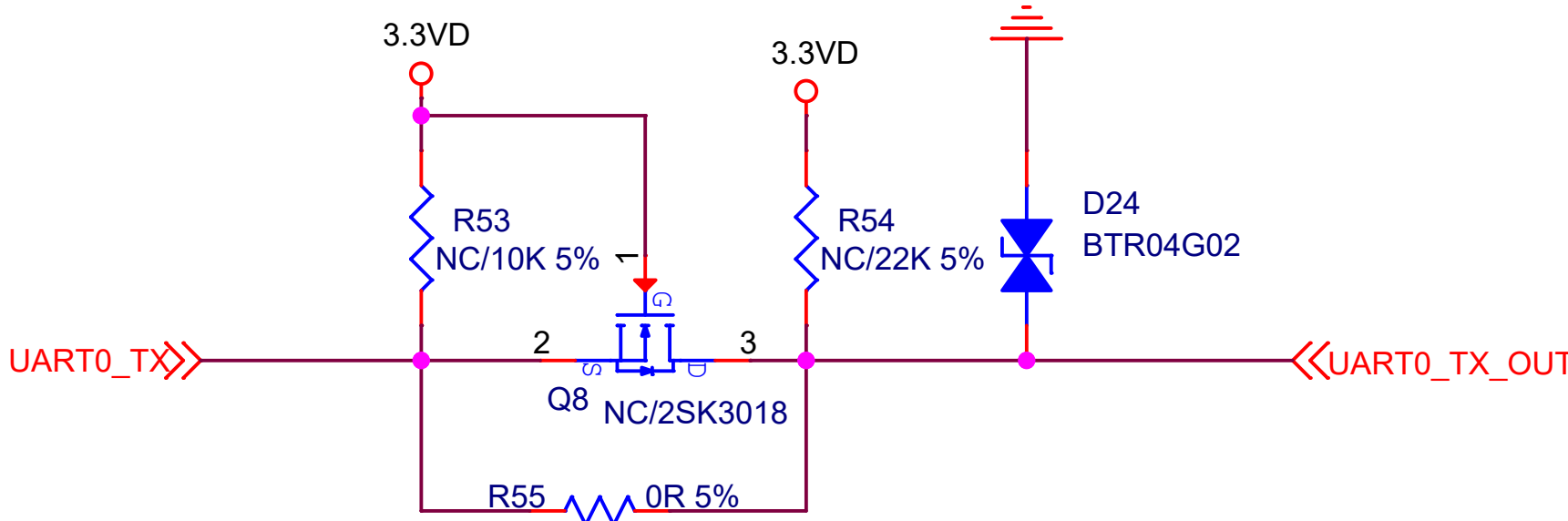
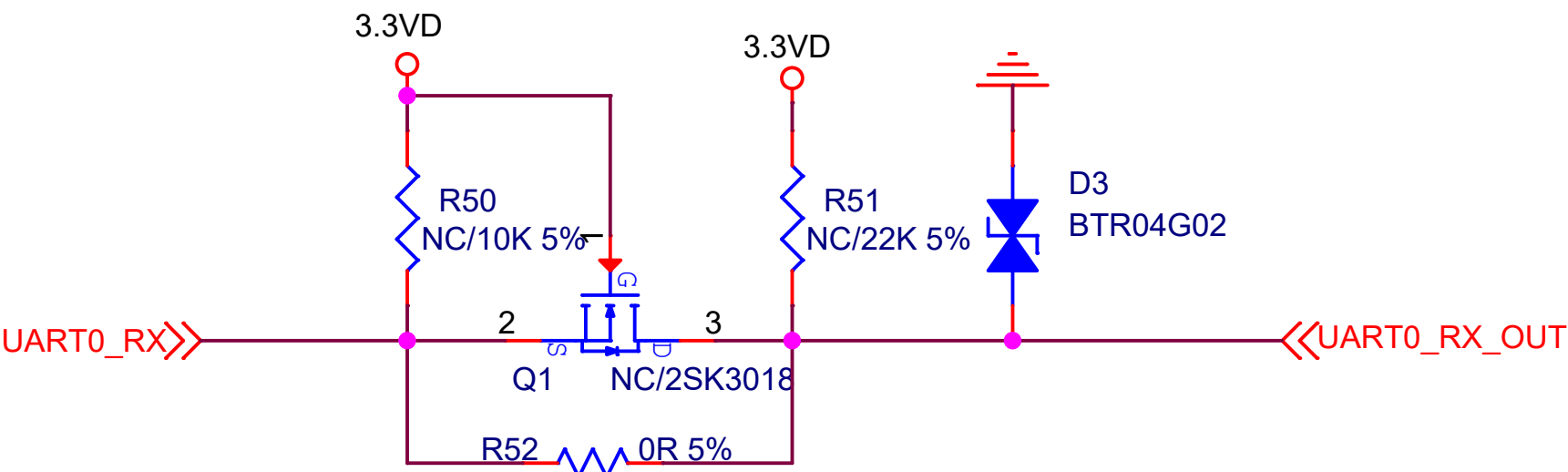
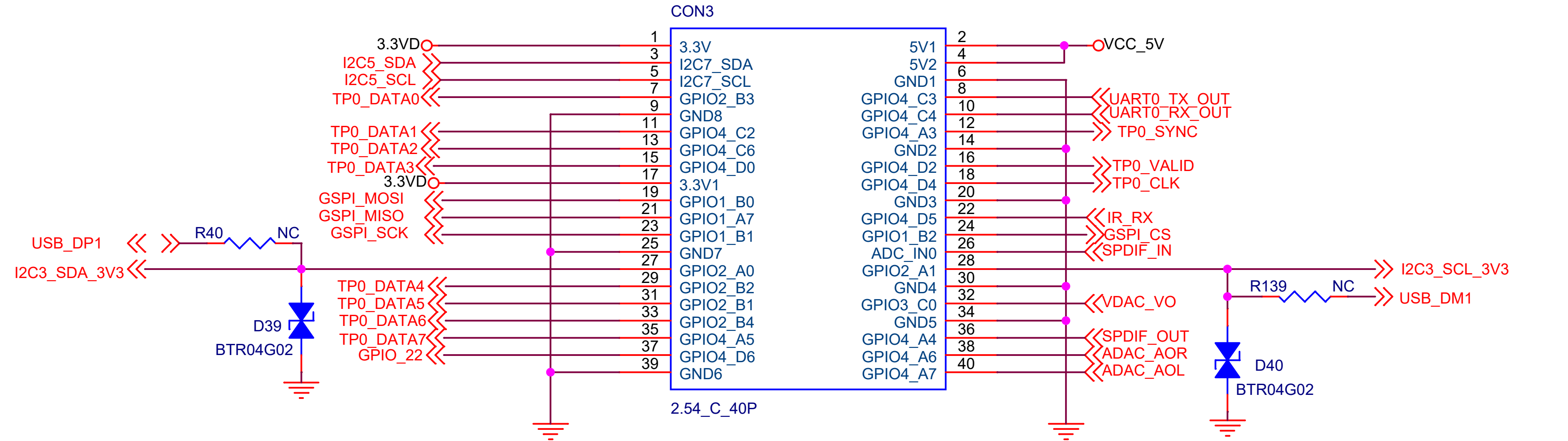
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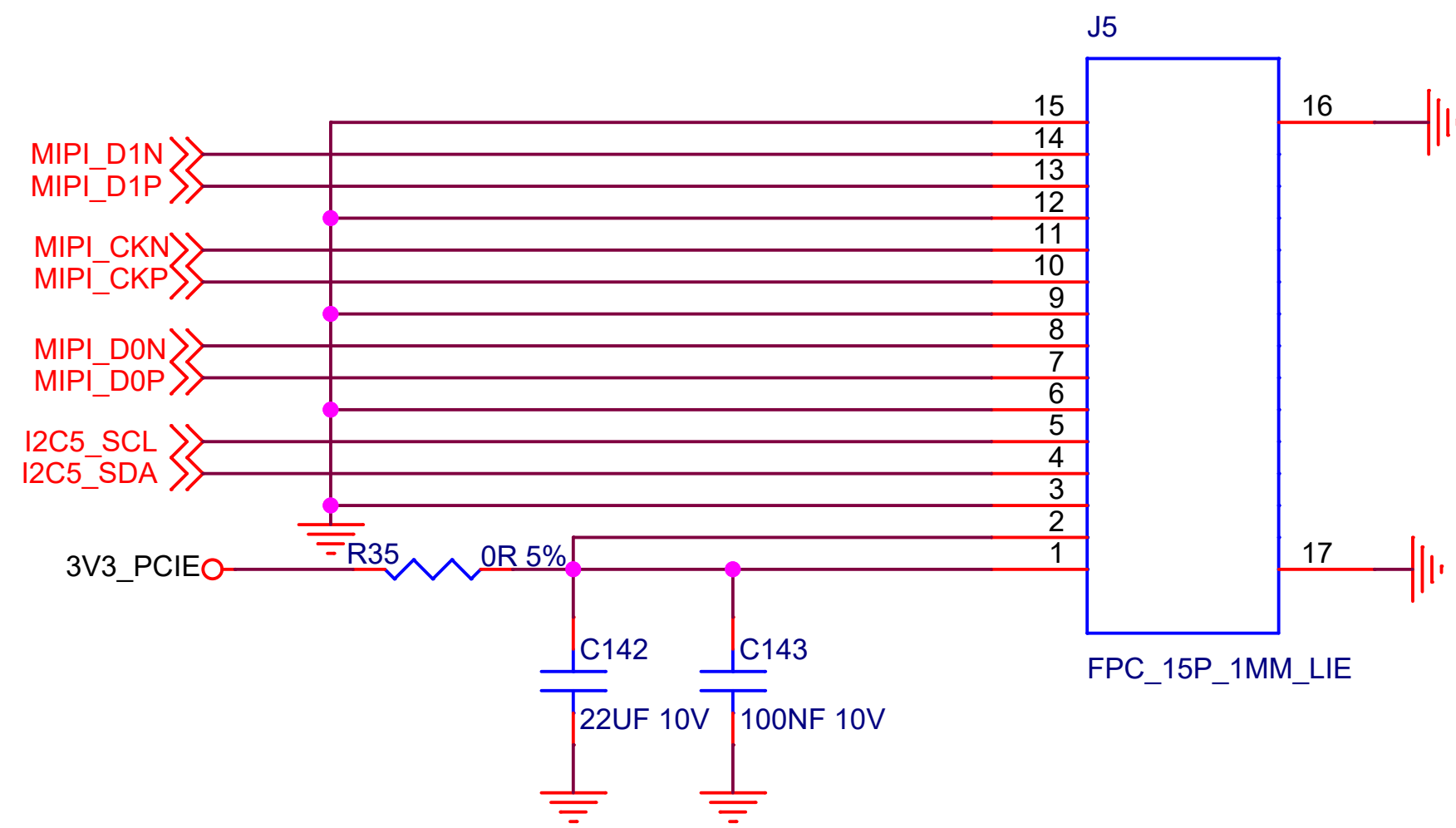


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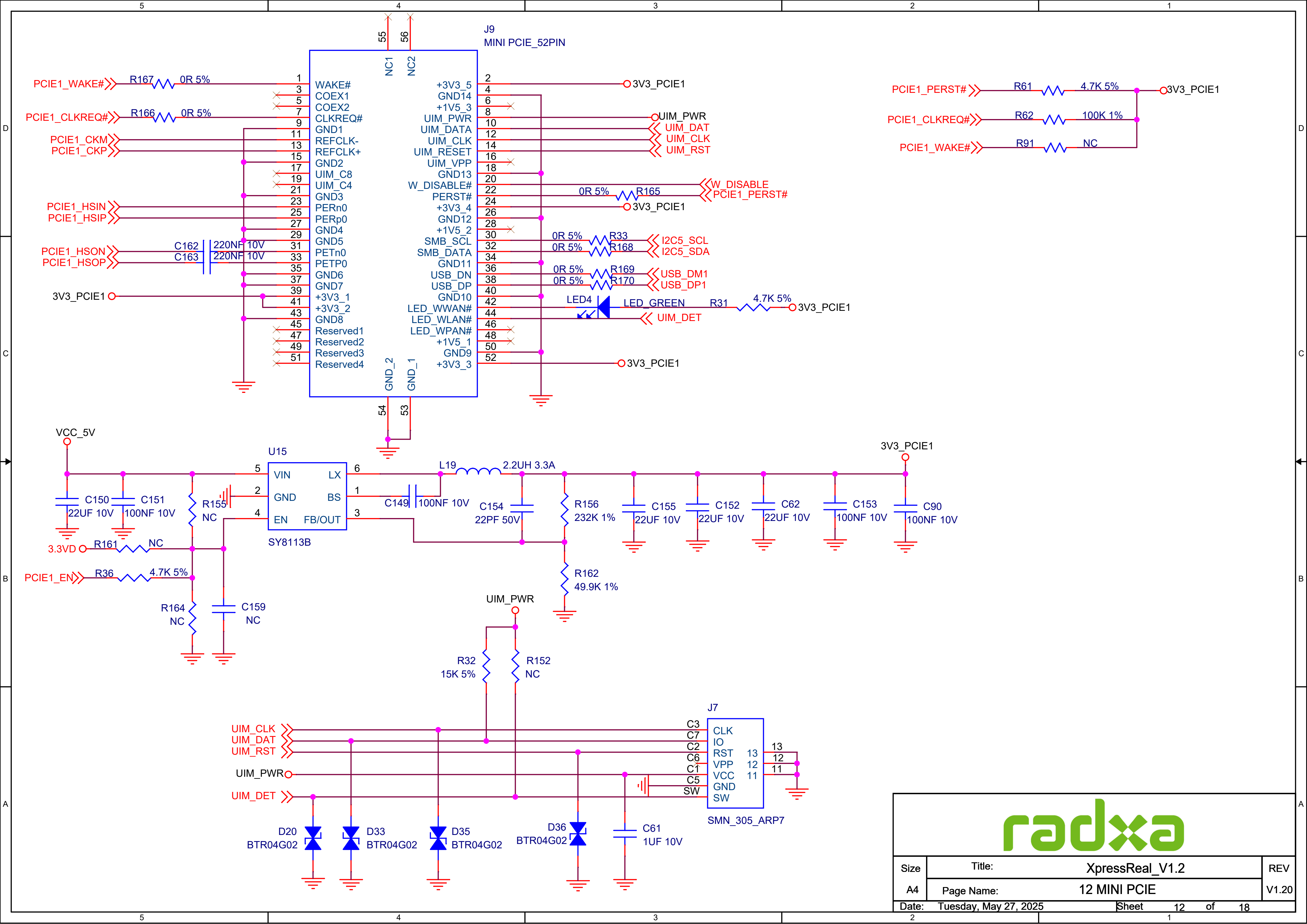
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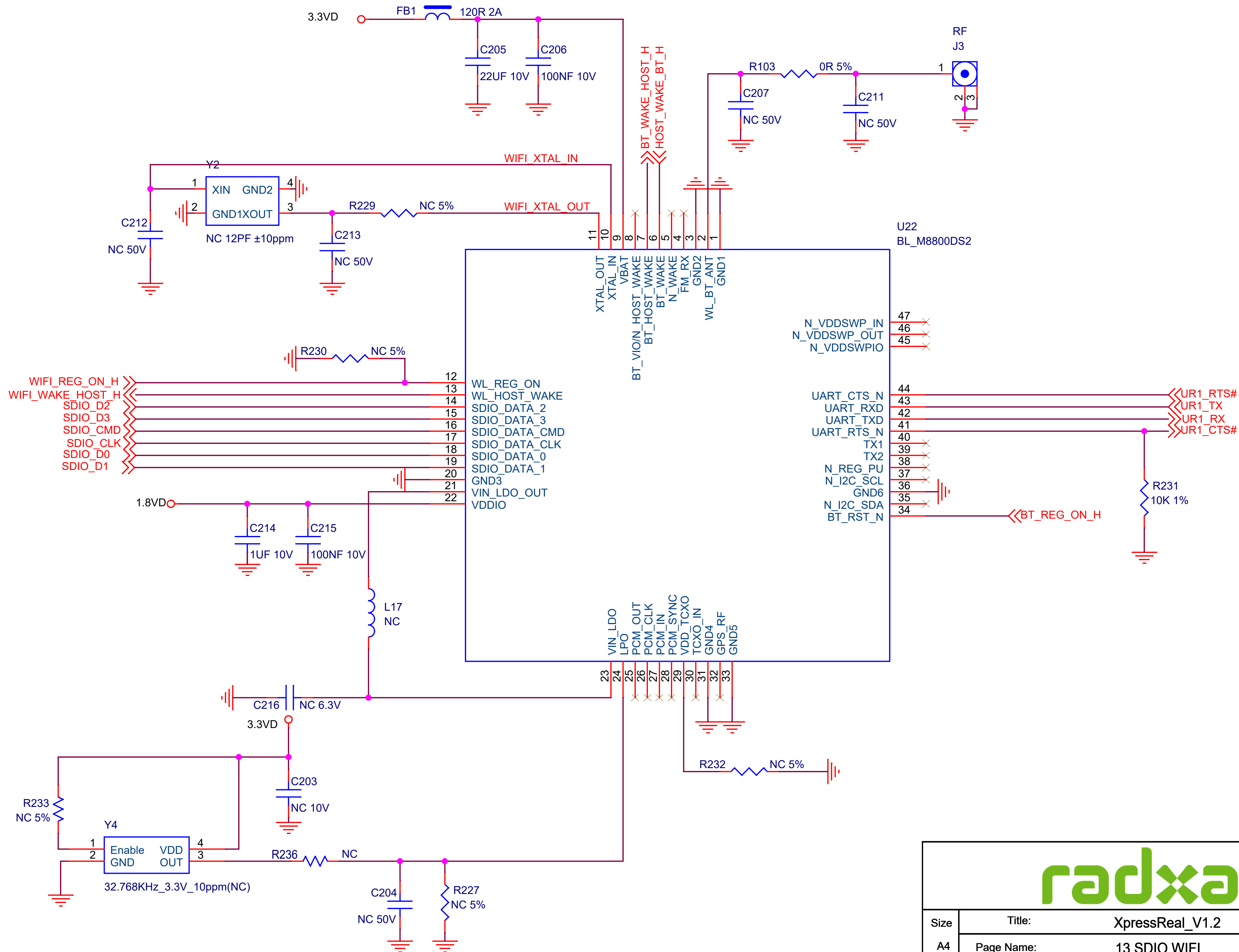
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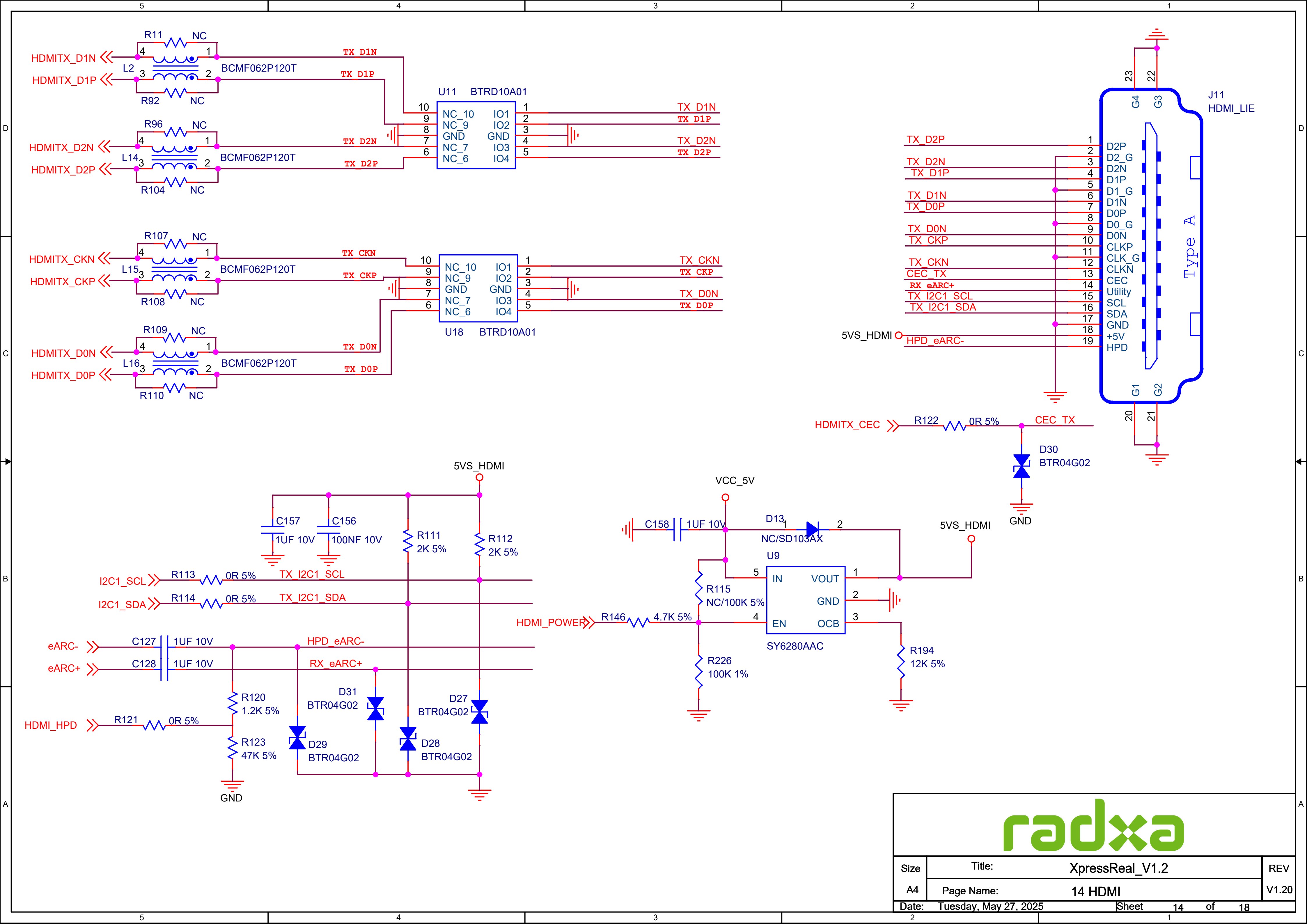
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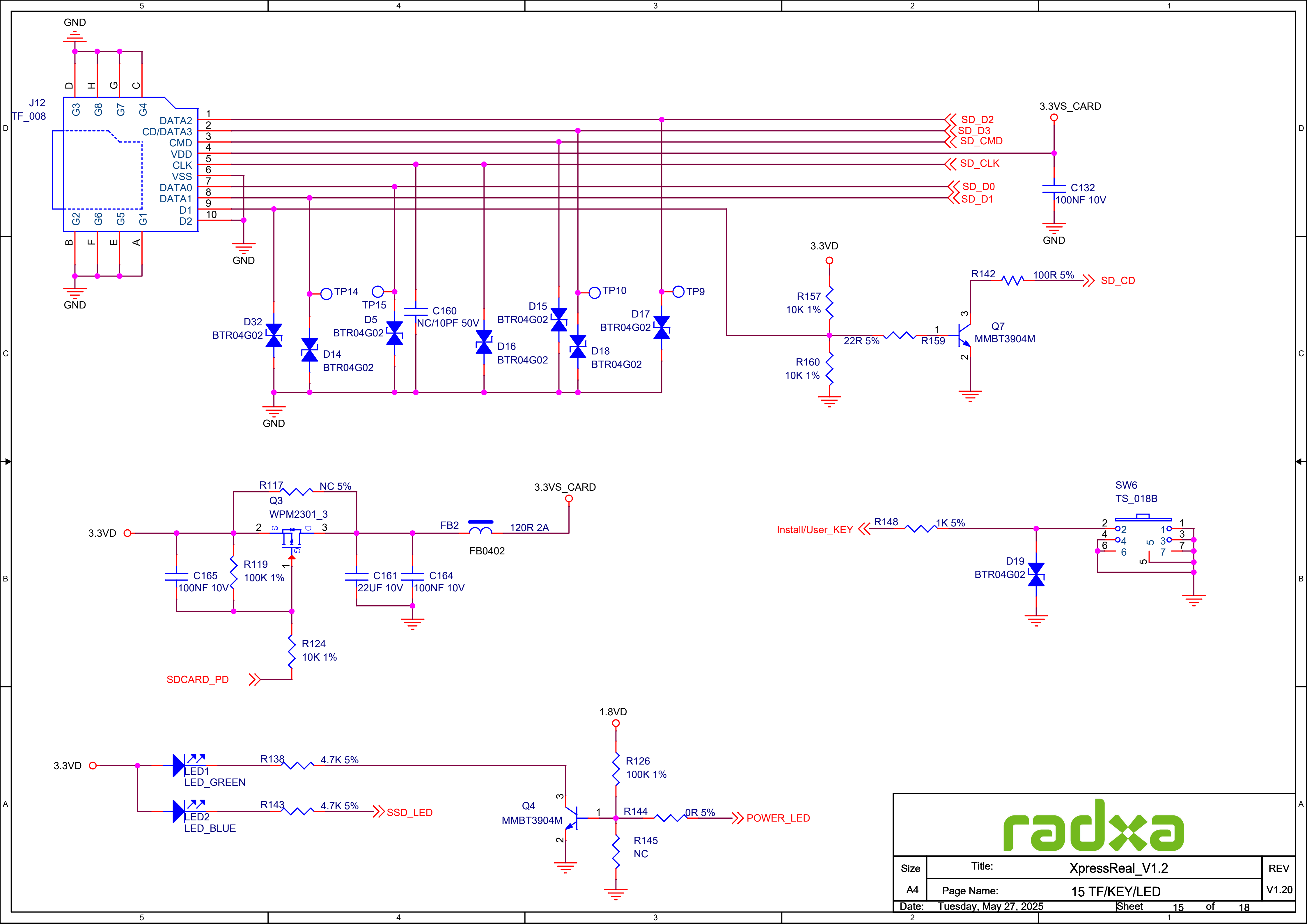
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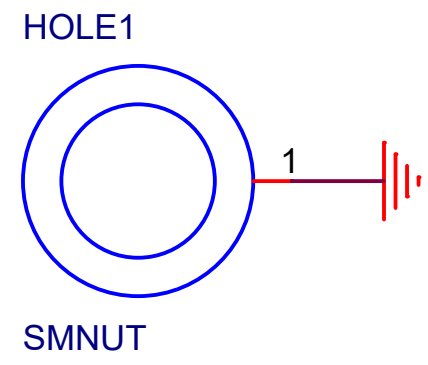
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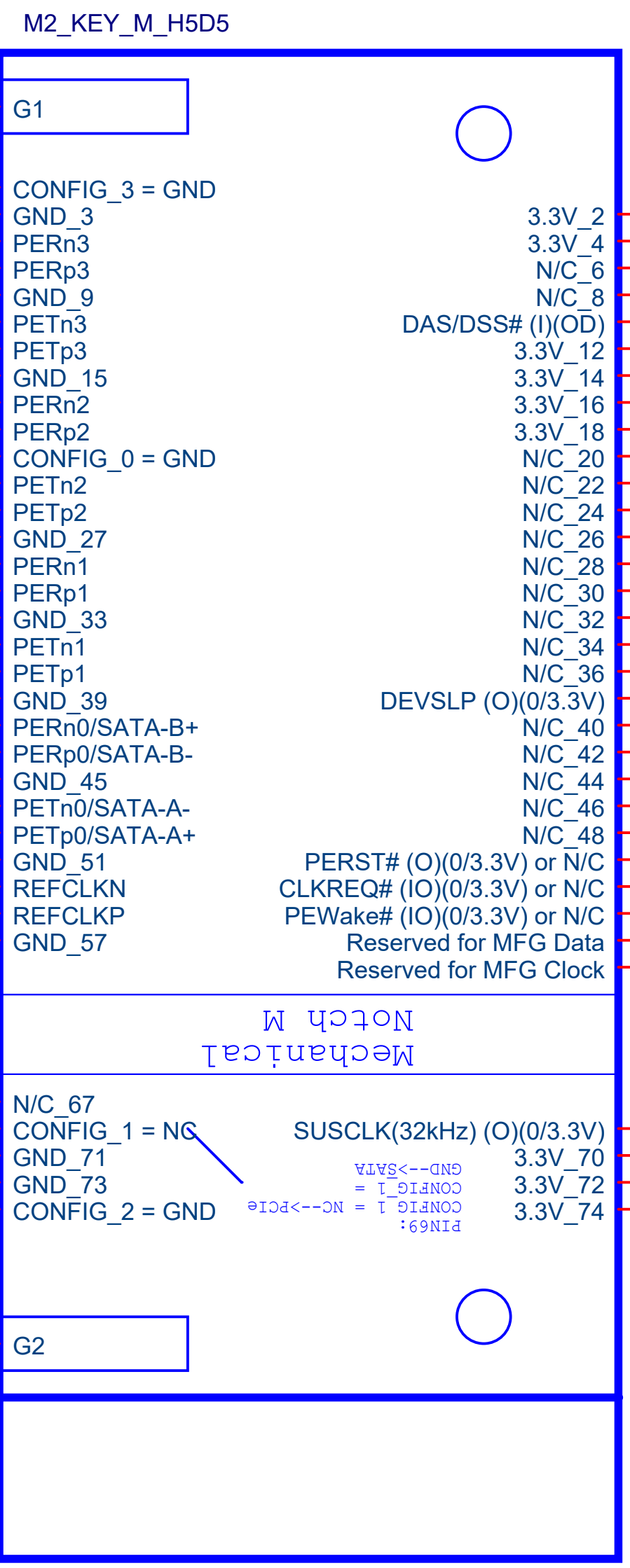


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PCIE0_HSIN
PCIE0_HSIP
PCIE0_HSON
PCIE0_HSOP
PCIE0_CKM
PCIE0_CKP

C86 100NF 10V
C87 100NF 10V



DAS/DSS# (I)(OD)

DEVSLP (O)(0/3.3V)
PERST# (O)(0/3.3V) or N/C
CLKREQ# (IO)(0/3.3V) or N/C
PEWake# (IO)(0/3.3V) or N/C
Reserved for MFG Data
Reserved for MFG Clock

Mechanical Notch

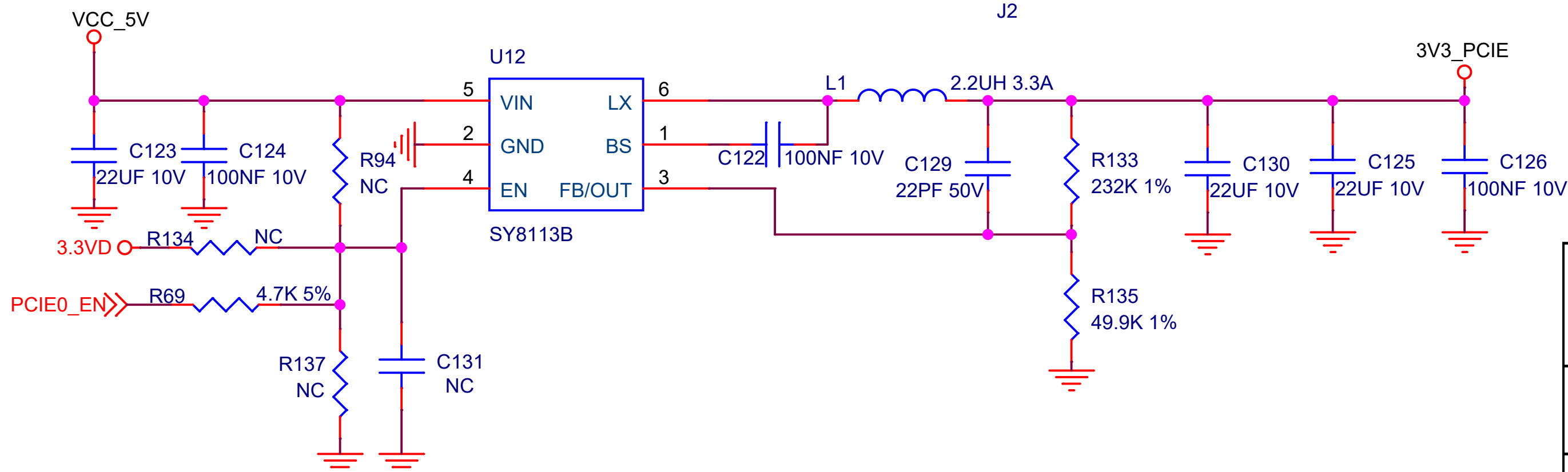
SUSCLK(32kHz) (O)(0/3.3V)
CONFIG_1 = NC
CONFIG_2 = GND

3.3V_2
3.3V_4
N/C_6
N/C_8
3.3V_12
3.3V_14
3.3V_16
3.3V_18
N/C_20
N/C_22
N/C_24
N/C_26
N/C_28
N/C_30
N/C_32
N/C_34
N/C_36
N/C_40
N/C_42
N/C_44
N/C_46
N/C_48

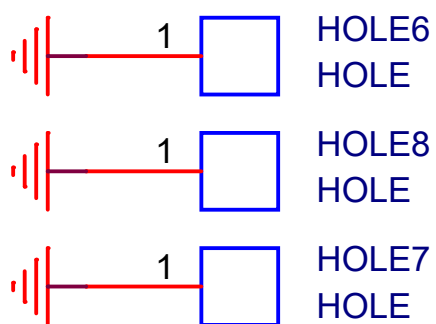
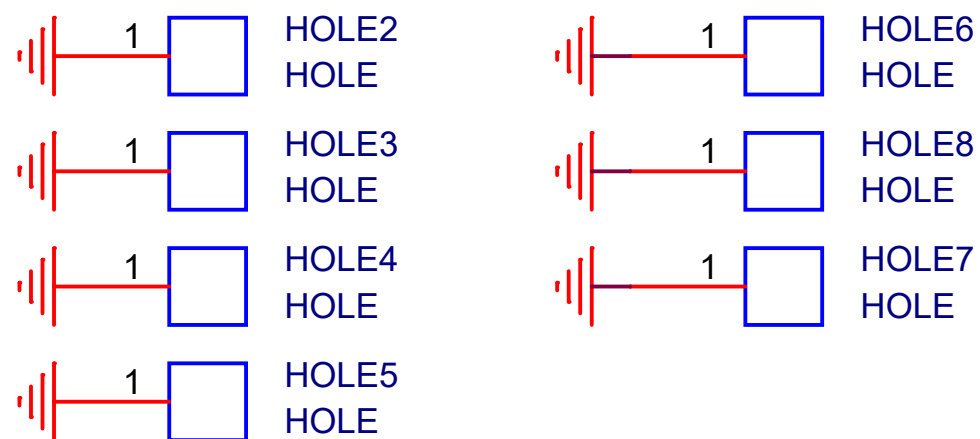
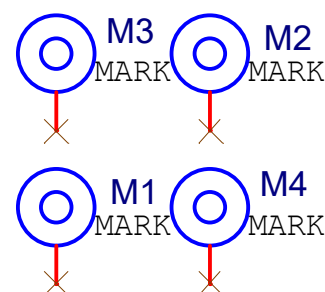
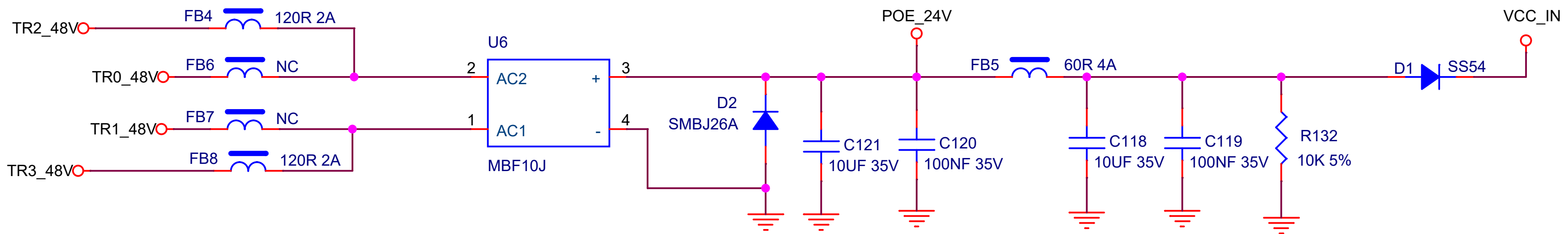
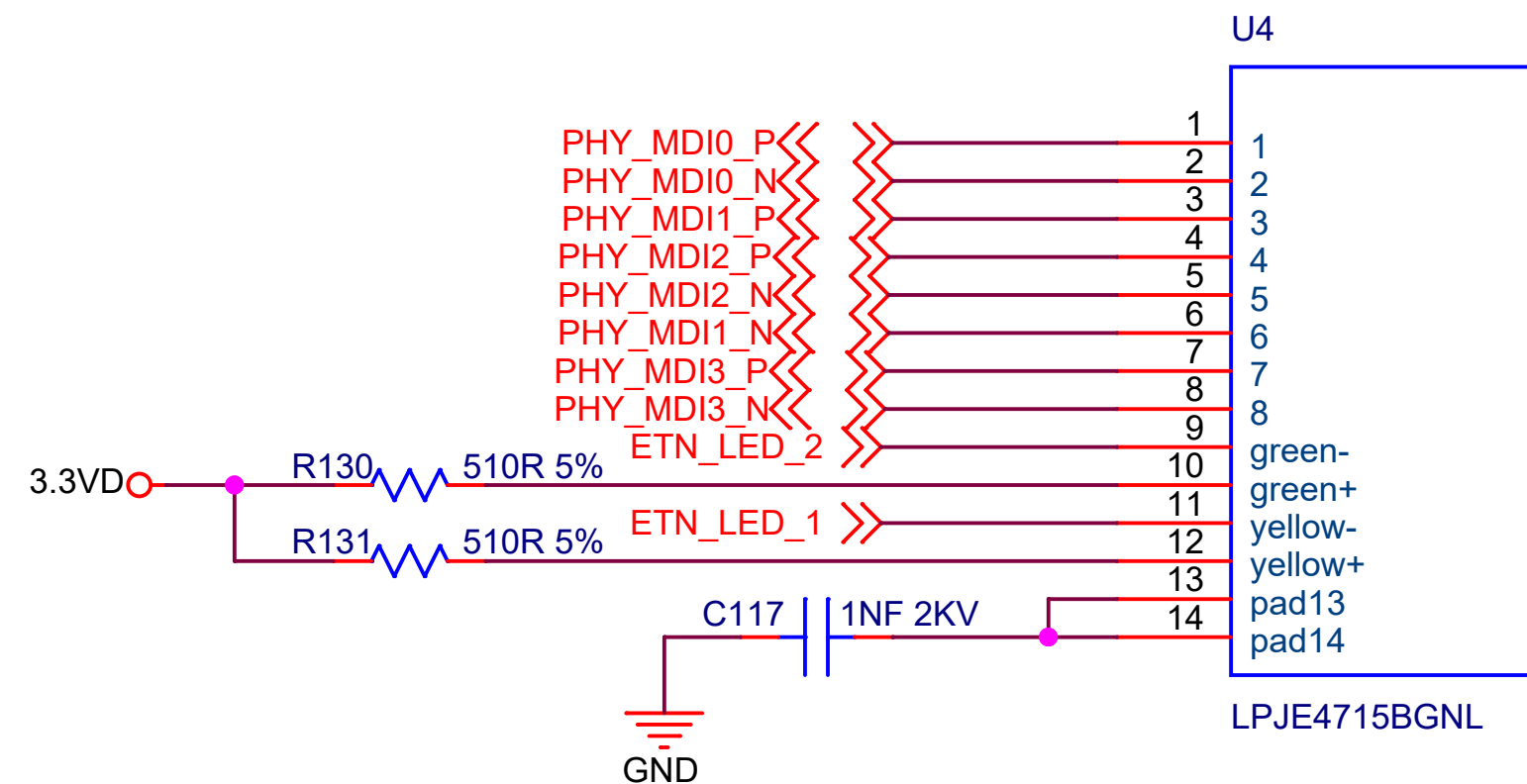
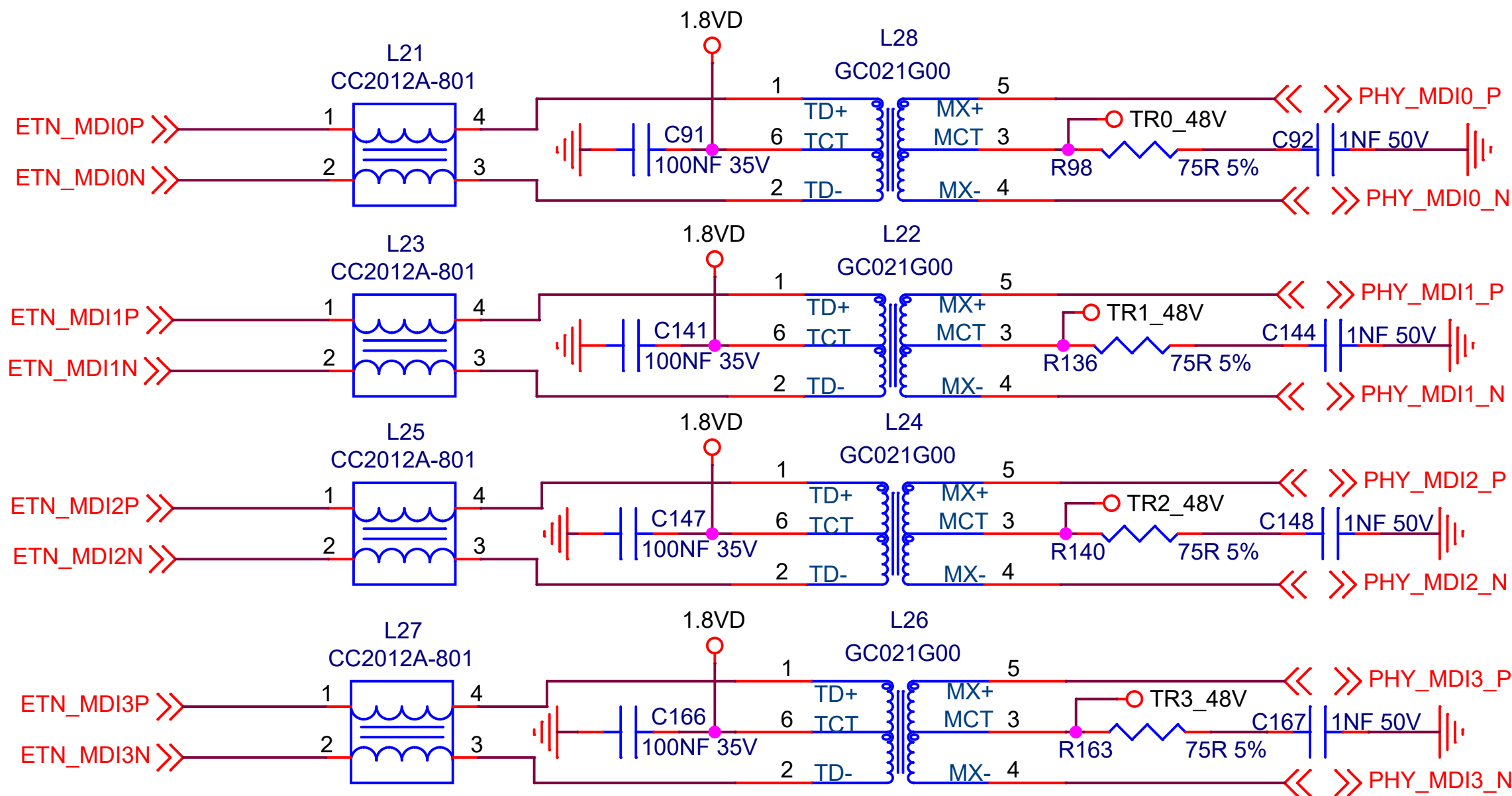
3V3_PCIE

PCIE0_RST#
PCIE0_CLKREQ#
PCIE0_WAKE

3V3_PCIE



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