

Tablet Schematics For RK3566

RK_TABLET_RK3566_LP4D200P132SD6_V1.0

Main Functions Introduction

- 1) PMIC: RK817-5+Charger+DiscretePower
- 2) RAM: LPDDR4 1x32Bit(Default:2GB)
- 3) ROM: eMMC5.1(Default:16GB),Option Nand Flash
- 4) Support: Micro SD Card3.0
- 5) Support: 1 x USB2.0 OTG
- 6) Support: 4Lanes MIPI CSI Camera(Max 8M) or 2Lane+2Lane MIPI CSI Camera
- 7) Support: HDMI2.0 TX
- 8) Support: 4Lanes MIPI DS Touch Connector
- 9) Support: a/b/g/n/ac 2X2 WIFI
- 10) Support: Headphone output and Speaker out(1.3W@8ohm)
- 11) Support: Gyroscope-sensor G-sensor M-sensor PS-sensor
- 12) Support: Array Key(VOL+,VOL-)



www.t-firefly.com

Title: Cover Page

File: ROC-3566-PC

REV: V0.1

Create Date: Monday, March 30, 2020

Page Num: 1

Modify Date: Tuesday, June 01, 2021

Page Total: 37

Rockchip Confidential

A

Rockchip Confidential

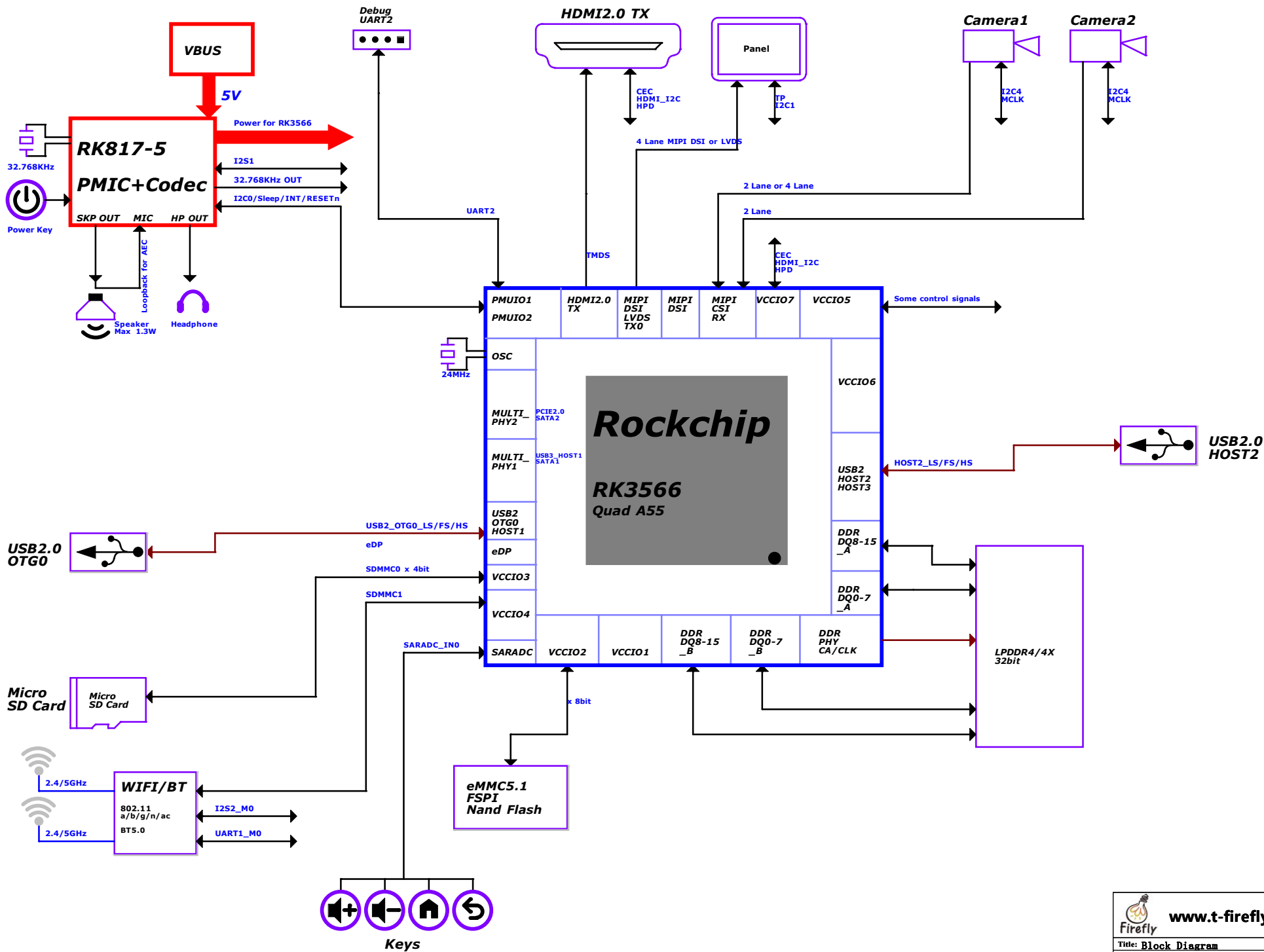


Firefly

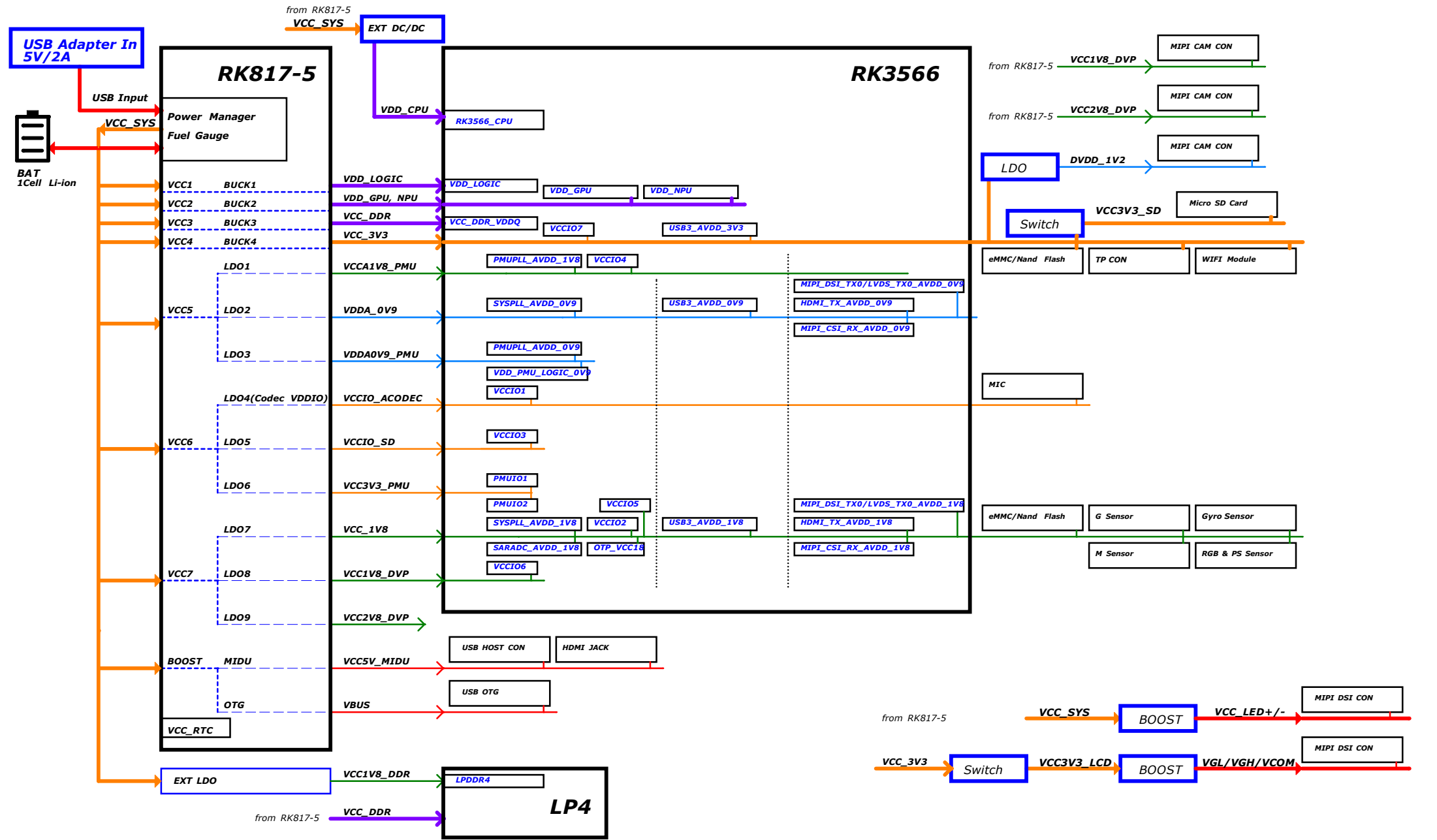
www.t-firefly.com

Title: Revision History	
File: ROC-3566-PC	REV: V0.1
Create Date: Monday, March 30, 2020	Page Num: 3
Modify Date: Tuesday, June 01, 2021	Page Total: 37

RK3566 Ref Block Diagram

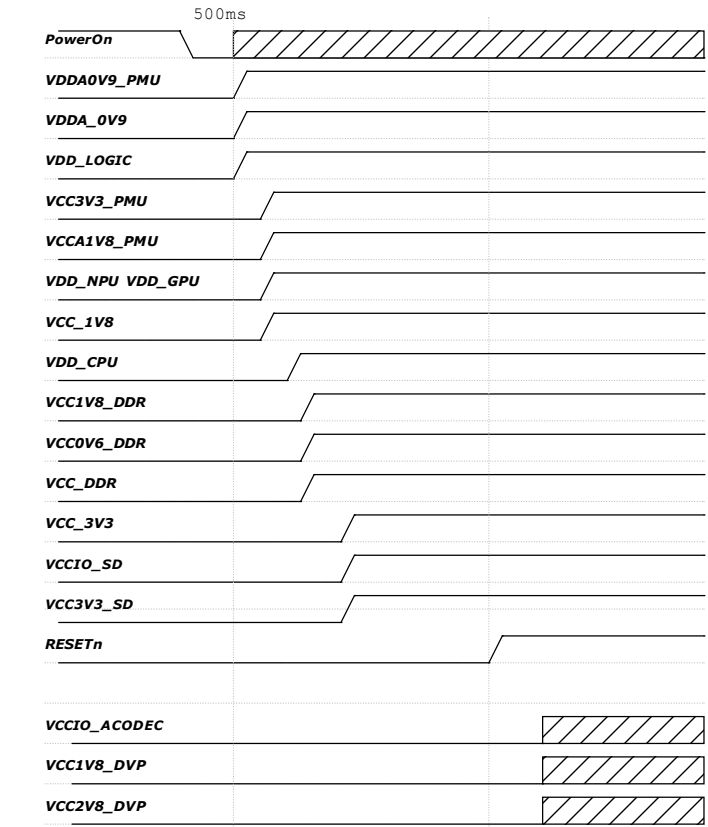


Power Diagram



Power Sequence

&Power Path assignment



Power Source	PMIC Channel	Supply Limit	Power Supply Name	Time Slot	Default Voltage	Work Status	Sleep Status
VCC_SYS	RK817-5_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_BUCK2	2.5A	VDD_NPU,VDD_GPU	Slot:2	0.9V	ON	OFF
VCC_SYS	RK817-5_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON
VCC_SYS	RK817-5_BUCK4	1.5A	VCC_3V3	Slot:4	3.3V	ON	OFF
VCC_SYS	RK817-5_LDO1	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON
	RK817-5_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF
	RK817-5_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_LDO4	0.4A	VCCIO_ACODEC	N/A	1.8V	ON	OFF
	RK817-5_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF
	RK817-5_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON
VCC_SYS	RK817-5_LDO7	0.4A	VCC_1V8	Slot:2	1.8V	ON	OFF
	RK817-5_LDO8	0.4A	VCC1V8_DVP	N/A	1.8V	ON	OFF
	RK817-5_LDO9	0.4A	VCC2V8_DVP	N/A	2.8V	ON	OFF
VCC_BAT	RK817-5_RESETn			Slot:4+5			
VCC_BAT	RK817-5_BOOST RK817-5_OTG	1.5A	VCC5V_MIDU VBUS	N/A	5.0V	ON	OFF
VCC_3V3	Switch		VCC3V3_SD	Slot:4	3.3V	ON	OFF
VCC_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF

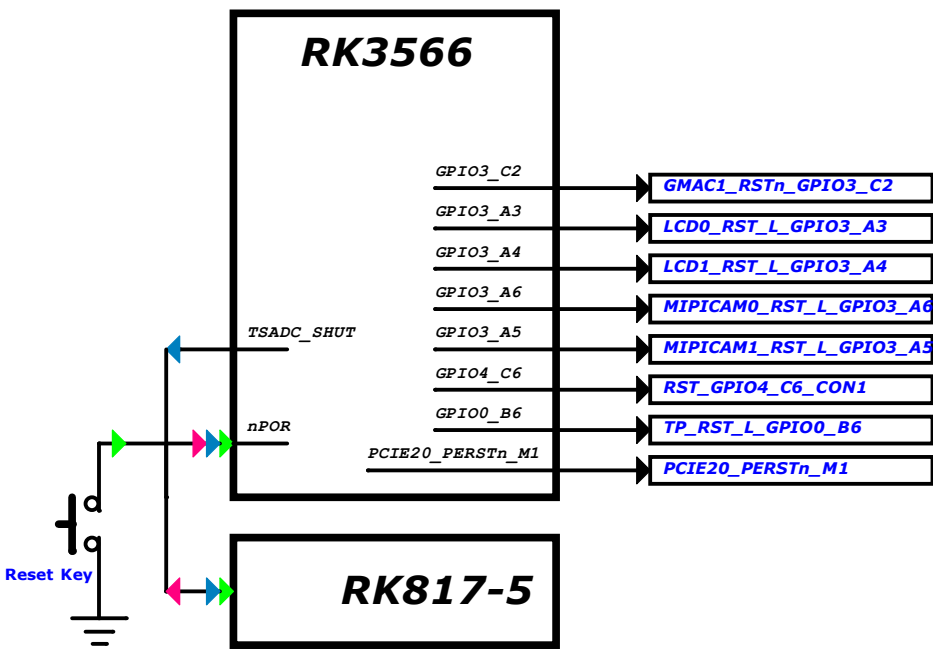
IO Power Domain Map

Refer to the actual design!

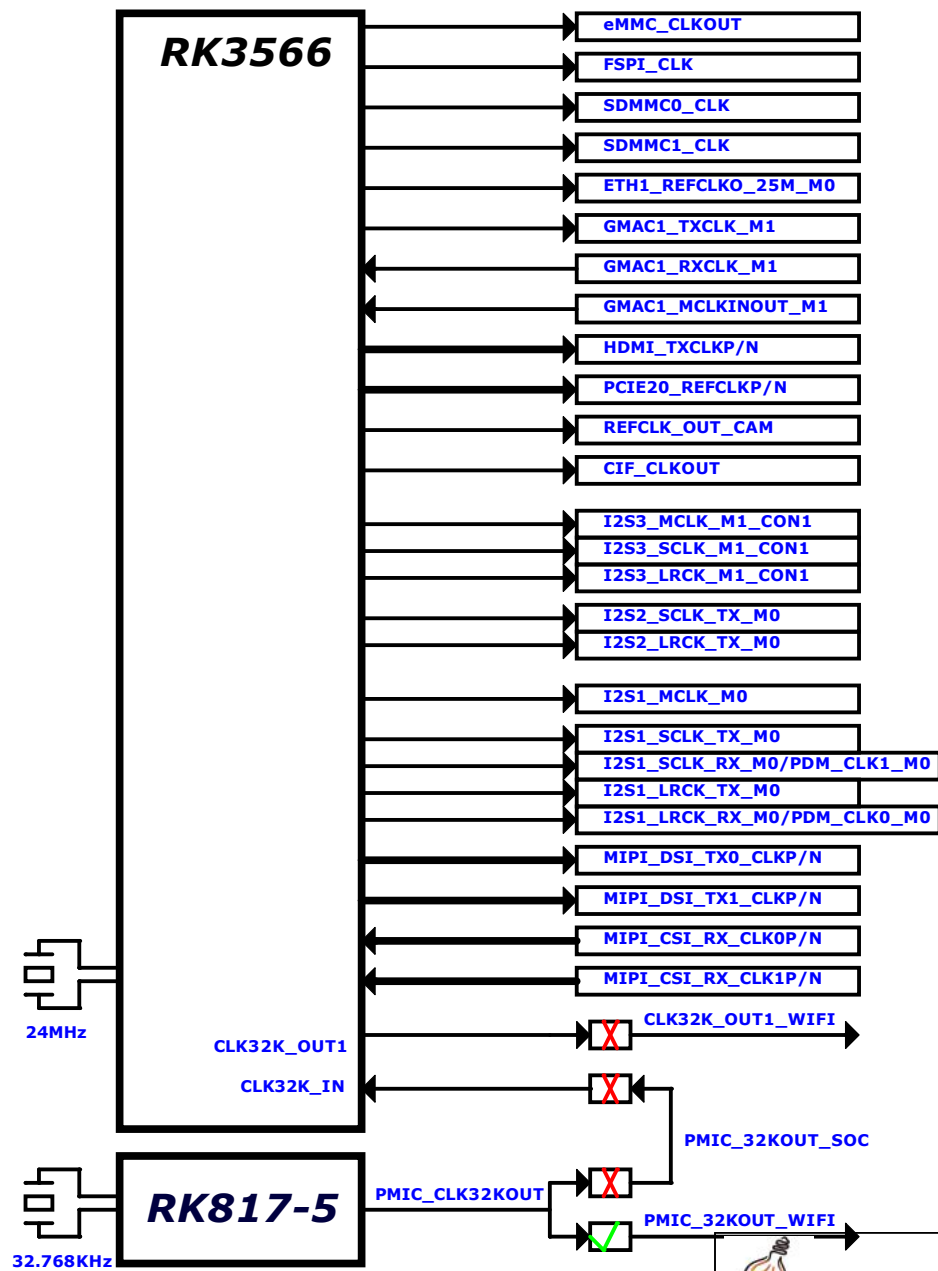
IO Domain	Pin Num	Support IO Voltage		Assignment IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	1P16	YES	NO	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	1N15	YES	YES	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	1D13	YES	YES	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	1C13	YES	YES	VCCIO_FLASH	VCC_1V8	1.8V	FLASH_VOL_SEL = 1 --> VCCIO_FLASH = 1.8V
VCCIO3	1F17	YES	YES	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	1E16	YES	YES	VCCIO4	VCCA1V8_PMU	1.8V	
VCCIO5	1N5 1N6	YES	YES	VCCIO5	VCC_1V8	1.8V	
VCCIO6	1L4 1L5	YES	YES	VCCIO6	VCC1V8_DVP	1.8V	
VCCIO7	1N8	YES	YES	VCCIO7	VCC_3V3	3.3V	



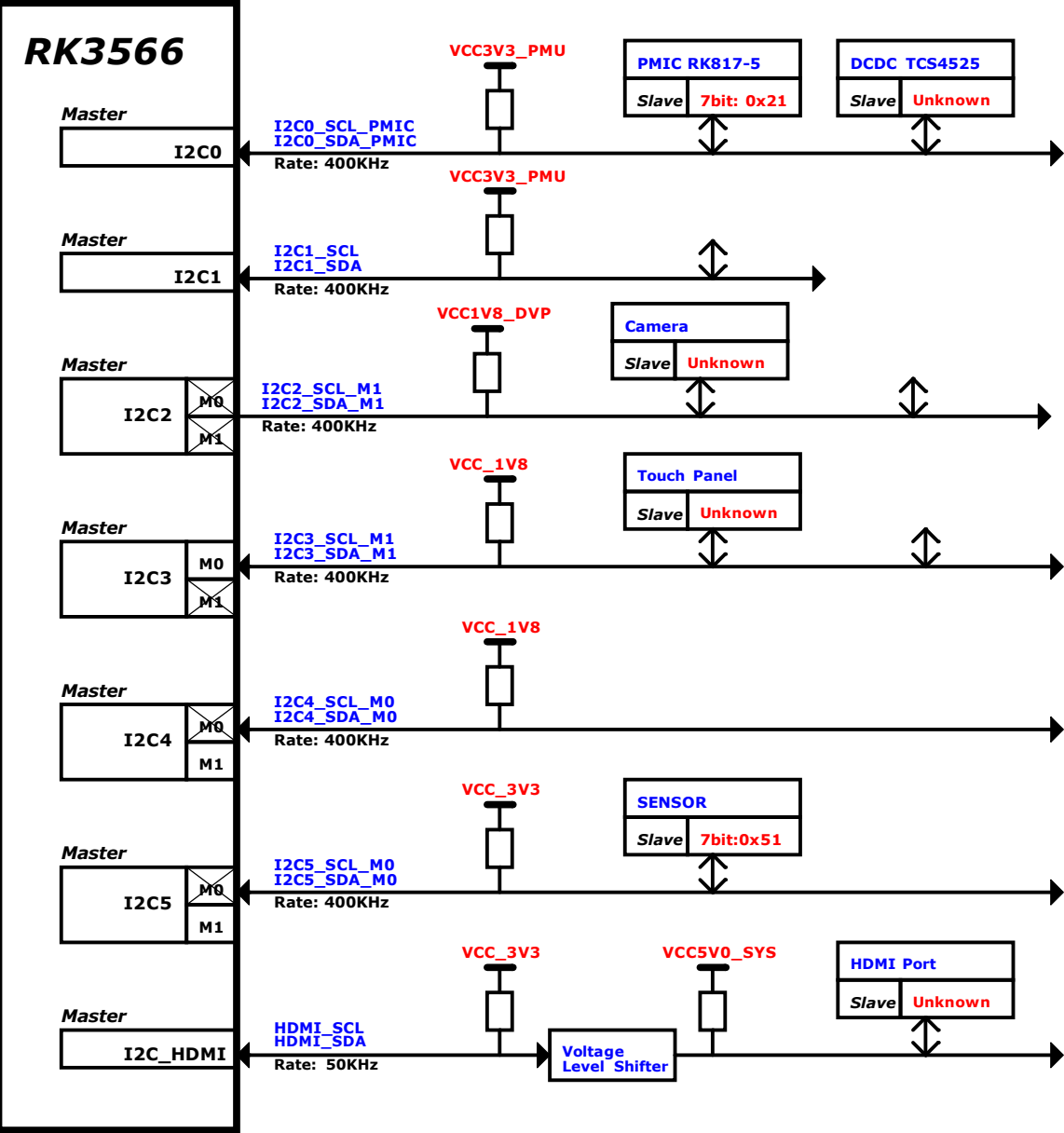
RESET Signal MAP



Clock Map



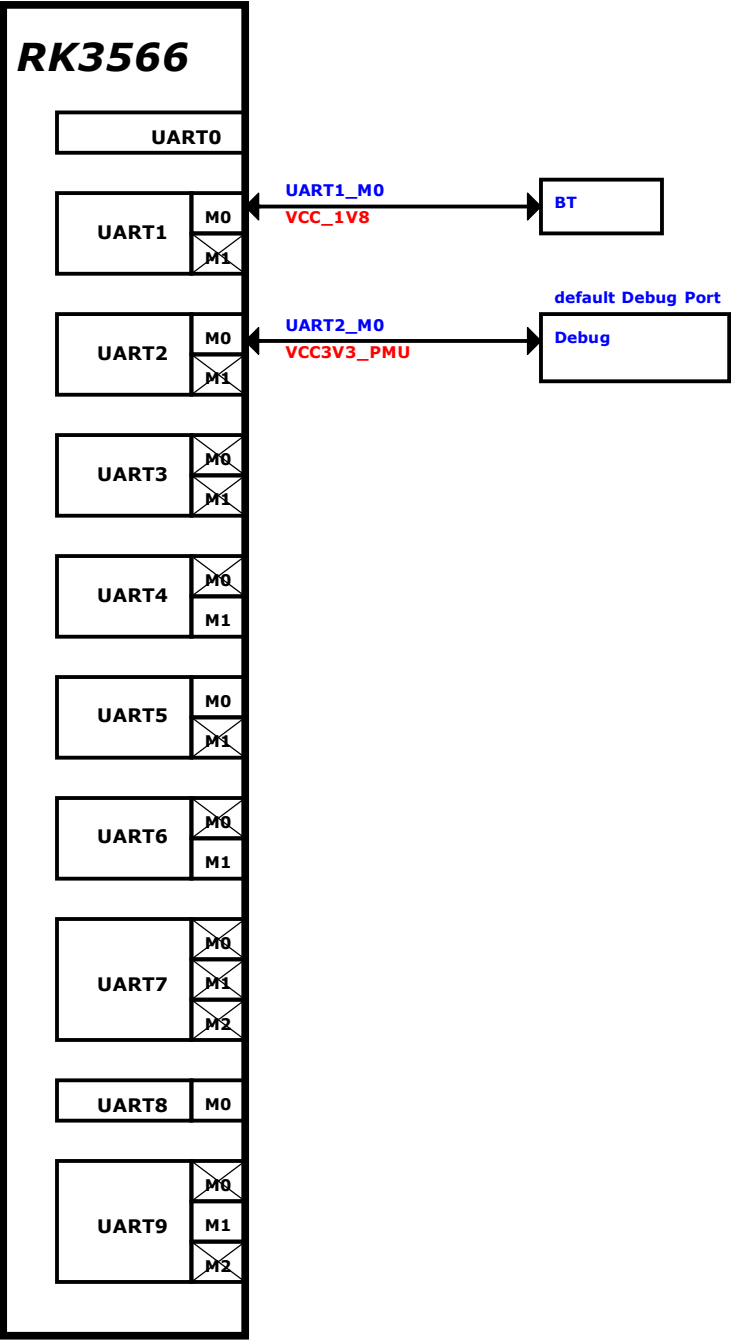
I2C MAP



www.t-firefly.com

Title: I2C Bus Map	
File: ROC-3566-PC	REV: V0.1
Create Date: Monday, March 30, 2020	Page Num: 8
Modify Date: Tuesday, June 01, 2021	Page Total: 37

UART MAP



M0

M1

Unselected IOmux path
IOmux path in use

RK3566_ABCDE

(Power&GND)

U1000A

VDD_CPU_1
VDD_CPU_2
VDD_CPU_3
VDD_CPU_4
VDD_CPU_5
VDD_CPU_6
VDD_CPU_7
VDD_CPU_8
VDD_CPU_9
VDD_CPU_10
VDD_CPU_11

1C12
1D11
1D12
1E11
1E12
1E13
1F11
1F12
1F13
1F14
1G13

C1000 4.7uF
C1002 4.7uF
C1003 22uF
X5R
6.3V
C0402
X5R
6.3V
C0402
X5R
6.3V
C0603

VDD_LOGIC_1
VDD_LOGIC_2
VDD_LOGIC_3
VDD_LOGIC_4
VDD_LOGIC_5
VDD_LOGIC_6
VDD_LOGIC_7
VDD_LOGIC_8
VDD_LOGIC_9

1H7
1H8
1H9
1H10
1J7
1J10
1K7
1K10
1L7

C1005 100nF
C1006 4.7uF
C1007 4.7uF
C1008 4.7uF
C1009 22uF
X5R
10V
C0201
X5R
6.3V
C0402
X5R
6.3V
C0402
X5R
6.3V
C0402
X5R
6.3V
C0603

VDD_GPU_1
VDD_GPU_2
VDD_GPU_3
VDD_GPU_4
VDD_GPU_5

1L8
1L9
1M7
1M8
1M9

C1012 100nF
C1013 4.7uF
C1014 22uF
X5R
10V
C0201
X5R
6.3V
C0402
X5R
6.3V
C0603

VDD_NPU_1
VDD_NPU_2
VDD_NPU_3
VDD_NPU_4
VDD_NPU_5

1G15
1H14
1H15
1J14
1J15

C1017 100nF
C1018 22uF
X5R
10V
C0201
X5R
6.3V
C0603

RK3566
BGA565_15R50X14R40X0R90

Caps should be placed under the U1000 package

Caps should be placed close to the U1000 package

U1000B

VSS_1
VSS_2
VSS_3
VSS_4
VSS_5
VSS_6
VSS_7
VSS_8
VSS_9
VSS_10
VSS_11
VSS_12
VSS_13
VSS_14
VSS_15
VSS_16
VSS_17
VSS_18
VSS_19
VSS_20
VSS_21
VSS_22
VSS_23
VSS_24
VSS_25
VSS_26
VSS_27
VSS_28
VSS_29
VSS_30
VSS_31
VSS_32
VSS_33
VSS_34
VSS_35
VSS_36
VSS_37
VSS_38
VSS_39
VSS_40
VSS_41
VSS_42
VSS_43
VSS_44
VSS_45
VSS_46
VSS_47
VSS_48
VSS_49
VSS_50

A1
A2
A38
B1
B2
B6
B11
B14
B18
B21
B28
B31
D2
J2
L2
U2
W2
AA2
AD2
AP2
AR1
AP8
E37
AC37
AE37
AH37
AL37
AP37
AR38
B10
B11
B15
B19
C4
C5
C6
C8
C9
C14
C18
D1
D3
D10
D14
E3
E8
E10
E14
E15

RK3566
BGA565_15R50X14R40X0R90

U1000C

VSS_51
VSS_52
VSS_53
VSS_54
VSS_55
VSS_56
VSS_57
VSS_58
VSS_59
VSS_60
VSS_61
VSS_62
VSS_63
VSS_64
VSS_65
VSS_66
VSS_67
VSS_68
VSS_69
VSS_70
VSS_71
VSS_72
VSS_73
VSS_74
VSS_75
VSS_76
VSS_77
VSS_78
VSS_79
VSS_80
VSS_81
VSS_82
VSS_83
VSS_84
VSS_85
VSS_86
VSS_87
VSS_88
VSS_89
VSS_90
VSS_91
VSS_92
VSS_93
VSS_94
VSS_95
VSS_96
VSS_97
VSS_98
VSS_99
VSS_100

1F17
1F6
1F7
1F8
1F9
1F10
1F15
1F16
1G3
1G6
1G7
1G8
1G9
1G10
1G11
1G12
1G14
1H1
1H2
1H6
1H11
1H12
1H13
1J1
1J6
1J8
1J9
1J11
1J12
1J13
1K2
1K3
1K4
1K5
1K6
1K8
1K9
1K11
1K12
1K13
1K14
1K15
1L3
1L6
1L10
1L11
1L12
1L13
1L14
1L15

RK3566
BGA565_15R50X14R40X0R90

U1000D

VSS_101
VSS_102
VSS_103
VSS_104
VSS_105
VSS_106
VSS_107
VSS_108
VSS_109
VSS_110
VSS_111
VSS_112
VSS_113
VSS_114
VSS_115
VSS_116
VSS_117
VSS_118
VSS_119
VSS_120
VSS_121
VSS_122
VSS_123
VSS_124
VSS_125
VSS_126
VSS_127
VSS_128
VSS_129
VSS_130
VSS_131

1M3
1M4
1M5
1M6
1M10
1M11
1M12
1M13
1M14
1M15
1M16
1M17
1M20
1N3
1N4
1N7
1P1
1P5
1P6
1P7
1P15
1R3
1R4
1R5
1R6
1R7
1T3
1T5
1U2
1V1
1V4

RK3566
BGA565_15R5x14R4x0R90

U1000E

AVSS_1
AVSS_2
AVSS_3
AVSS_4
AVSS_5
AVSS_6
AVSS_7
AVSS_8
AVSS_9
AVSS_10
AVSS_11
AVSS_12
AVSS_13
AVSS_14
AVSS_15
AVSS_16
AVSS_17
AVSS_18
AVSS_19
AVSS_20
AVSS_21
AVSS_22
AVSS_23
AVSS_24
AVSS_25
AVSS_26
AVSS_27
AVSS_28
AVSS_29
AVSS_30
AVSS_31
AVSS_32
AVSS_33
AVSS_34
AVSS_35
AVSS_36
AVSS_37
AVSS_38
AVSS_39
AVSS1_1
AVSS1_2
AVSS1_3
AVSS1_4
AVSS1_5
AVSS1_6
AVSS1_7
AVSS1_8
AVSS1_9
AVSS1_10
AVSS1_11
AVSS1_12
AVSS1_13
AVSS1_14

AP13
AP16
AP19
AP22
AP25
AP28
AP31
AP34
1N11
1N12
1P8
1P10
1P14
1R8
1R9
1R11
1R12
1R13
1R14
1R15
1T7
1T8
1T9
1T10
1T11
1T12
1T13
1T14
1T15
1T16
1T17
1U2
1U3
1U5
1U7
1V7
1V12
1V13
1V18
H37
L37
P37
U37
Y37
1F20
1G16
1G18
1G19
1G20
1J16
1J18
1K18
1L19

RK3566
BGA565_15R50X14R40X0R90



www.t-firefly.com

Title: RK3566 Power/GND

File: ROC-3566-PC

REV: V0.1

Create Date: Monday, March 30, 2020

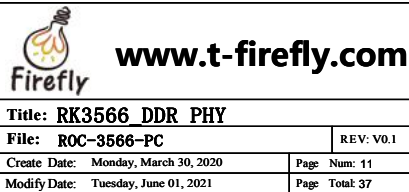
Page Num: 10

Modify Date: Tuesday, June 01, 2021

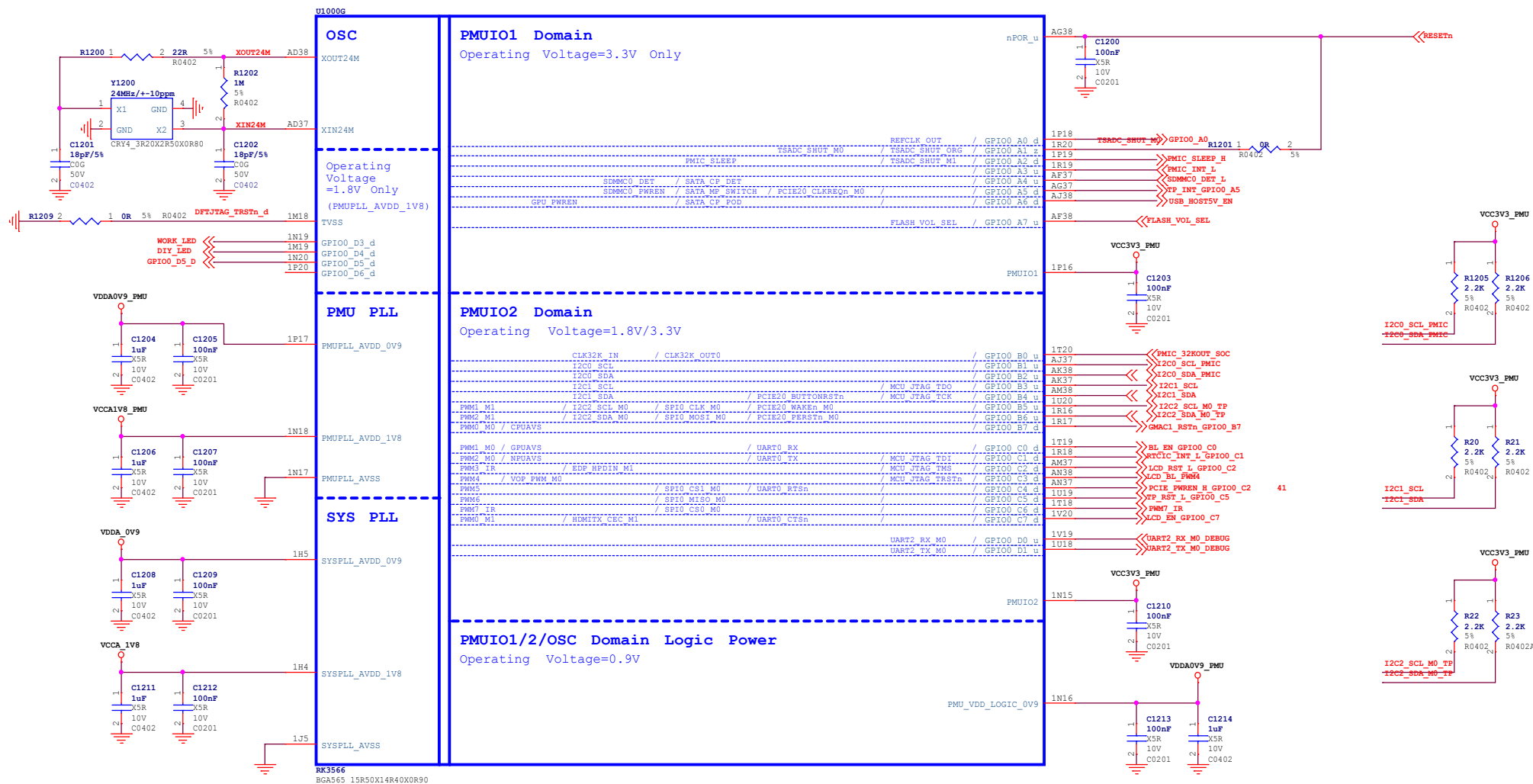
Page Total: 37

Rockchip Confidential

Rockchip Confidential



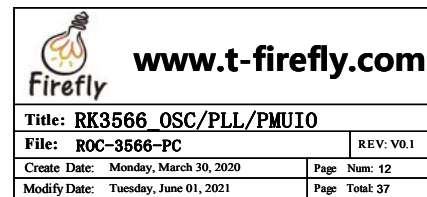
RK3566 G (OSC/PLL/PMUIO1/2)



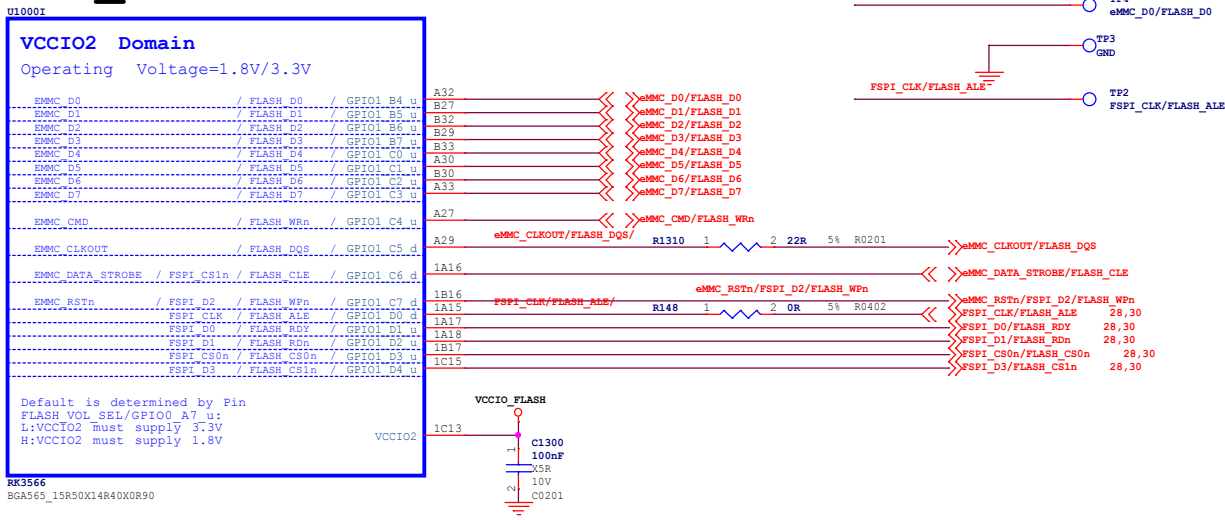
Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

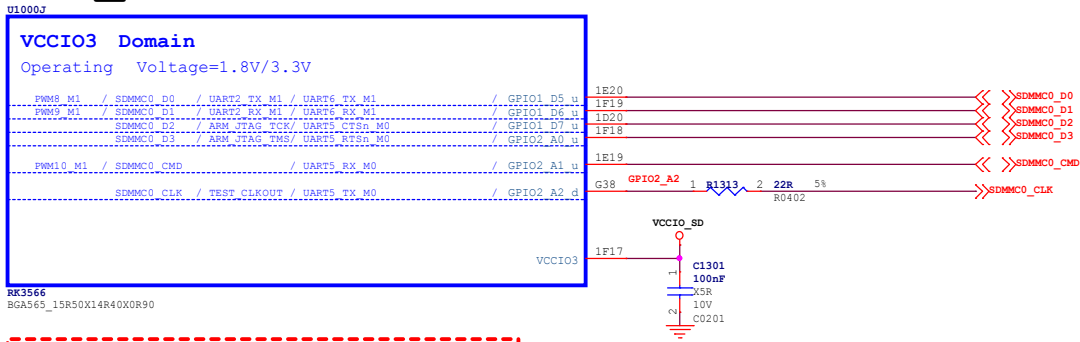
Rockchip Confidential



RK3566_I (VCCIO2 Domain)

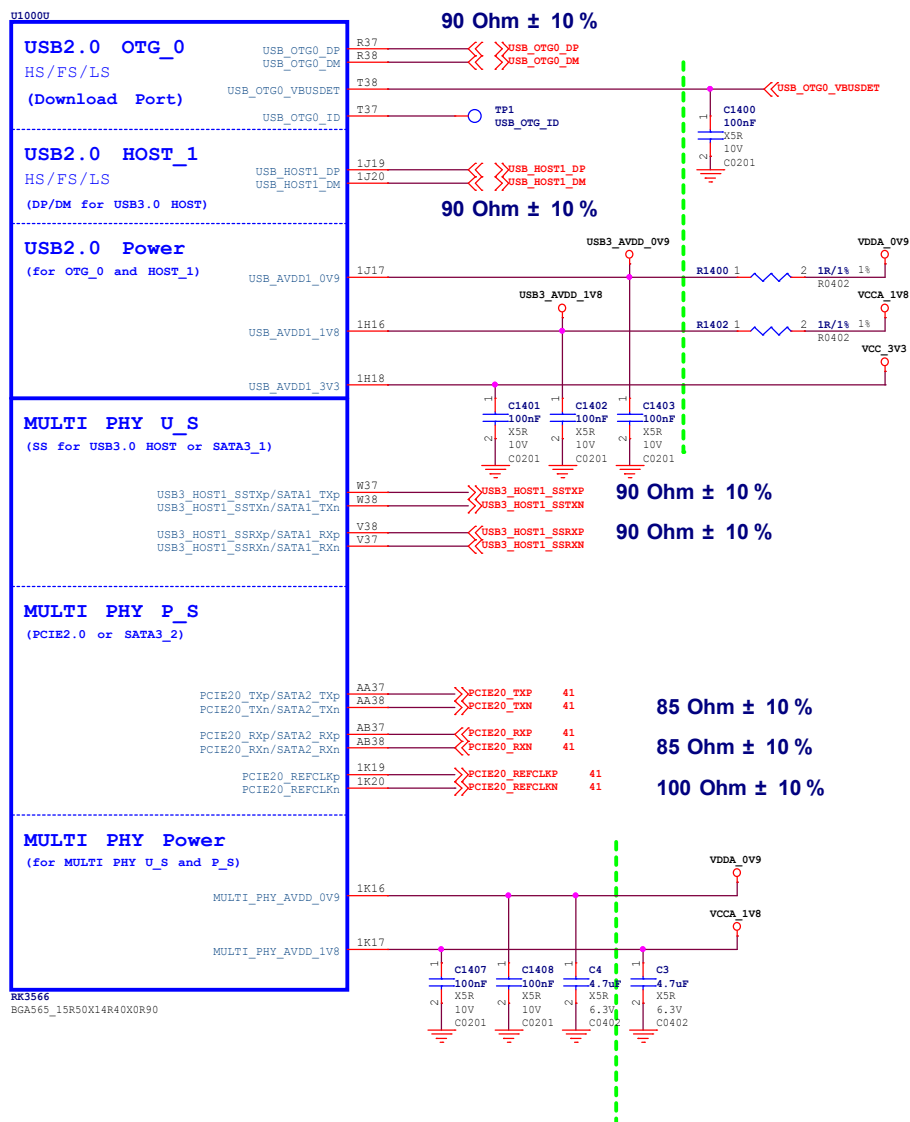


RK3566_J (VCCIO3 Domain)



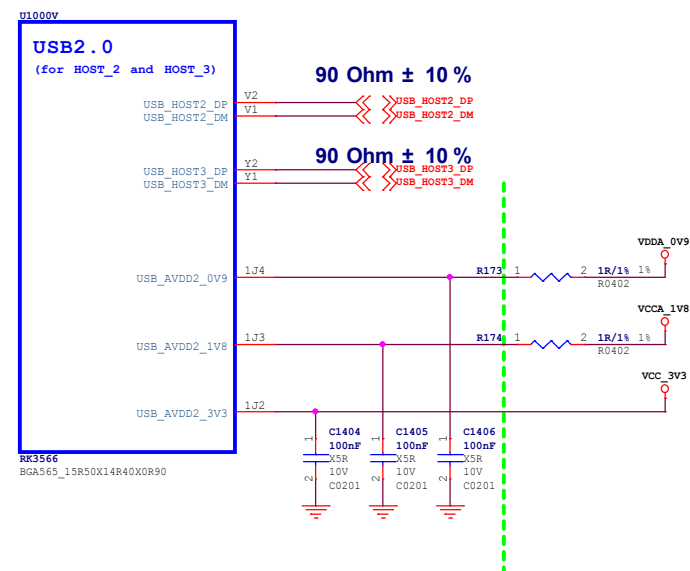
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3566 V (USB2.0 HOST)



Note :

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



www.t-firefly.com

Title: RK3566 USB/PCIe/SATA PHY

File: ROC-3566-PC

REV: V0.1

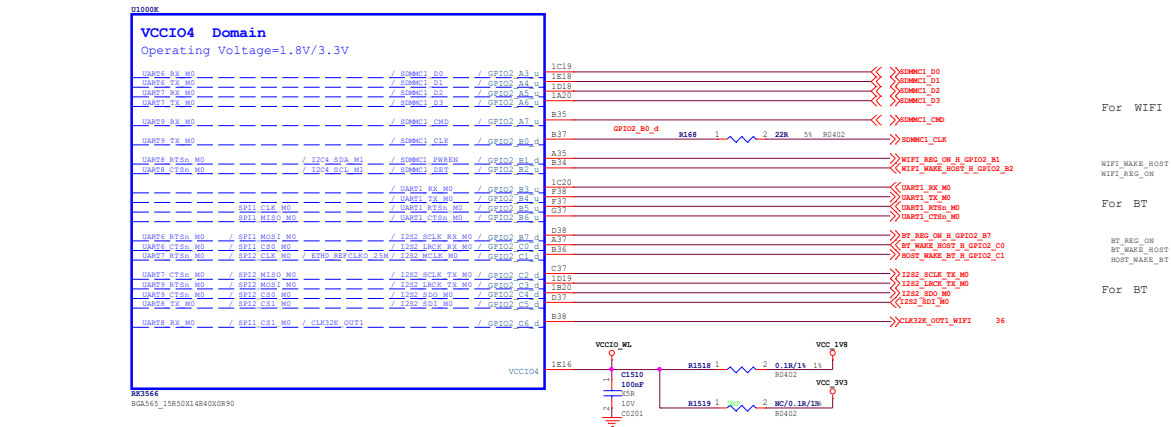
Create Date: Monday, March 30, 2020

Page Num: 14

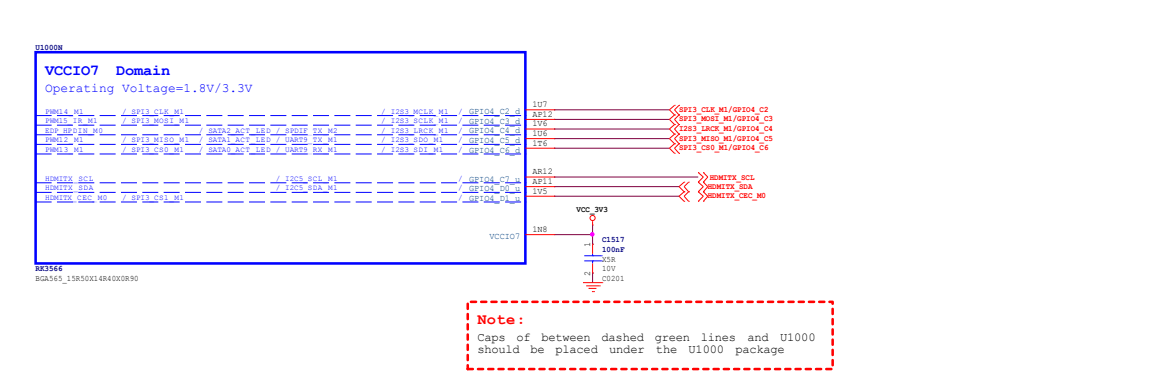
Modify Date: Tuesday, June 01, 2021

Page Total: 37

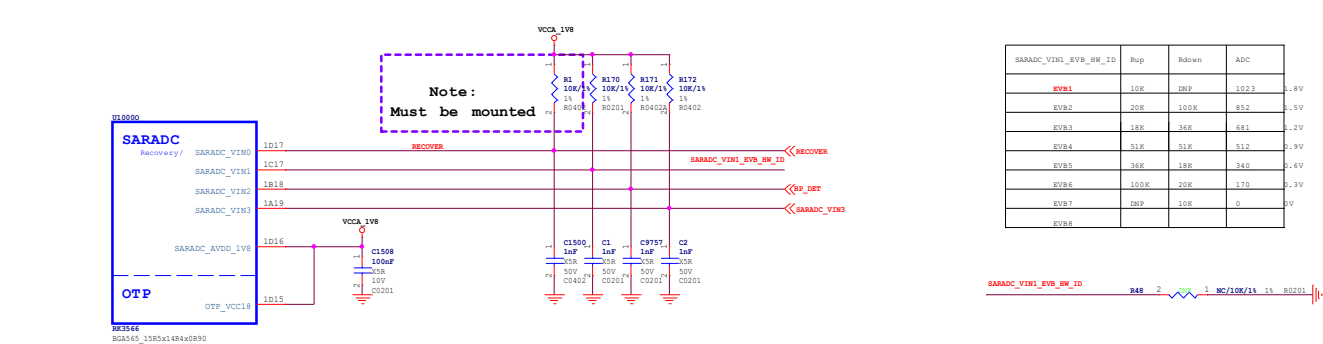
RK3566_K(VCCIO4 Domain)



RK3566_N(VCCIO7 Domain)



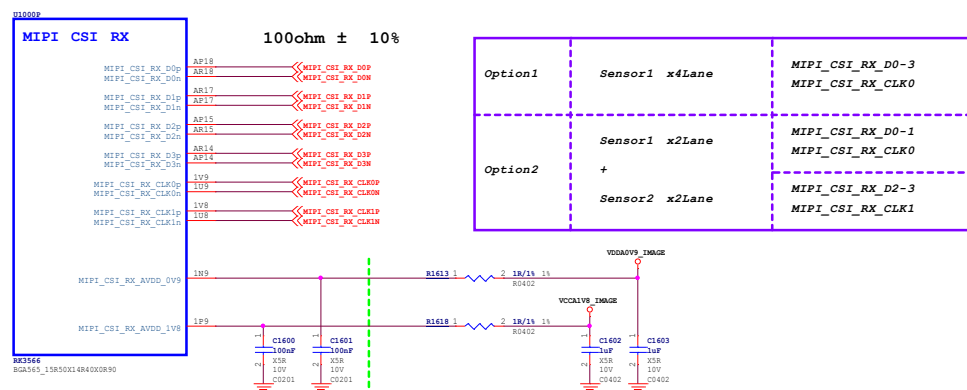
RK3566_O (SARADC/OTP)



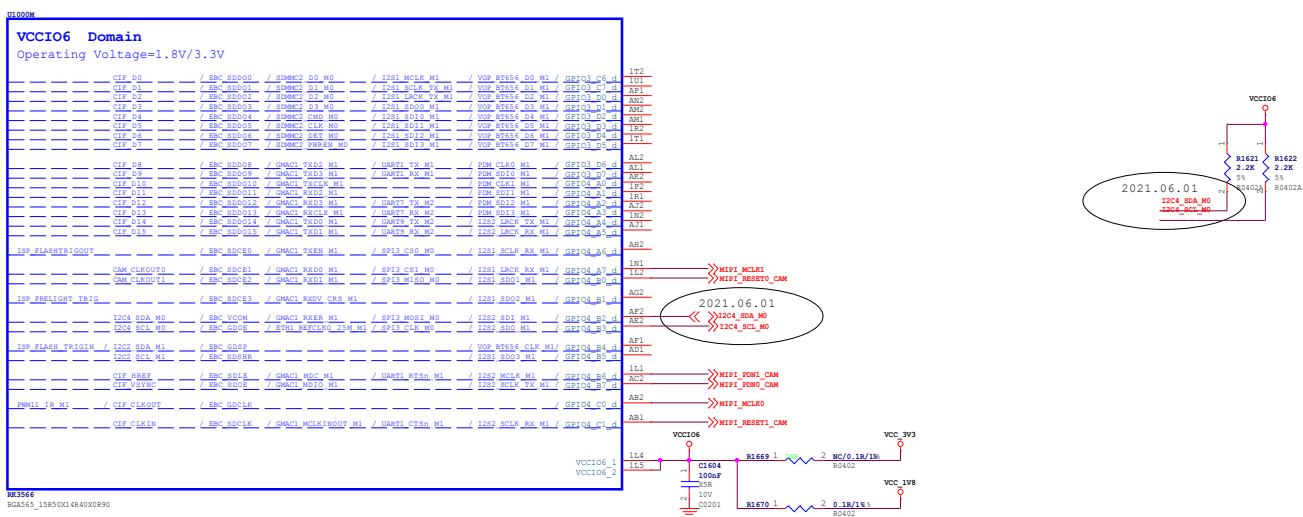
SARADC_VIN1_EVB_HW_ID	Up	Down	ADC	
EVB1	10K	20K	1023	1.8V
EVB2	20K	100K	852	1.5V
EVB3	18K	36K	681	1.2V
EVB4	51K	51K	512	0.9V
EVB5	36K	18K	340	0.6V
EVB6	100K	20K	170	0.3V
EVB7	20K	10K	0	0V
EVB8				



RK3566 P (MIPI CSI RX)



RK3566 M(VCCIO6 Domain)



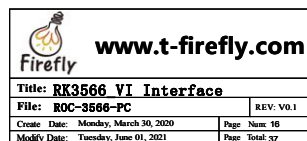
Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support	BT601	YCbCr	422	8bit	input
Support	BT656	YCbCr	422	8bit	input
Support	RAW	8/10/12bit	input		
Support	BT1120	YCbCr	422	8/10/12/16bit	input, single/dual-edge sampling
Support	2/4 mixed	BT656/BT1120	YCbCr	422	8bit input

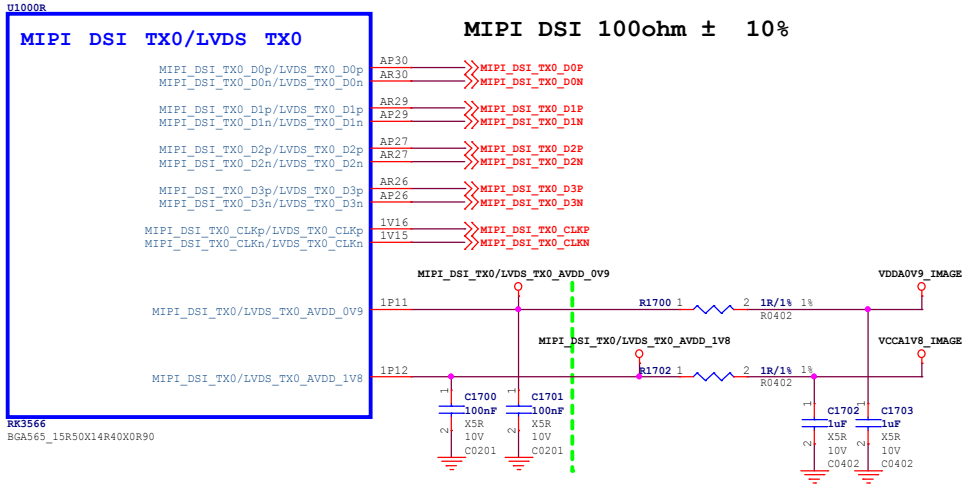
Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

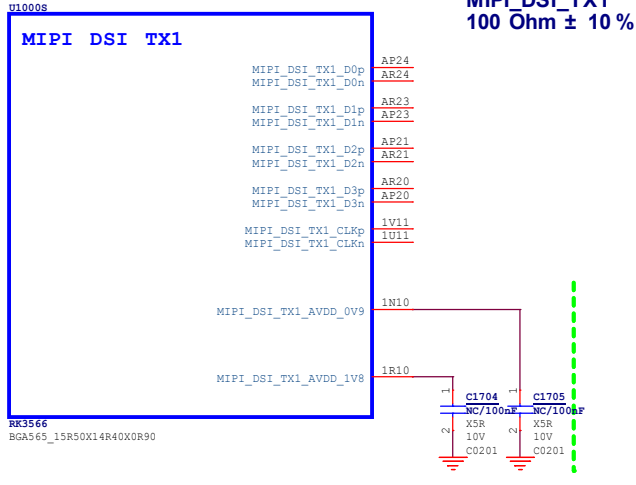
Rockchip Confidential



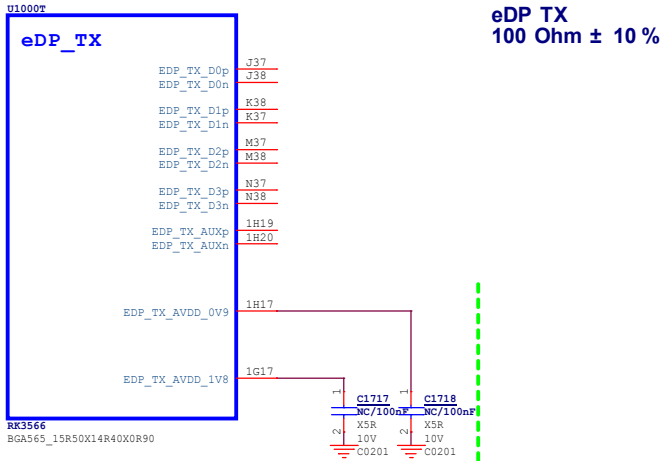
RK3566_R (MIPI_DSI_TX0/LVDS_TX0)



RK3566_S (MIPI_DSI_TX1)



RK3566_T (eDP/DP TX)

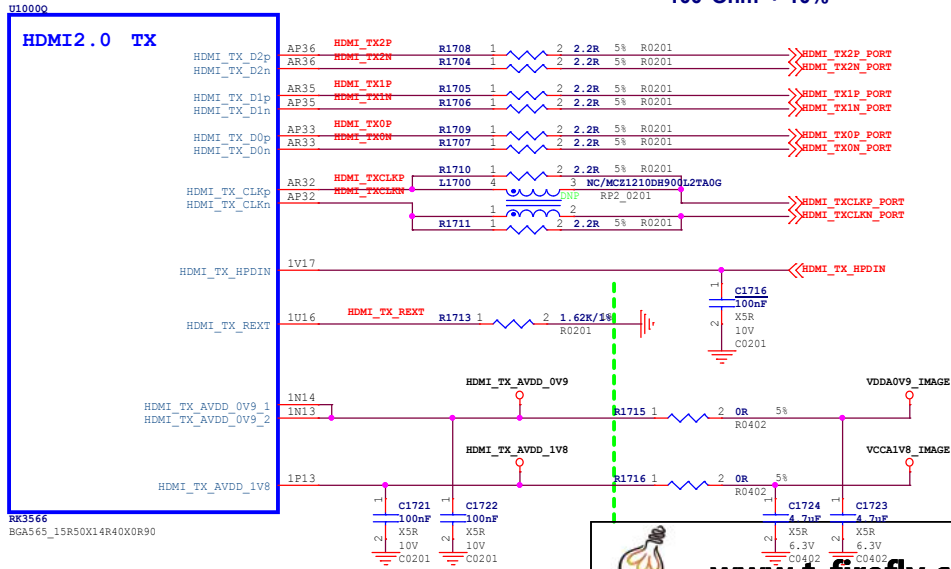


Boxed capacitors should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

RK3566_Q (HDMI2.0 TX)



Title: RK3566_V0 Interface 1		
File: ROC-3566-PC		REV: V0.1
Create Date: Monday, March 30, 2020	Page	Num: 17
Modify Date: Tuesday, June 01, 2021	Page	Total: 37

Rockchip Confidential

VCCI05 Domain

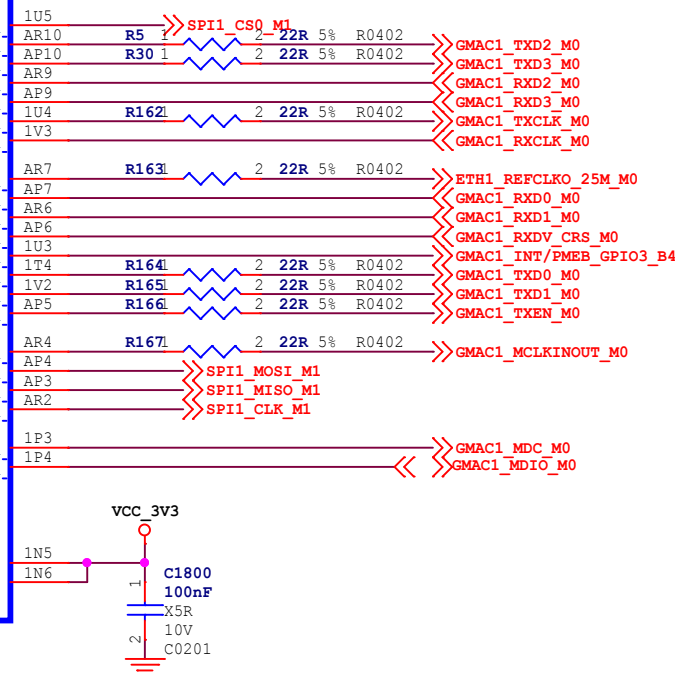
Operating Voltage=1.8V/3.3V

	VOP BT1120 D0	/ SPI1 CS0 M1		/ SDMMC2 D0 M1	/ GPIO3 A1 d
	VOP BT1120 D1	/ GMAC1 TXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1	/ GPIO3 A2 d
	VOP BT1120 D2	/ GMAC1 TXD3 M0	/ I2S3 SCLK M0	/ SDMMC2 D2 M1	/ GPIO3 A3 d
	VOP BT1120 D3	/ GMAC1 RXD2 M0	/ I2S3 LRCK M0	/ SDMMC2 D3 M1	/ GPIO3 A4 d
	VOP BT1120 D4	/ GMAC1 RXD3 M0	/ I2S3 SDO M0	/ SDMMC2 CMD M1	/ GPIO3 A5 d
	VOP BT1120 CLK	/ GMAC1 TXCLK M0	/ I2S3 SDI M0	/ SDMMC2 CLK M1	/ GPIO3 A6 d
	VOP BT1120 D5	/ GMAC1 RXCLK M0		/ SDMMC2 DET M1	/ GPIO3 A7 d
	VOP BT1120 D6	/ ETH1 REFCLK0 25M M0		/ SDMMC2 PWREN M1	/ GPIO3 B0 d
PWM8 M0	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1		/ GPIO3 B1 d
PWM9 M0	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1		/ GPIO3 B2 d
	VOP BT1120 D9	/ I2C5 SCL M0	/ GMAC1 RXDV CRS M0	/ PDM SDI0 M2	/ GPIO3 B3 d
	VOP BT1120 D10	/ I2C5 SDA M0	/ GMAC1 RXER M0	/ PDM SDI1 M2	/ GPIO3 B4 d
PWM10 M0	/ VOP BT1120 D11	/ I2C3 SCL M1	/ GMAC1 TXD0 M0		/ GPIO3 B5 d
PWM11 IR M0	/ VOP BT1120 D12	/ I2C3 SDA M1	/ GMAC1 TXD1 M0		/ GPIO3 B6 d
PWM12 M0		/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SDI2 M2	/ GPIO3 B7 d
PWM13 M0		/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SDI3 M2	/ GPIO3 C0 d
	VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERSTn M1	/ I2S1 SDO2 M2	/ GPIO3 C1 d
	VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ I2S1 SDO3 M2	/ GPIO3 C2 d
	VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ I2S1 SCLK RX M2	/ GPIO3 C3 d
PWM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0	/ UART7 TX M1	/ PDM CLK1 M2	/ GPIO3 C4 d
PWM15 IR M0	/ SPDIF TX M1	/ GMAC1 MDIO M0	/ UART7 RX M1	/ I2S1 LRCK RX M2	/ GPIO3 C5 d

RK3566
BGA565 15R50X14R40X0R90

Note :

Caps of between dashed green lines and U1000 should be placed under the U1000 package



www.t-firefly.com

Title: RK3566 V0 Interface 2

File: ROC-3566-PC

REV: V0.1

Create Date: Wednesday, May 06, 2020

Page Num: 18

Modify Date:	Tuesday, June 01, 2021
--------------	------------------------

Page Total: 37

RK3566_H (VCCIO1 Domain)

U1000H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

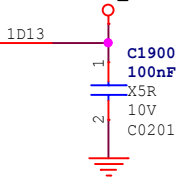
/ I2C3 SDA M0	/ UART3 RX M0	/ AUDIOPWM LOUT p	/ GPIO1 A0 u
/ I2C3 SCL M0	/ UART3 TX M0	/ AUDIOPWM LOUT n	/ GPIO1 A1 u
SCR_CLK	/ I2S1 MCLK M0	/ UART3 RTSn M0	/ GPIO1 A2 d
SCR_IO	/ I2S1 SCLK TX M0	/ UART3 CTSn M0	/ GPIO1 A3 d
	I2S1 SCLK RX M0	/ UART4 RX M0	/ PDM CLK1 M0
		/ SPDIF TX M0	/ GPIO1 A4 d
SCR_RST	/ I2S1 LRCK TX M0	/ UART4 RTSn M0	/ GPIO1 A5 d
	I2S1 LRCK RX M0	/ UART4 TX M0	/ PDM CLK0 M0
		/ AUDIOPWM ROUT p	/ GPIO1 A6 d
SCR_DET	/ I2S1 SDO0 M0	/ UART4 CTSn M0	/ AUDIOPWM ROUT n
	I2S1 SDO1 M0	/ I2S1 SDI3 M0	/ PDM SDI3 M0
		/ PCIE20 CLKREQn M2	/ GPIO1 B0 d
	I2S1 SDO2 M0	/ I2S1 SDI2 M0	/ PDM SDI2 M0
		/ PCIE20 WAKEn M2	/ GPIO1 B1 d
	I2S1 SDO3 M0	/ I2S1 SDI1 M0	/ PDM SDI1 M0
		/ PCIE20 PERSTn M2	/ GPIO1 B2 d
		/ I2S1 SDI0 M0	/ PDM SDI0 M0
			/ GPIO1 B3 d

RK3566
BGA565_15R50X14R40X0R90

VCCIO1

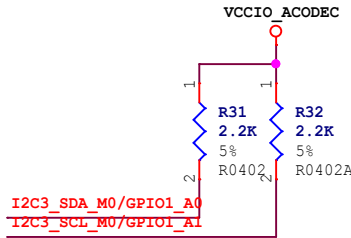
A22	B22	>>>I2C3_SDA_M0/GPIO1_A0
		>>>I2C3_SCL_M0/GPIO1_A1
A23		>>>I2S1_MCLK_M0_RK809
B23	1A13	>>>I2S1_SCLK_TX_M0_RK809
B24	1A14	>>>I2S1_LRCK_TX_M0_RK809
		>>>PDM_CLK0_M0_RK809
B25	1B13	>>>I2S1_SDO0_M0_RK809
		>>>PCIE20_CLKREQn_M2 41
A26		>>>PCIE20_WAKEn_M2 41
B26		>>>PCIE20_PERSTn_M2 41
1B14		>>>I2S1_SDIO_M0/PDM_SDIO_M0_RK809

VCCIO_ACODEC



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package



www.t-firefly.com

Title: RK3566 Audio Interface

File: ROC-3566-PC

REV: V0.1

Create Date: Monday, March 30, 2020

Page Num: 19

Modify Date: Tuesday, June 01, 2021

Page Total: 37

Rockchip Confidential

POWER CONTROL

POWER

RESET

RECOVER

LED DISPLAY

IR

2021.05.14

Firefly www.t-firefly.com

Title: TYPEC-OTG/KEY/IR

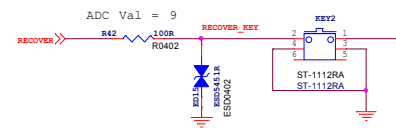
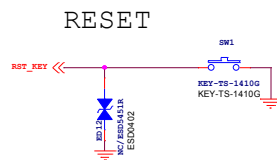
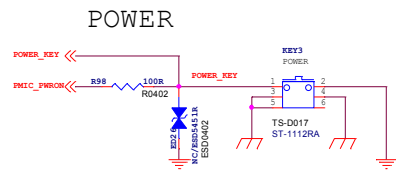
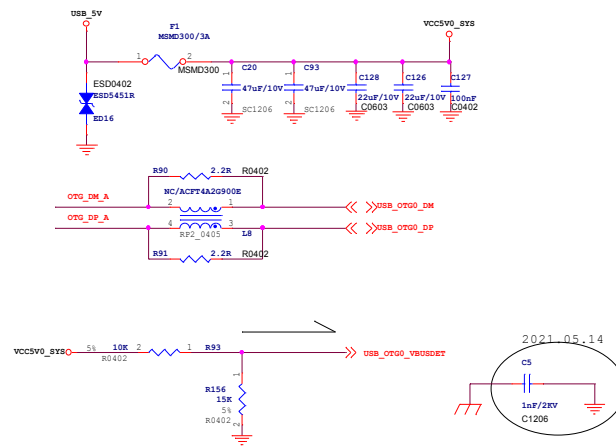
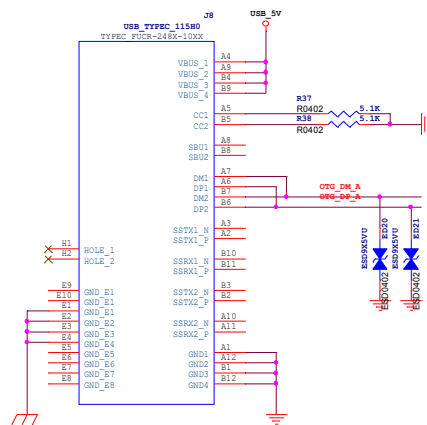
File: ROC-3566-PC

Create Date: Wednesday, January 06, 2021

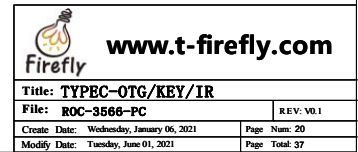
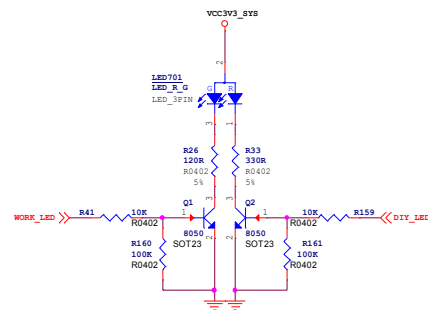
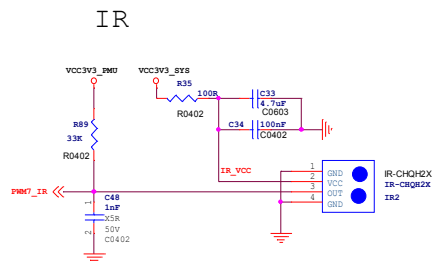
Modify Date: Tuesday, June 01, 2021

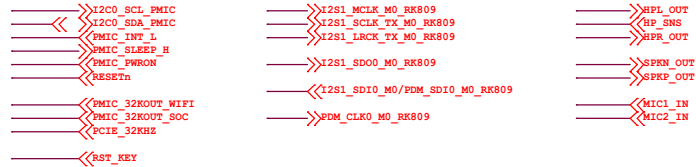
Page Num: 20

Page Total: 37

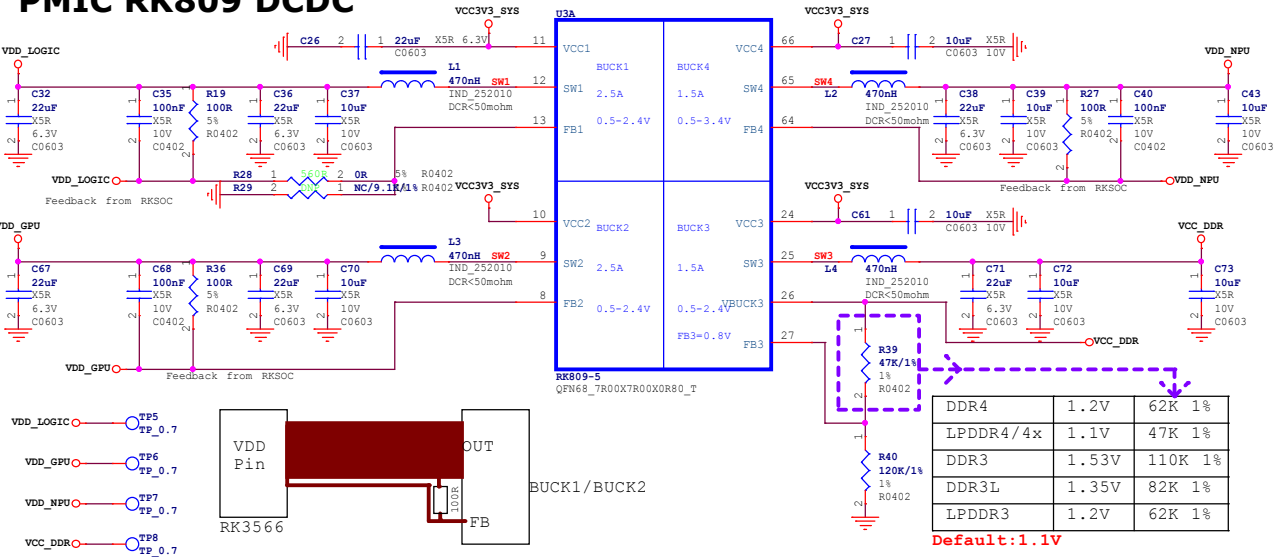


LED DISPLAY

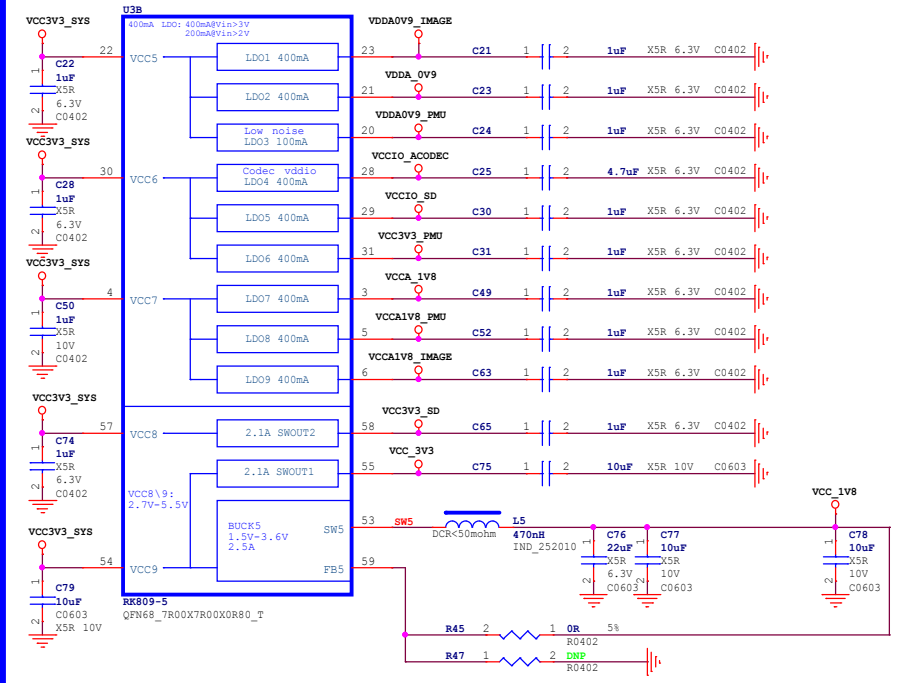




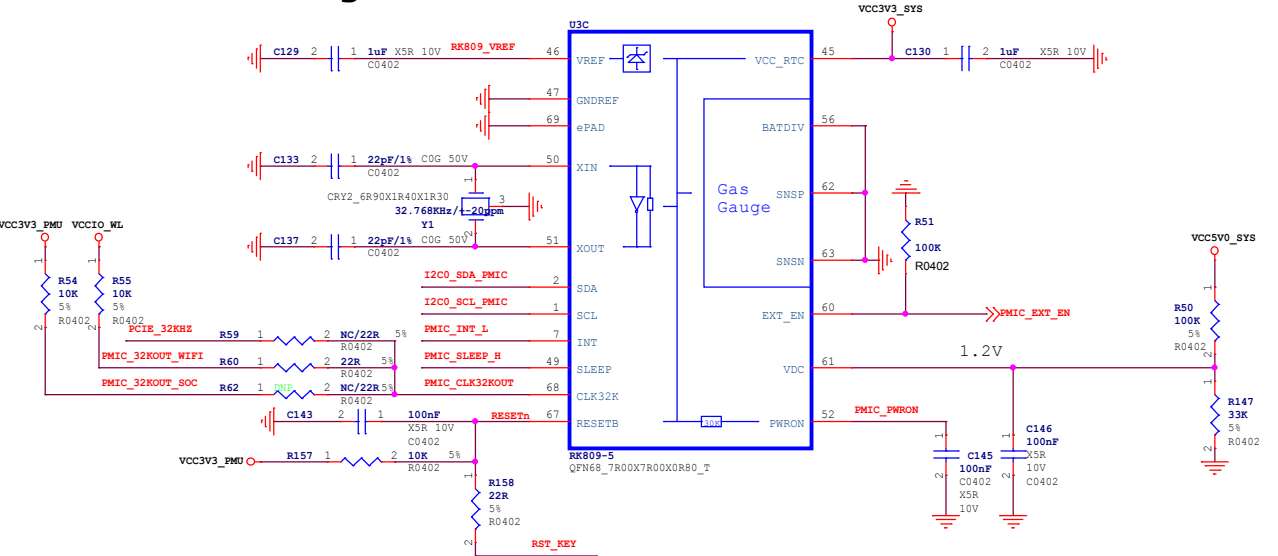
PMIC RK809 DCDC



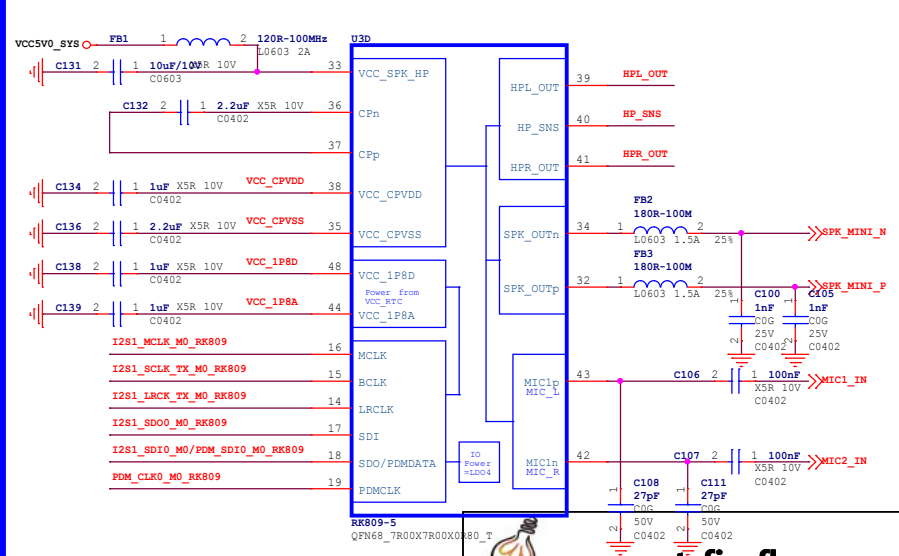
PMIC RK809 LDO



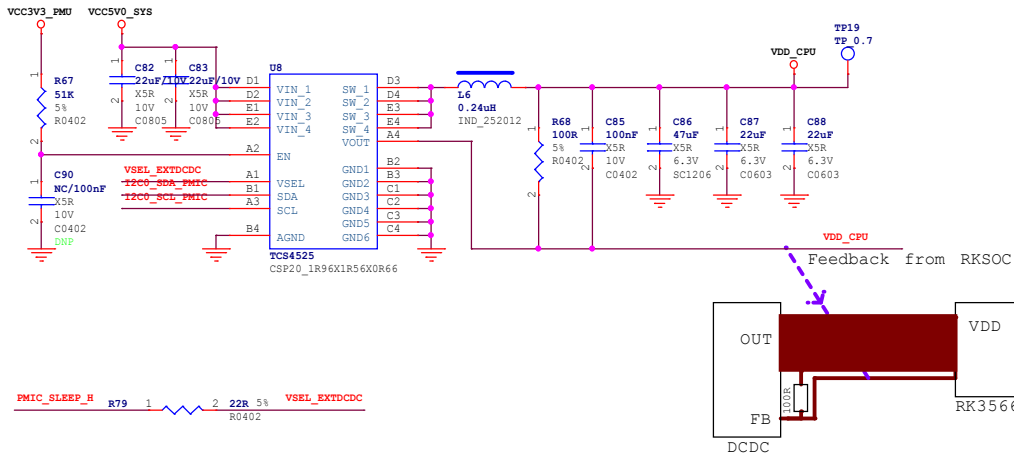
PMIC RK809 Managerment



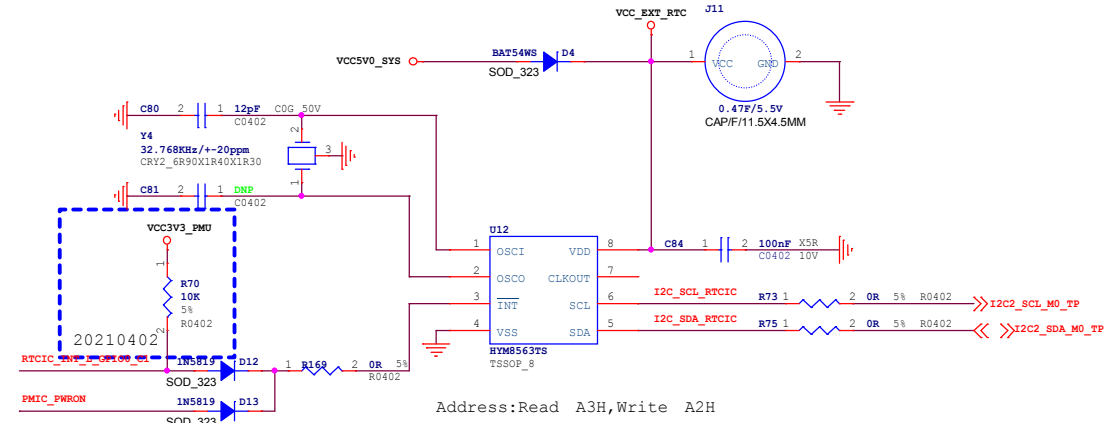
PMIC RK809 CODEC



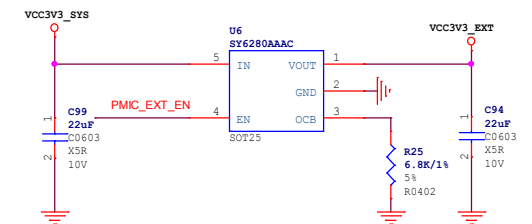
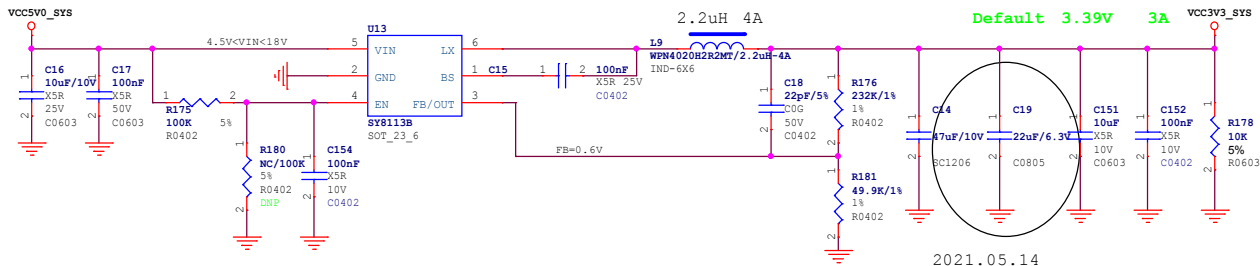
VDD_CPU_EXT



RTC IC



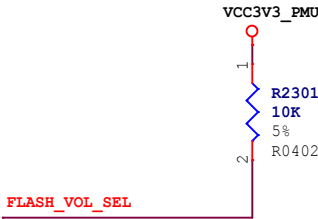
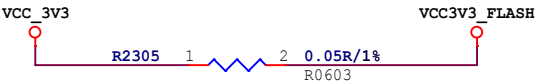
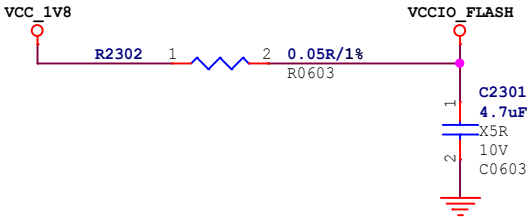
VCC3V3_SYS



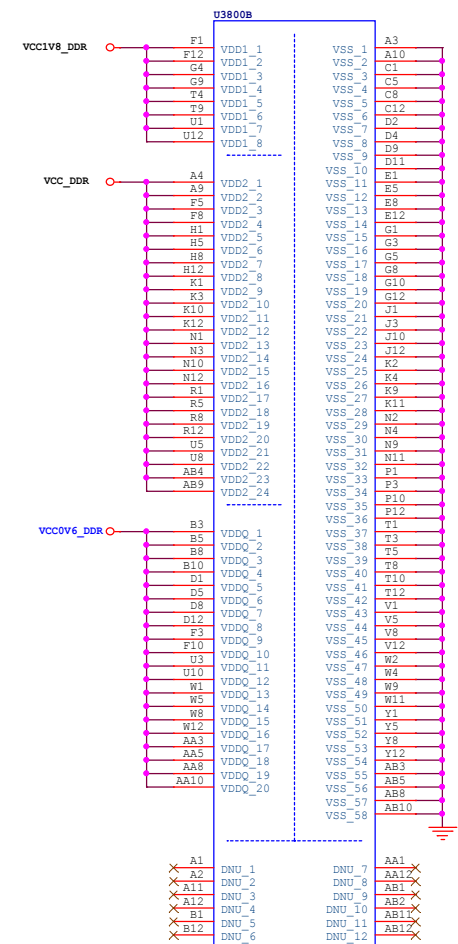
Flash Power Manage

FLASH_VOL_SEL

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)



Note:
FLASH VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L:3.3V IO driven
Logic=H:1.8V IO driven



VCC_DDR

20V

C3801 22uF
6.3V
C0603

C3802 10uF
6.3V
C0603

C3803 10uF
6.3V
C0603

C3804 1uF
10V
X5R

C3805 100nF
10V
X5R

C3806 100nF
10V
X5R

C3807 100nF
10V
X5R

C3808 100nF
10V
X5R

C3809 100nF
10V
X5R

C3810 100nF
10V
X5R

C3811 100nF
10V
X5R

C3812 100nF
10V
X5R

C3813 100nF
10V
X5R

C3814 100nF
10V
X5R

C3815 100nF
10V
X5R

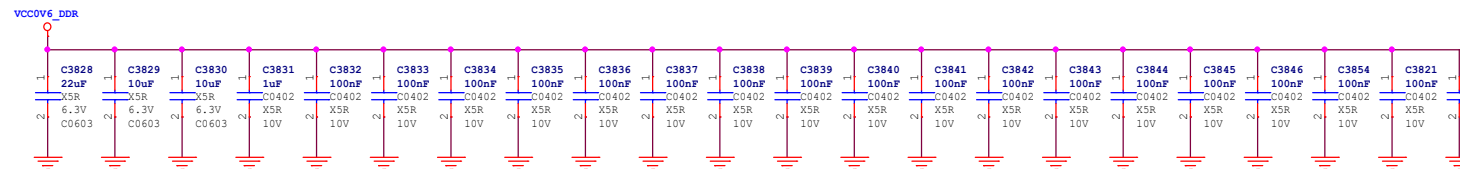
C3816 100nF
10V
X5R

C3817 100nF
10V
X5R

C3818 100nF
10V
X5R

C3819 100nF
10V
X5R

C3820 100nF
10V
X5R



Title: DRAM-LPDDR4X_1X32bit_200P

File: ROC-3566-PC	REV: V0.1
-------------------	-----------

Create Date: Monday, November 30, 2020	Page Num: 24
Modify Date: Tuesday, June 01, 2021	Page Total: 37

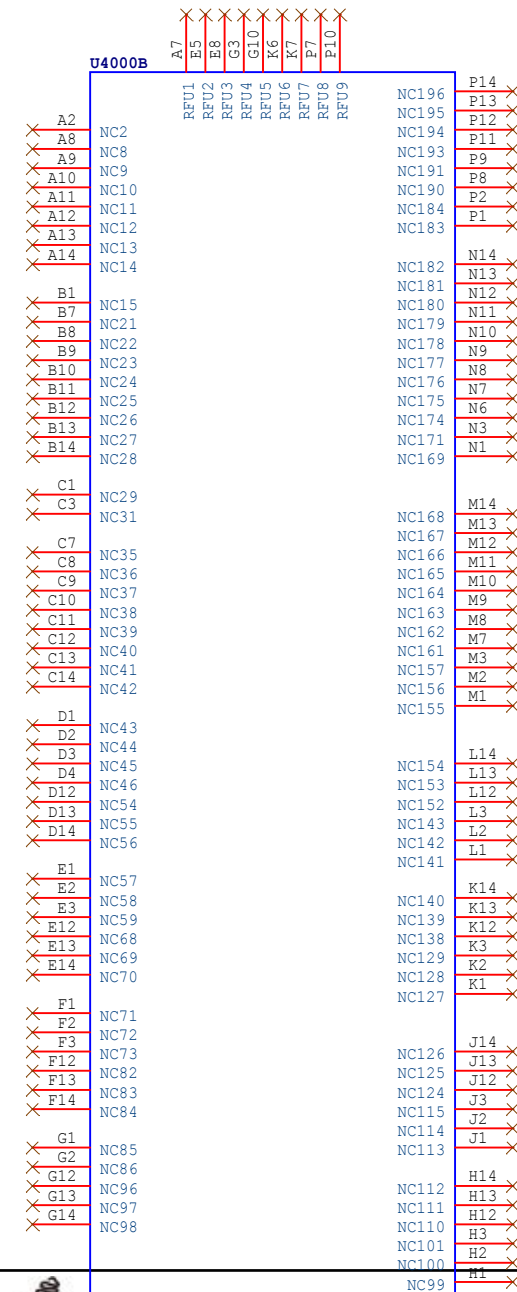
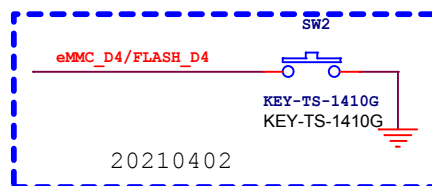
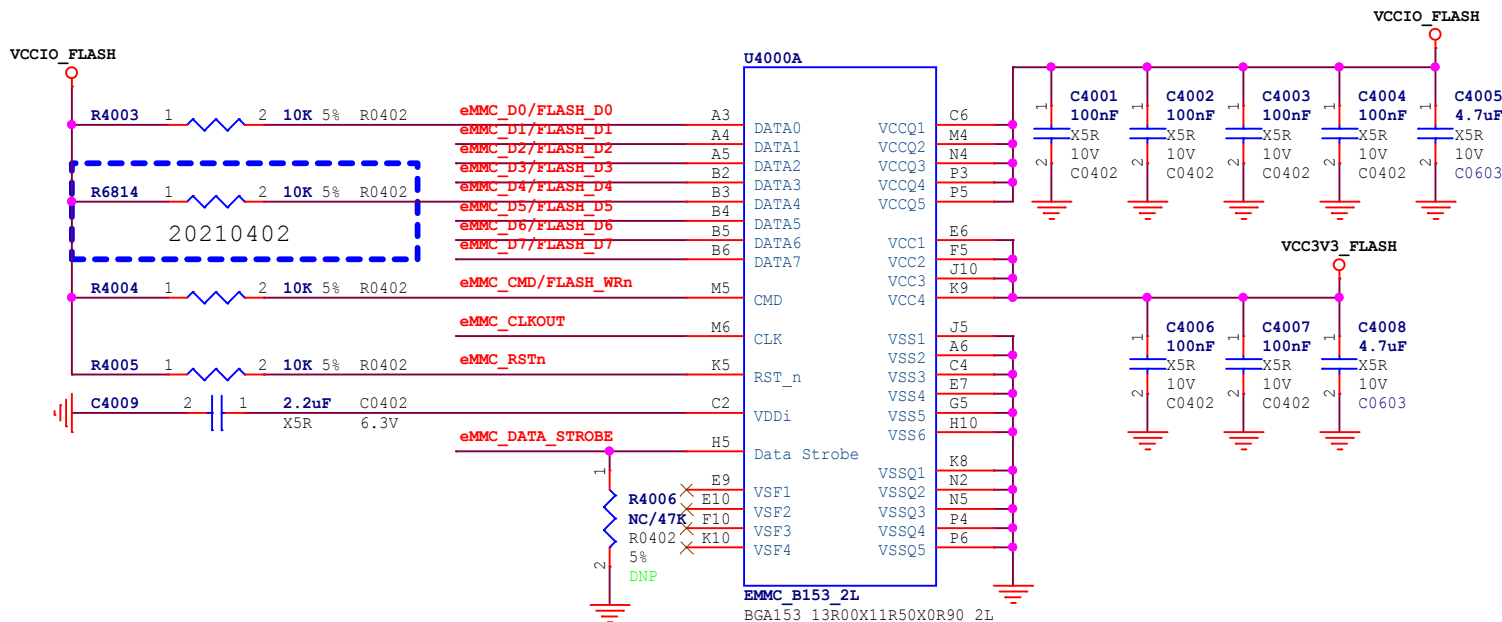
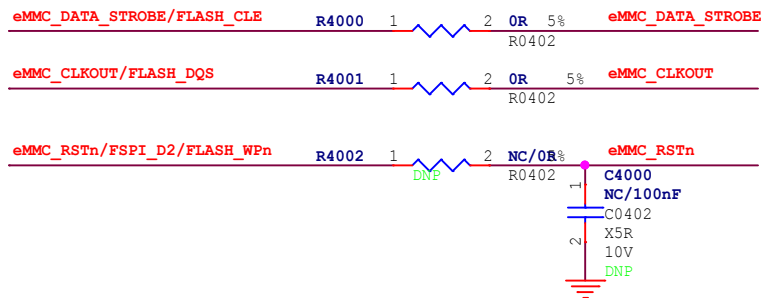
>>eMMC_D0/FLASH_D0
>>eMMC_D1/FLASH_D1
>>eMMC_D2/FLASH_D2
>>eMMC_D3/FLASH_D3
>>eMMC_D4/FLASH_D4
>>eMMC_D5/FLASH_D5
>>eMMC_D6/FLASH_D6
>>eMMC_D7/FLASH_D7

>>eMMC_CMD/FLASH_WRn

>>eMMC_CLKOUT/FLASH_DQS

>>eMMC_DATA_STROBE/FLASH_CLE

>>eMMC_RSTn/FSPI_D2/FLASH_WPn



Firefly

EMMC_B153_2L BGA153_13R00X11R50X0R90_2L

www.t-firefly.com

Title: Flash-eMMC Flash

File: ROC-3566-PC

REV: V0.1

Create Date: Thursday, May 07, 2020

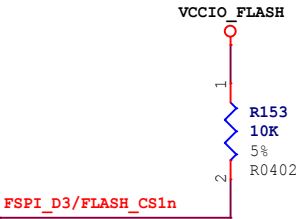
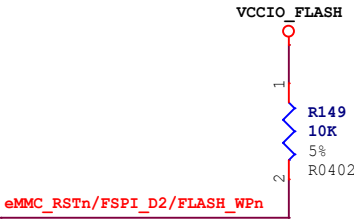
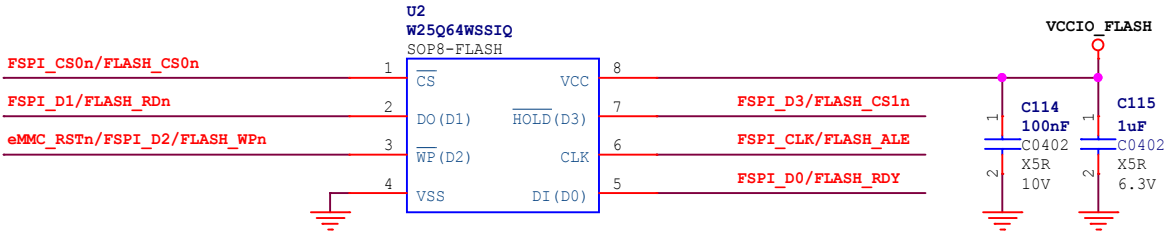
Page Num: 25

Modify Date: Tuesday, June 01, 2021

Page Total: 37

>>FSPI_CLK/FLASH_ALE 14,28
 >>FSPI_D0/FLASH_RDY 14,28
 >>FSPI_D1/FLASH_RDn 14,28
 >>eMMC_RSTn/FSPI_D2/FLASH_WPn 14,27,28
 >>FSPI_D3/FLASH_CS1n 14,28
 >>FSPI_CS0n/FLASH_CS0n 14,28

default VCC = 1.8V

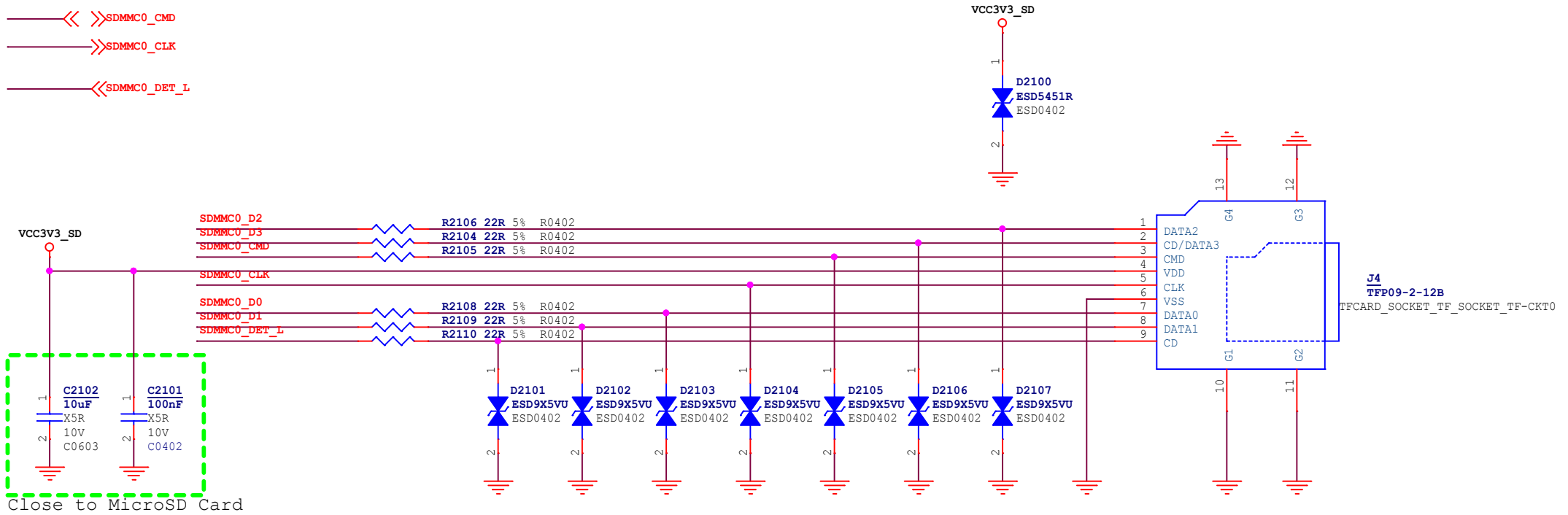


>>>SDMMC0_D0
>>>SDMMC0_D1
>>>SDMMC0_D2
>>>SDMMC0_D3

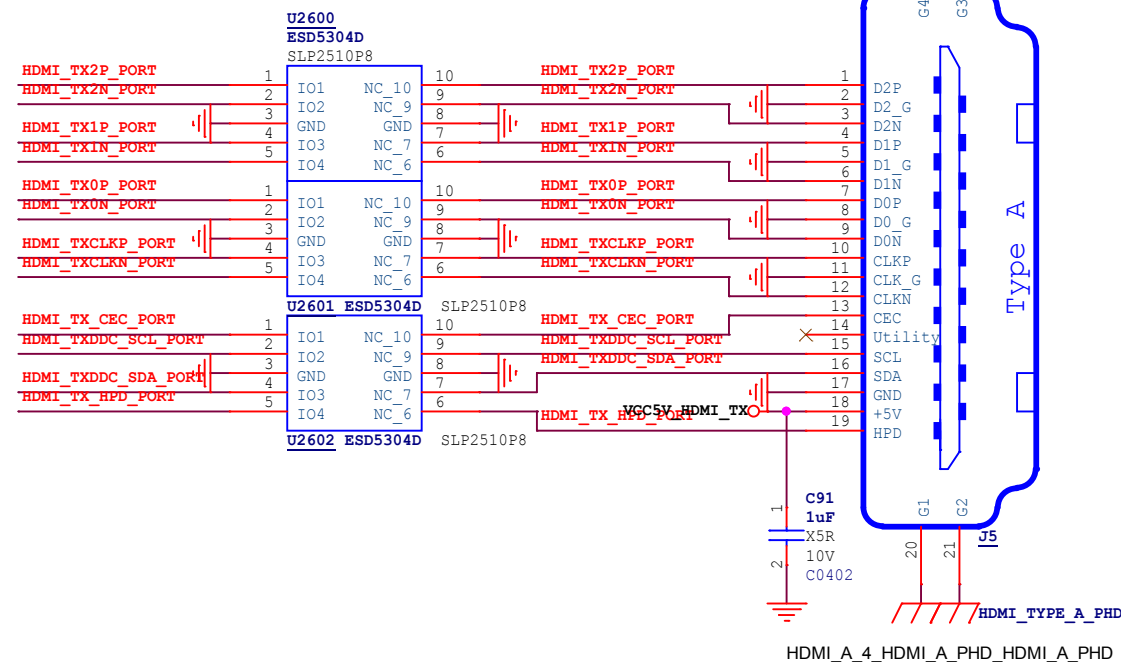
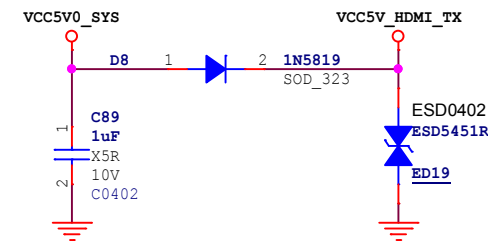
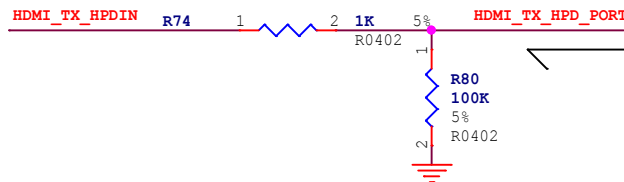
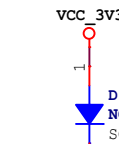
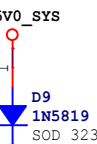
>>SDMMC0_CMD

>>SDMMC0_CLK

<<<SDMMC0_DET_L



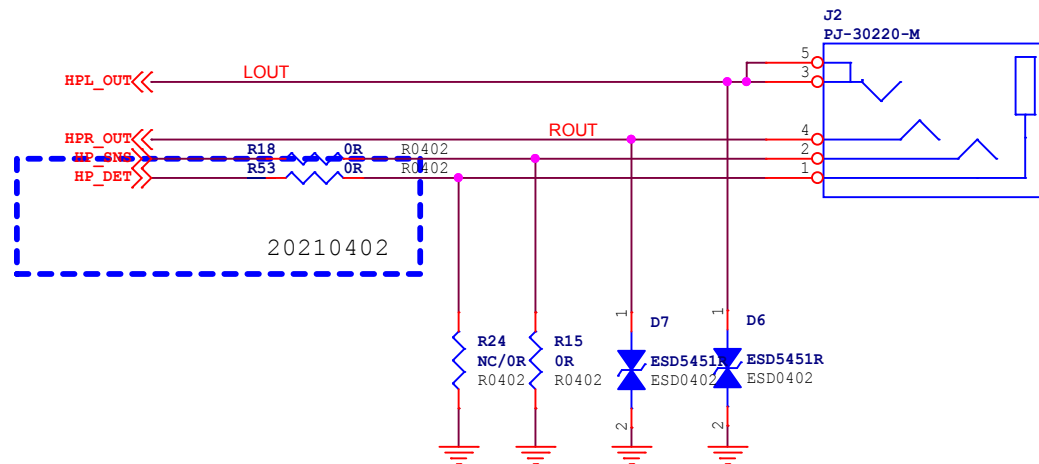
MicroSD Card

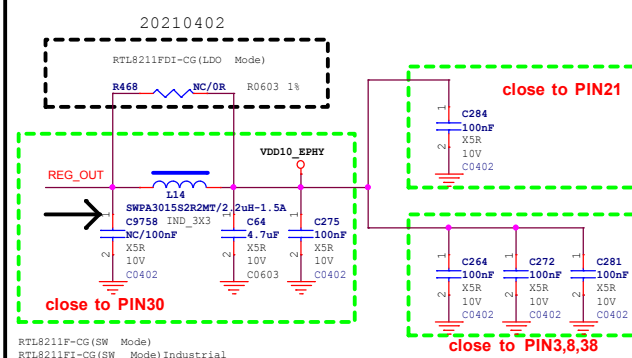
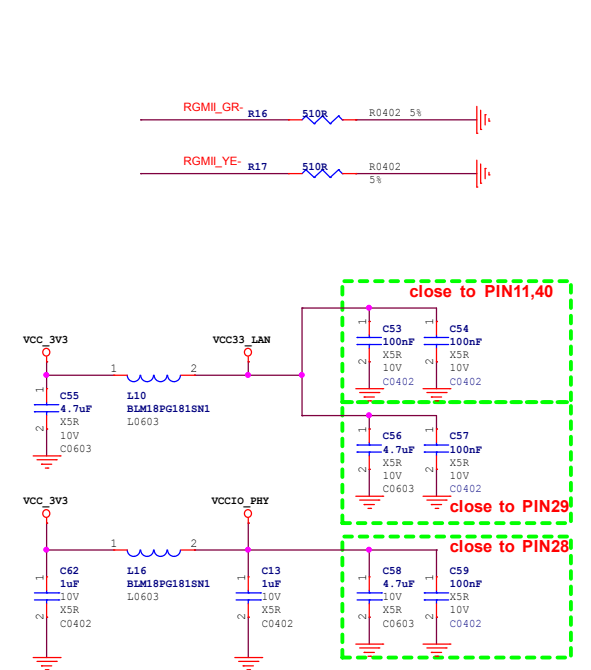
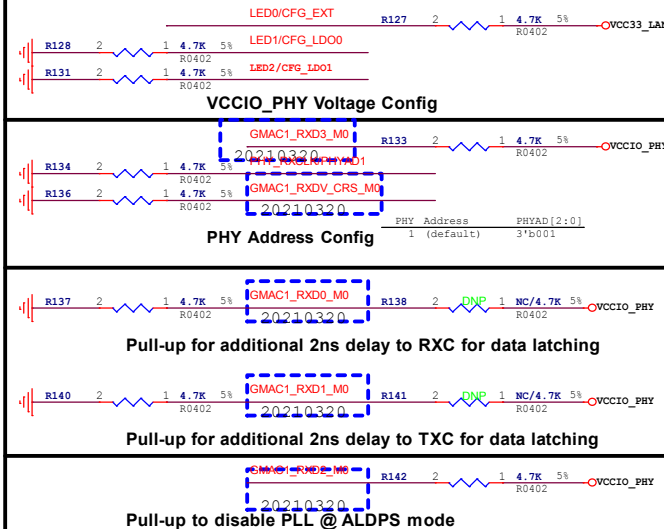
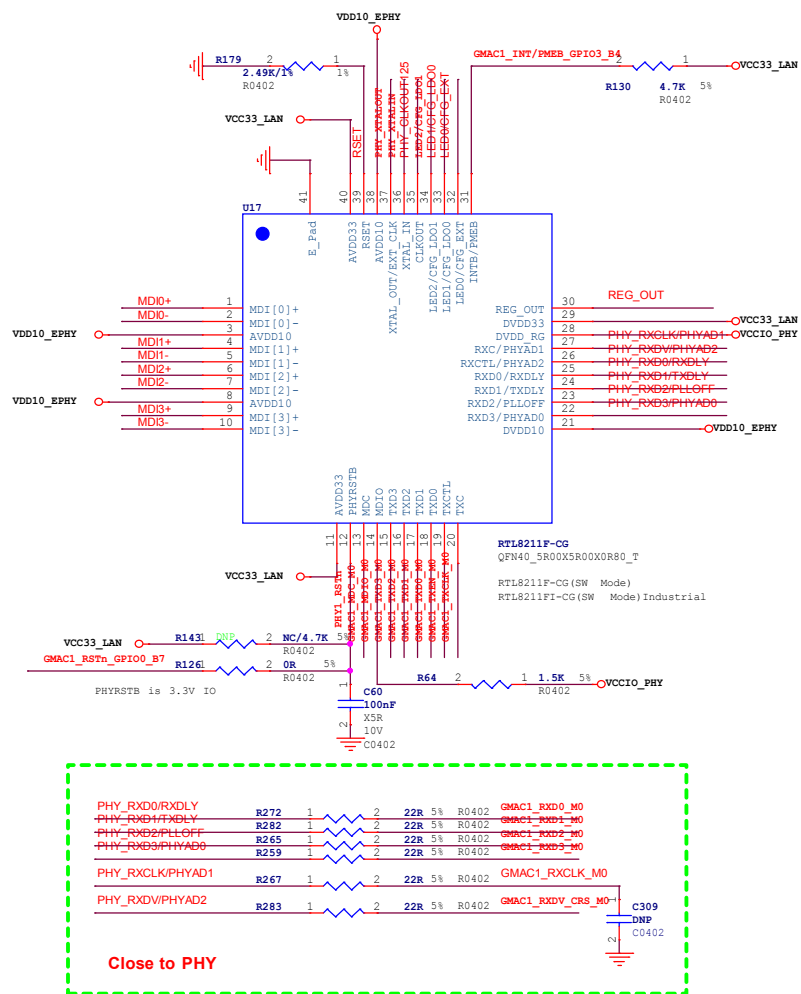
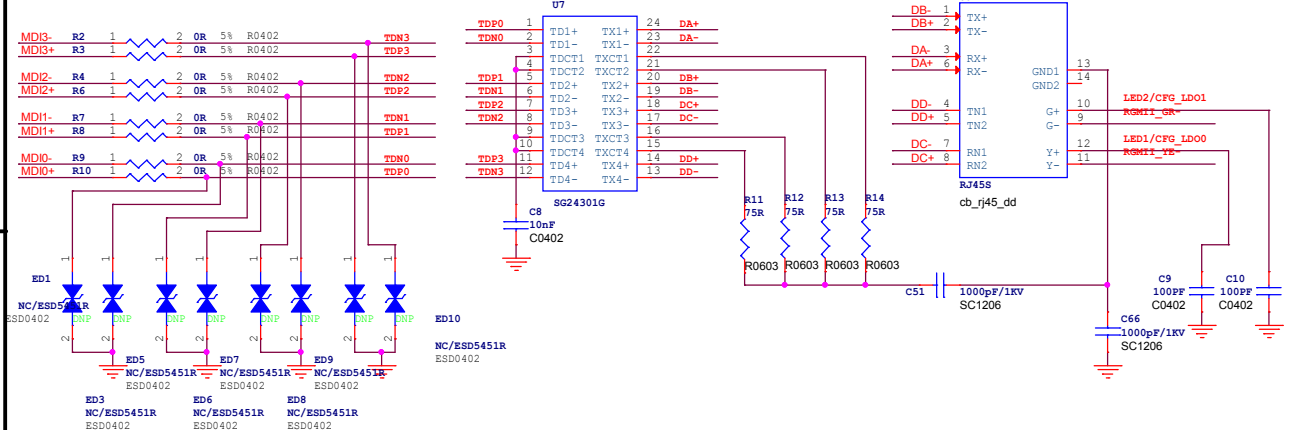
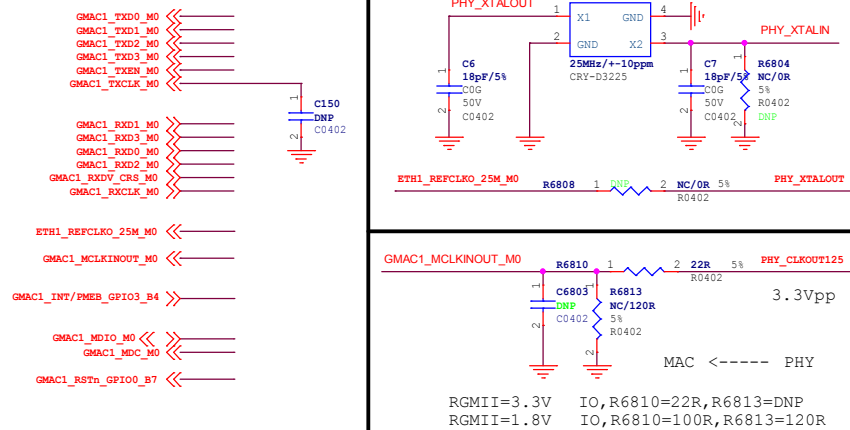


REV: V0.1

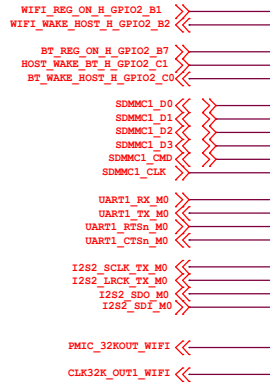
Page Num: 30

Page Total: 37

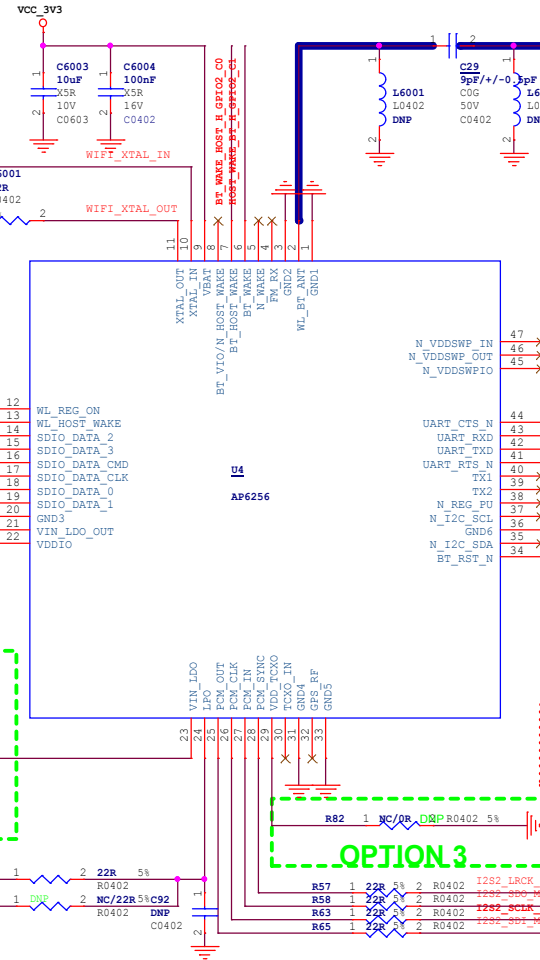
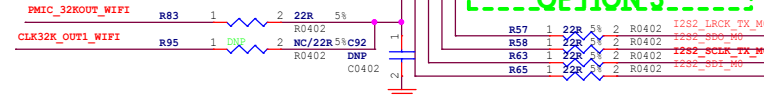
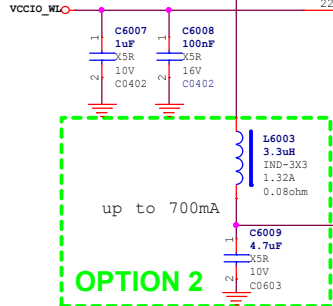
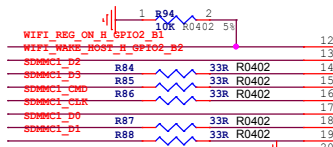
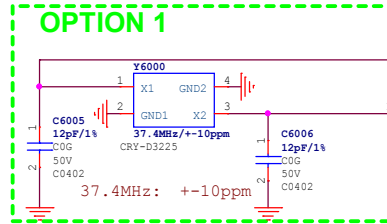




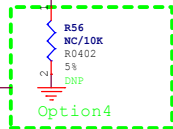
WIFI/BT Module



NOTE:
If WiFi/BT is needed to wake up SOC,
WIFI_REG_ON is needed to pull high.
So WIFI_REG_ON must be connected to
PMUIO.
WIFI_WAKE_HOST is also connected to
PMUIO



IF use BT to wake up system,
BT_RST is needed to pull high.
So BT_RST must be connected to PMUIO.
BT_WAKE_HOST is also connected to PMUIO.

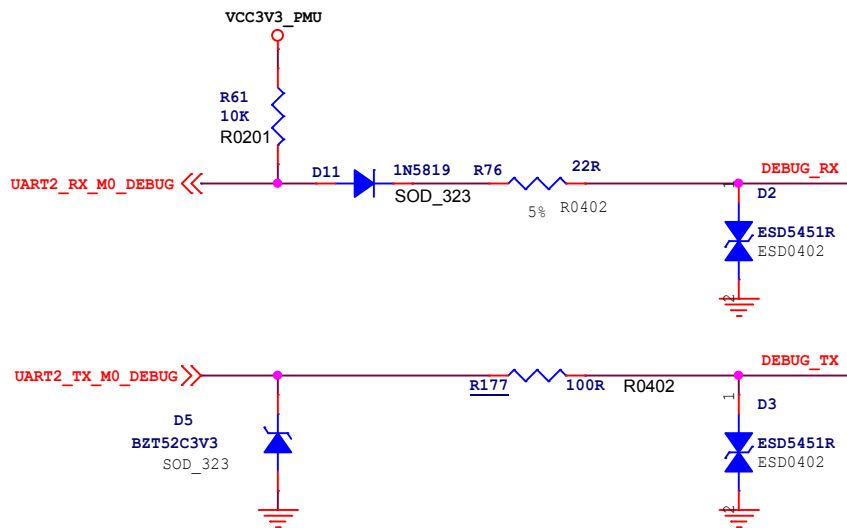
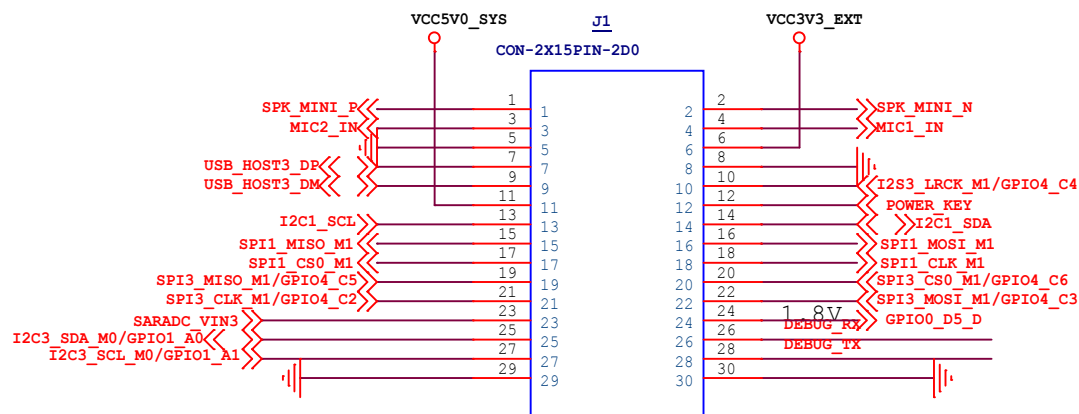


OPTION	WIFI				BT	Crystals	VCCIO_SDIO	OPTION1	OPTION2	OPTION3	OPTION4
	a	b/g/n	ac	5GHz							
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.63V	Yes	Yes	No	No
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.62-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	No
RTL8189FTV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.63V	No	No	No	Yes
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

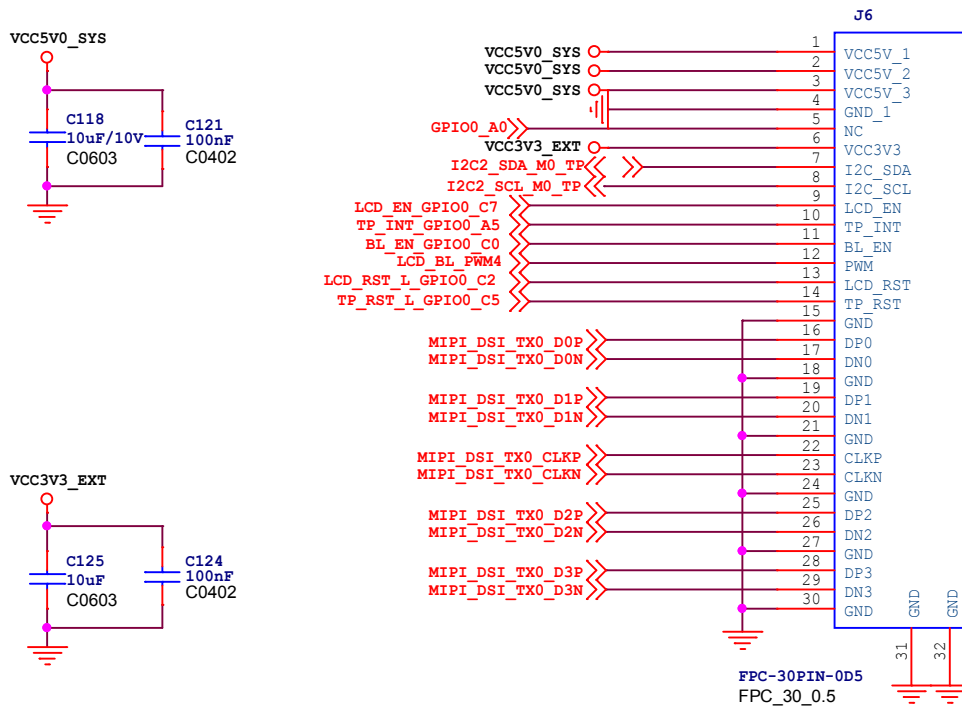
www.t-firefly.com

Title: WIFI/BT-SDIO 1T1R+UART
File: ROC-3566-PC
 Create Date: Thursday, January 07, 2021
 Modify Date: Tuesday, June 01, 2021

Page Num: 33
 Page Total: 37



MIP Display Interface



www.t-firefly.com

Title: MIPI-DSI

File: ROC-3566-PC

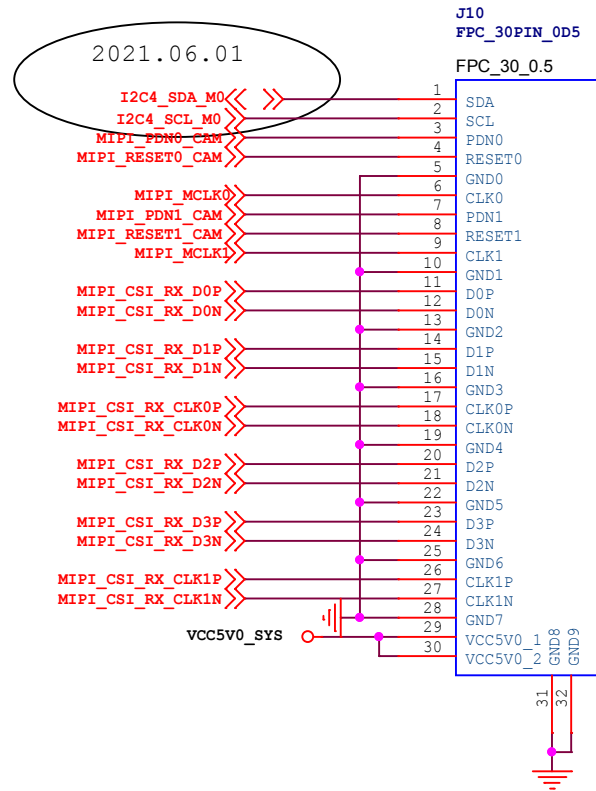
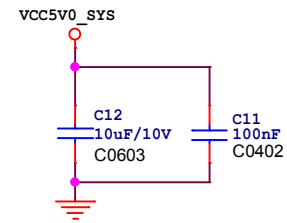
REV: V0.1

Create Date: Saturday, January 09, 2021

Page Num: 35

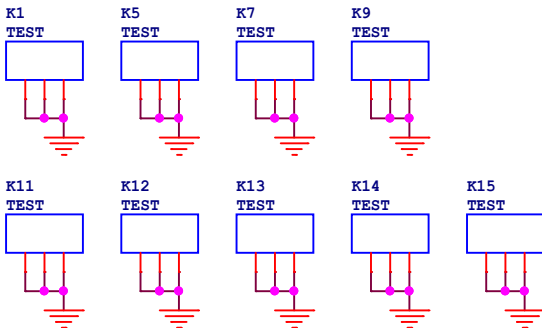
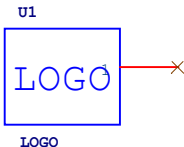
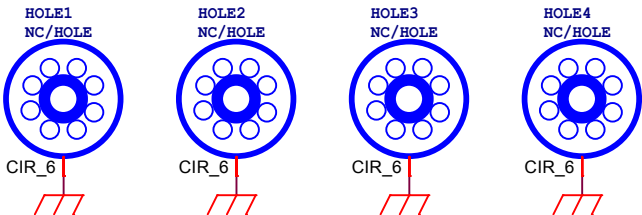
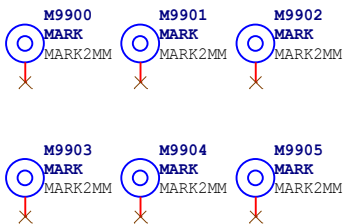
Modify Date: Tuesday, June 01, 2021

Page Total: 37



Page of Accessories

PCB Mark Point





www.t-firefly.com

Title: Mark/Hole/Heatsink	
File: ROC-3566-PC	REV: V0.1
Create Date: Wednesday, January 06, 2021	Page Num: 37
Modify Date: Tuesday, June 01, 2021	Page Total: 37