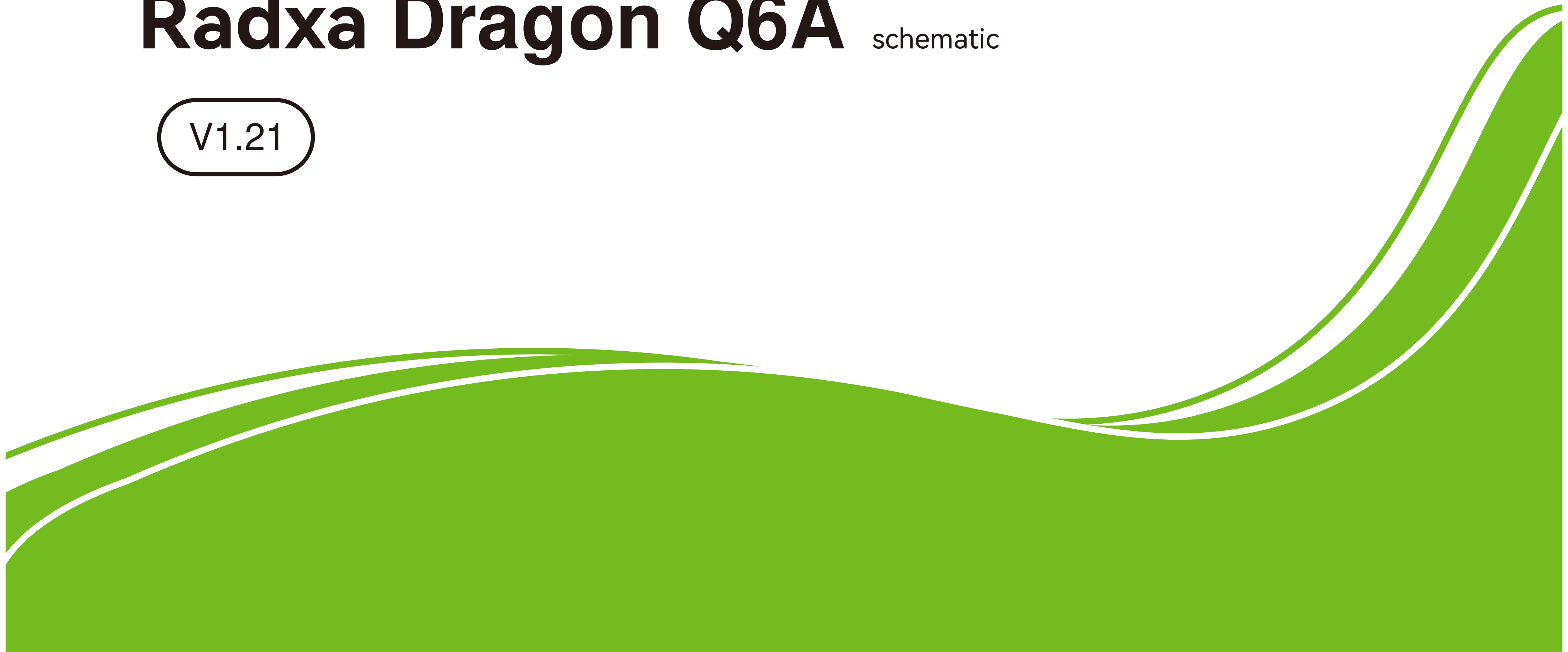
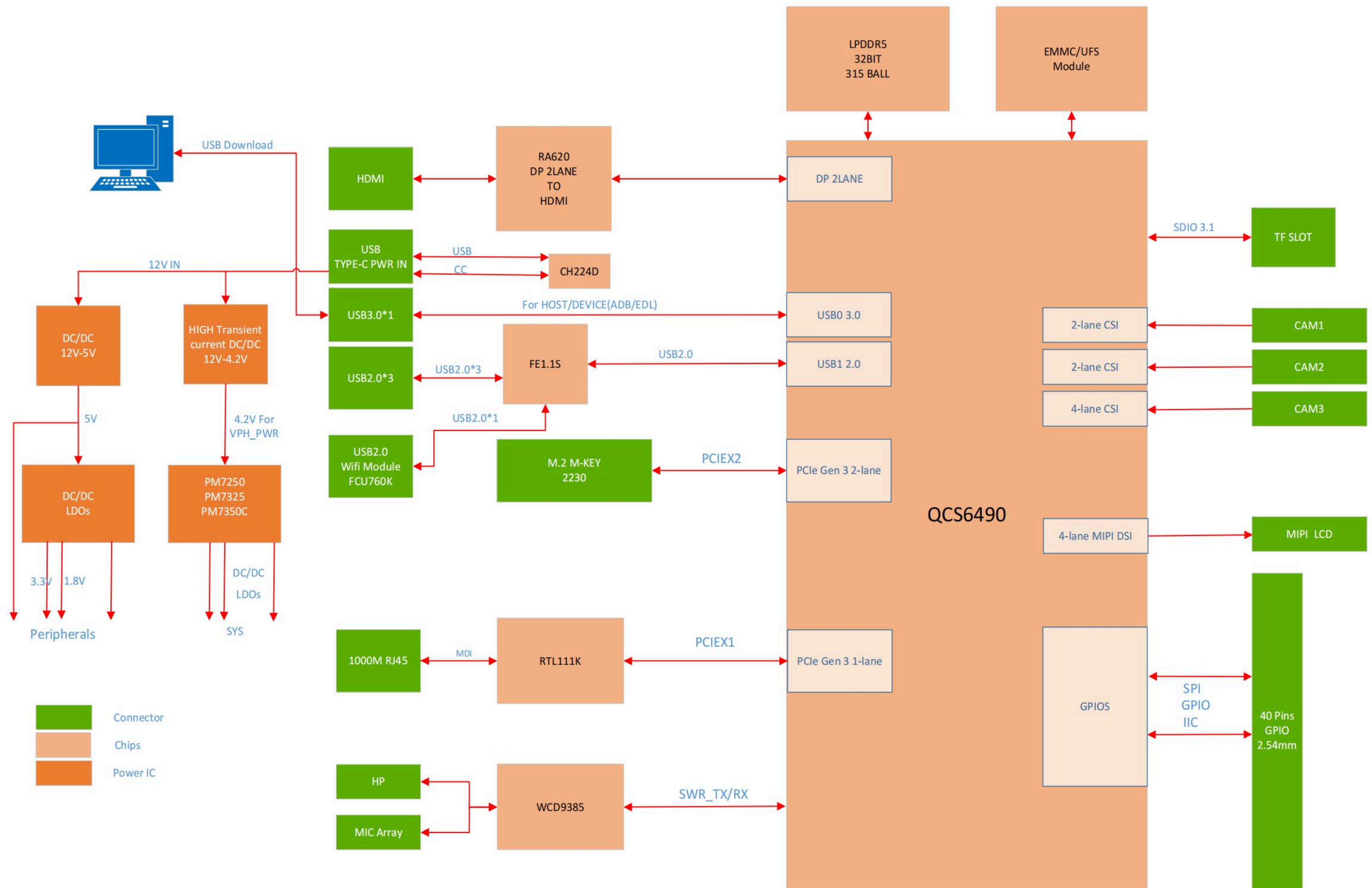




Radxa Dragon Q6A schematic

V1.21





QCM6490 CONTROL

CAD Note:
Single 50Ω
sensitive signals, away from noise sources/high speed signals..

CAD Note:
Add a placeholder cap to RESIN_N pin of QCM6490
meeting its max transition (rise/fall) time of 200 ns

CAD Note:
Place the resistors connected to the REXT pins near to MSM
and route away from noisy siganls.

Ensure there is an external 10k pull-up resistor
placeholder (DNI) on the SDC2_CMD for SD card.

single 45
Ω

diff 90
Ω

AUX

lane_0_1 DP0
lane_0_0 DP1
diff 85
Ω

lane_1_1 RX
lane_1_0 TX
diff 85
Ω

CAD Note:
PLACE SPMI resistors close to QCM
Route the SPMI signals in Daisy Chain/Start routing
from MSM to the PMICS to avoid stubs.

diff 90
Ω

Place away from PMIC and heat-sources

Place near to the QCM about 1cm and put into the shielding



QCM6490 GPIO

Note:
Only one protocol can be selected in one QUP engine at a time.
For example, simultaneous UART and I2C functionality are no longer supported.

Note: GPIO_45 (LD20-22882-18 Rev.C, QRD7325)
--EUD EN net is QCOM internal used only.
--GPIO_45 should not be hold as Level High during the Boot phase of SM7325.

I/O	UART	I2C/I3C	SPI
QUP_L0	CTS	SDA	MISO
QUP_L1	RFR	SCL	MOSI
QUP_L2 SCLK	Tx	-	
QUP_L3 CS_0	Rx	-	
QUP_L4 CS_1	-	-	
QUP_L5 CS_2	-	-	
QUP_L6 CS_3	-	-	

It is recommended to use GPIO 38 (internal pull up) for NFC_EN.
Add 12 K pull up to VDD_PX3. In case if other GPIO with internal pull down is re-purposed for NFC_EN, then this signal should have 2.7 K pull up to VDD_PX3. In such case software changes are required.

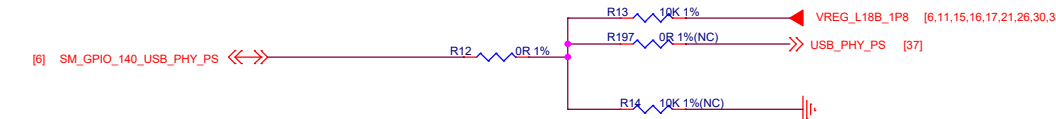
FORCE_USB_BOOT

Note:
The polarity of FORCE USB BOOT(GPIO 82) as active high or active low is set by FORCED_USB_BOOT_POLARITY_SEL(GPIO 139).

FORCED_USB_BOOT_POLARITY_SEL=L, FORCE_USB_BOOT=H;
FORCED_USB_BOOT_POLARITY_SEL=H, FORCE_USB_BOOT=L;



Typc C / Micro USB

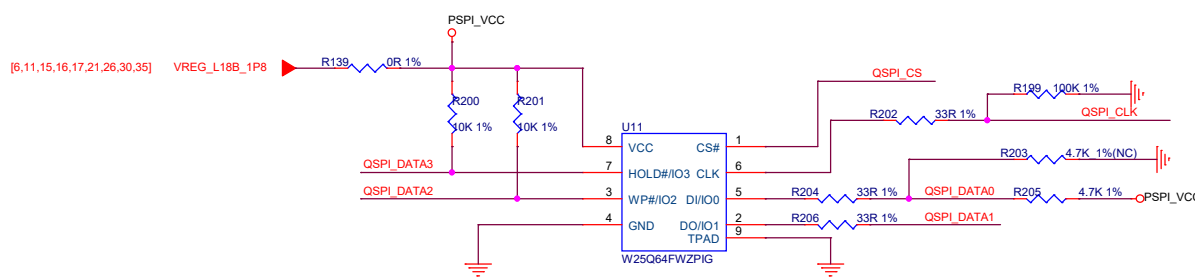


Type-C: R710 = NC, R707 = 0 ohm, R709 = NC
Micro USB: (USB SS-H_HS-L_SEL connect to USB port ID pin) R710 = 7.32K ohm within 1% accuracy, R707 = NC, R709 = 0 ohm

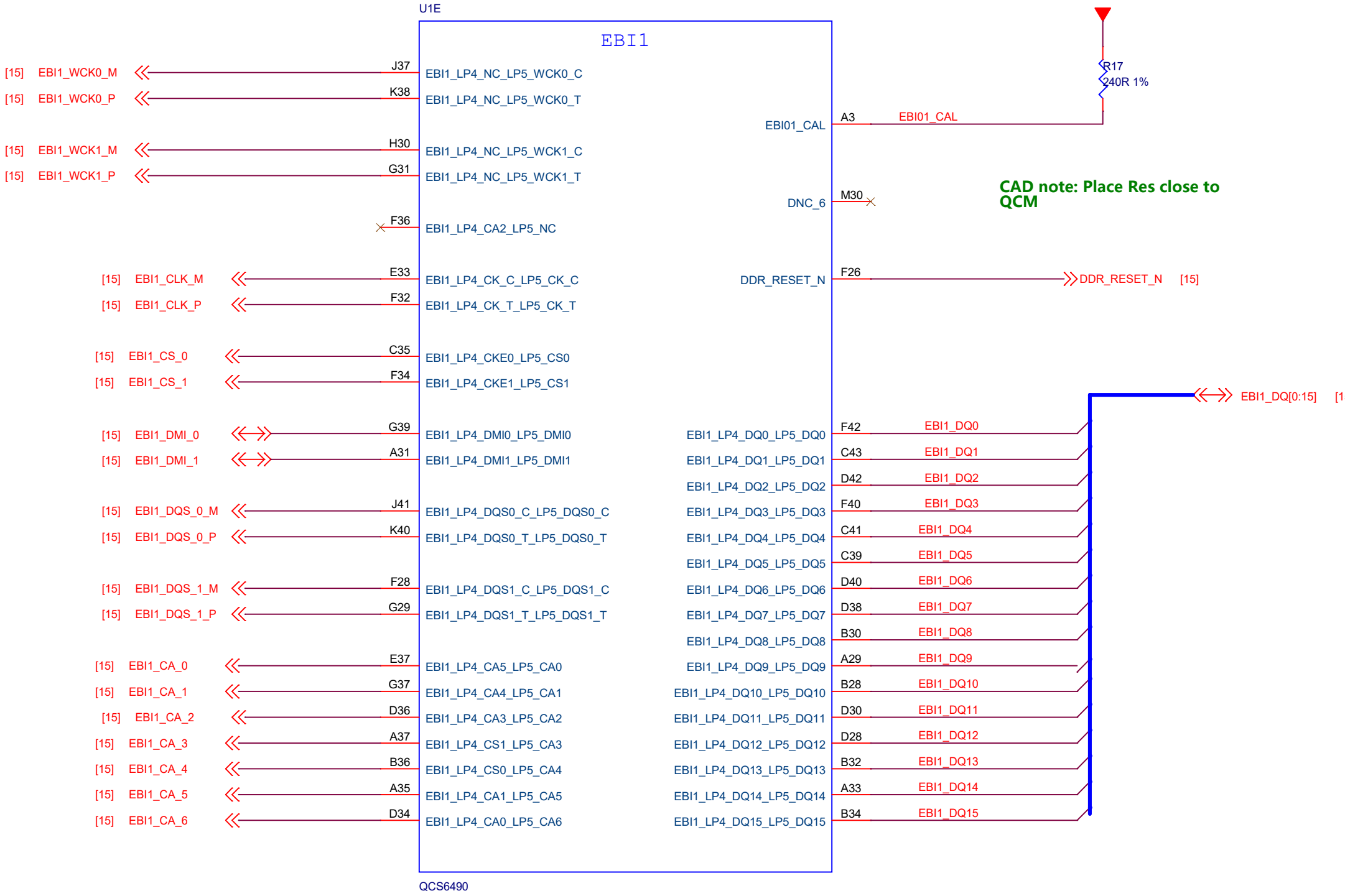
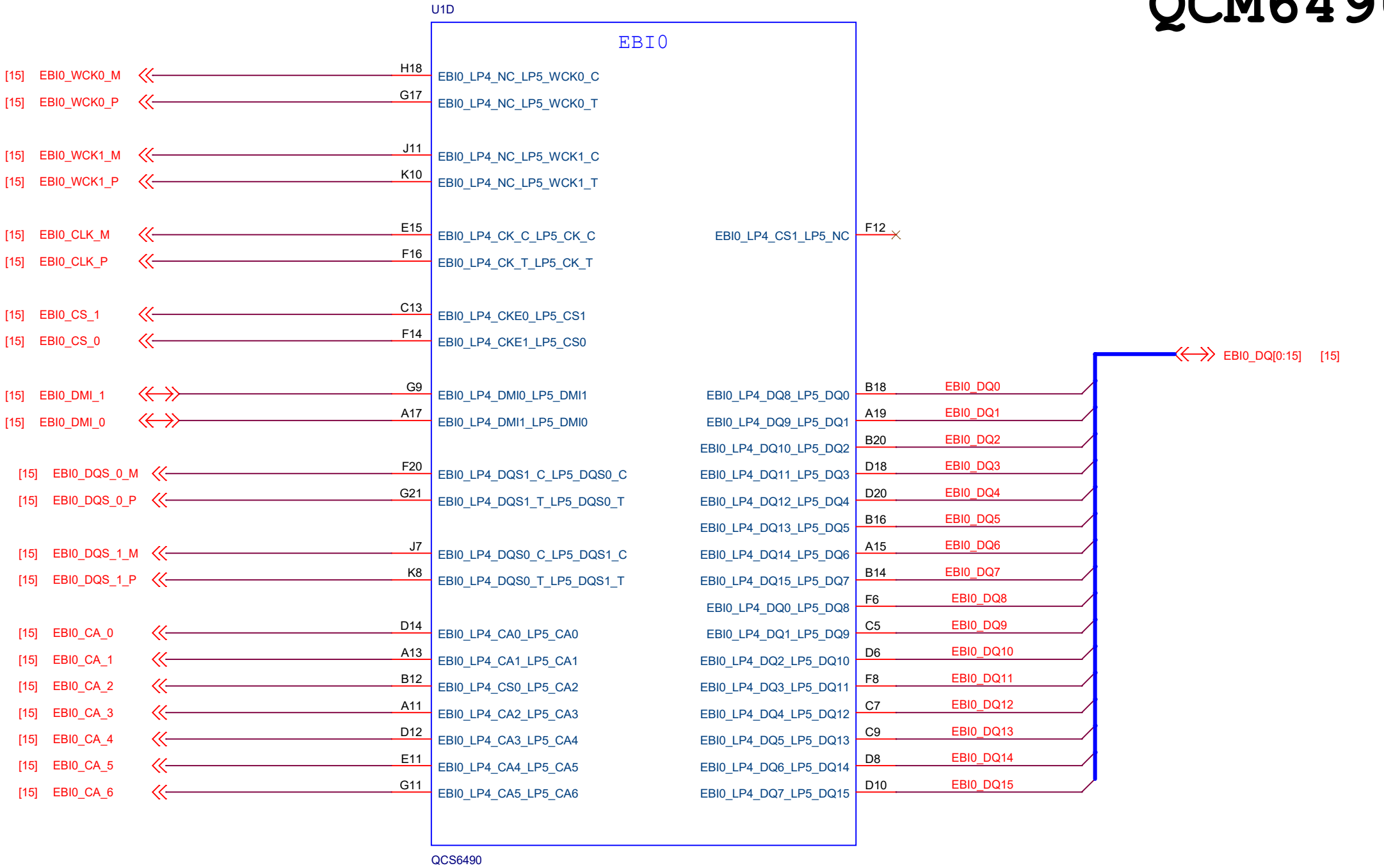
I2C BUS pull-ups

Note:
All I2C bus pull-up resistors are placed on other board, unless they are used on the SOM.

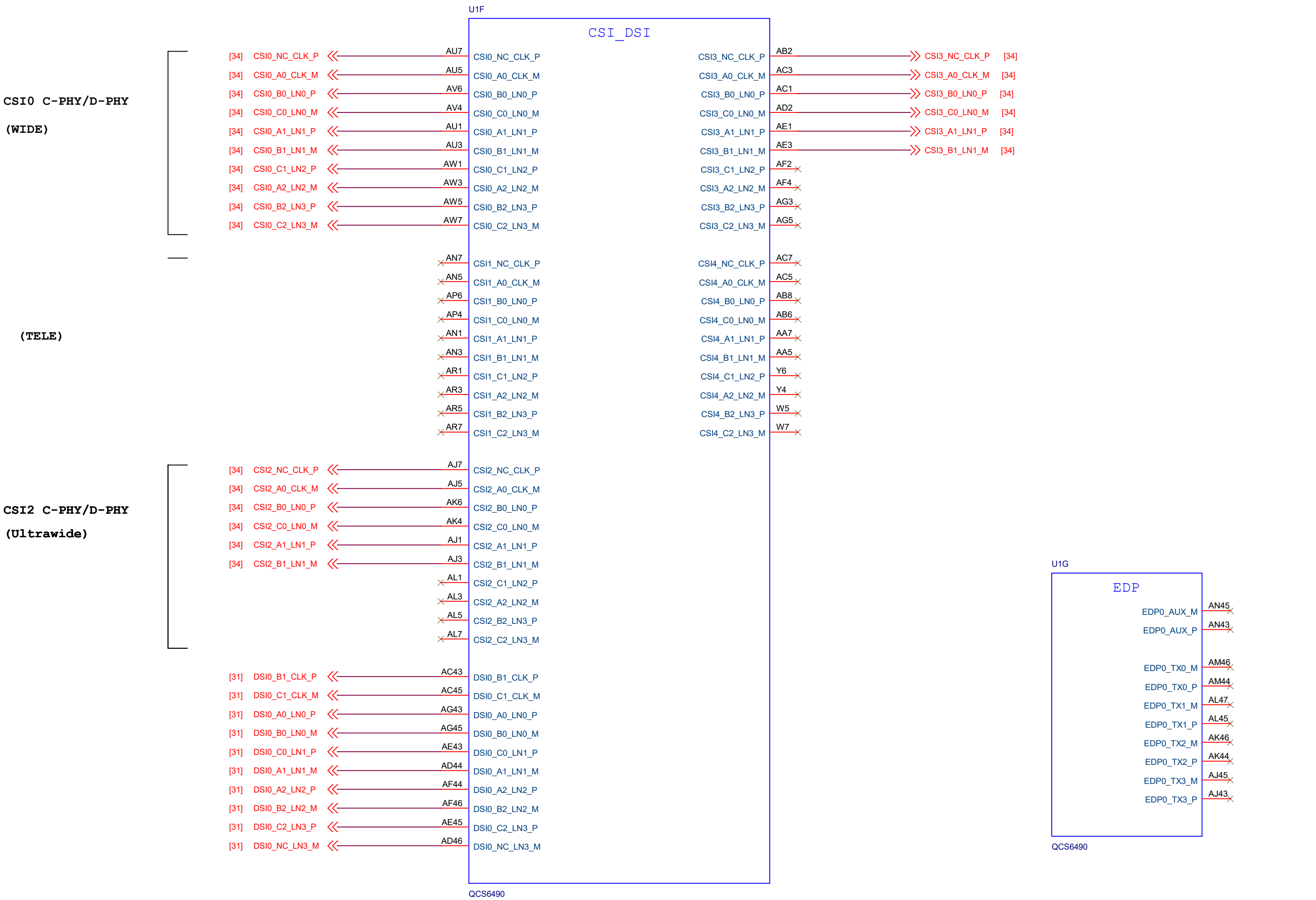
QSPI FLASH FOR BOOT



radxa



QCM6490 MIPI-CSI/DSI



ISP:
three IFEs and two IFE lite
up to five cameras may operate concurrently, up to eight sensors
IFE lite ISP supports 5 MP at 30 fps

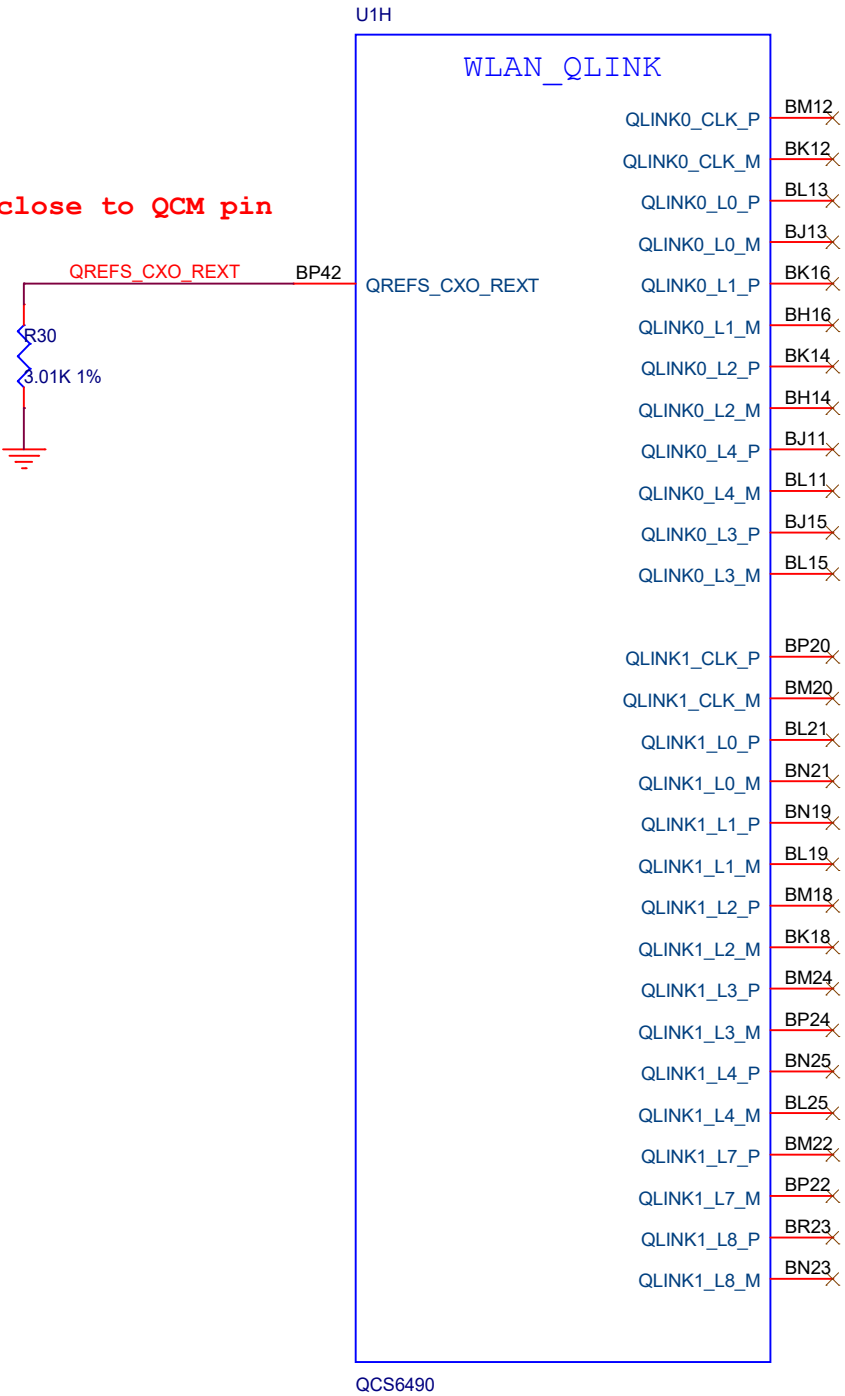
36 + 22 MP at 30 fps / 3 x 22 MP 30 fps ZSL
five concurrent MIPI CSI configurable in 4 + 4 + 4+ 4 + 4 configuration

CSI lane mapping when a 4-lane interface is configured as 2-lane plus 1-lane interfaces:
- DCLK => DCLK_A
- DLN0 => DLN0_A
- DLN1 => DLN1_A
- DLN2 => DLN0_B
- DLN3 => DCLK_B

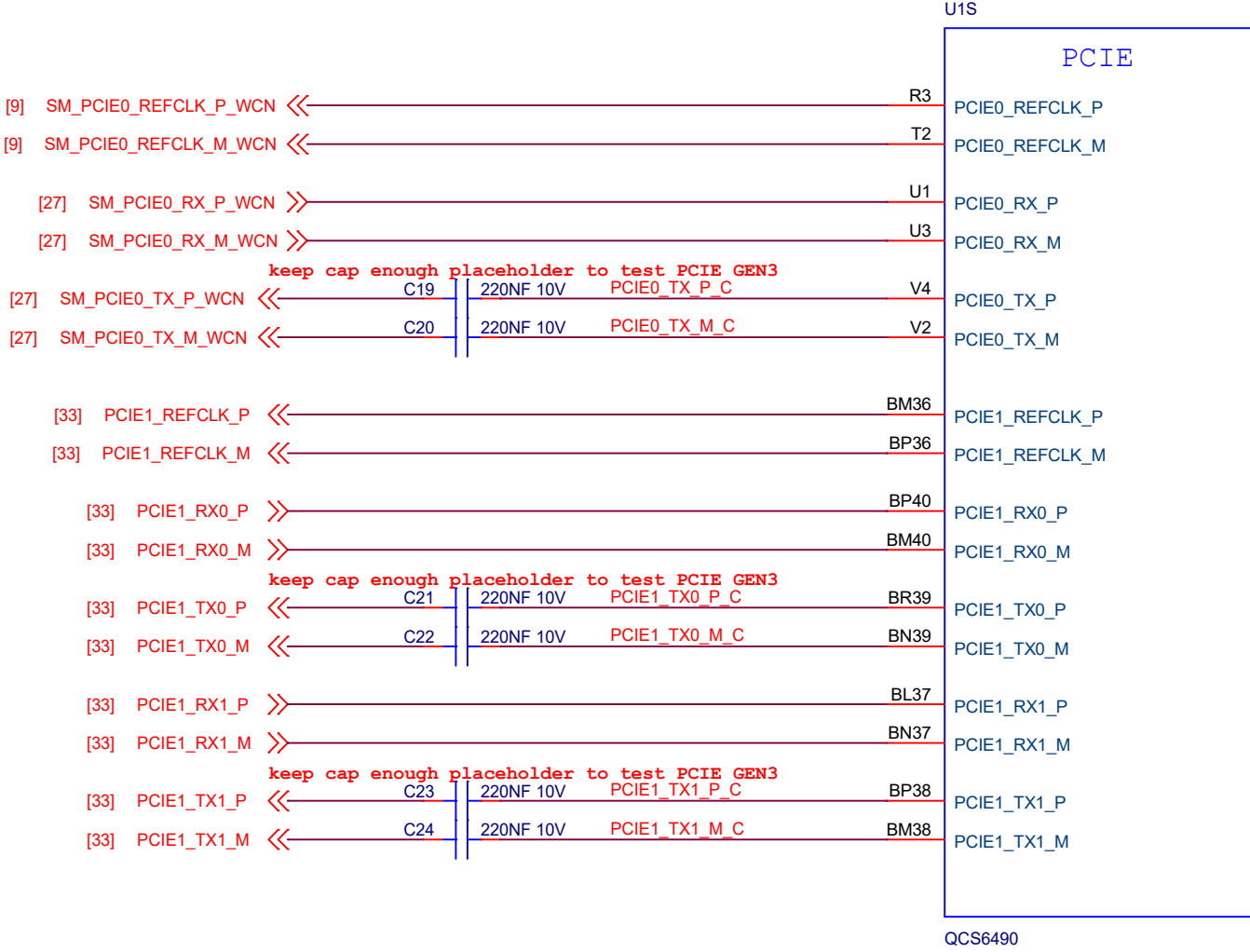
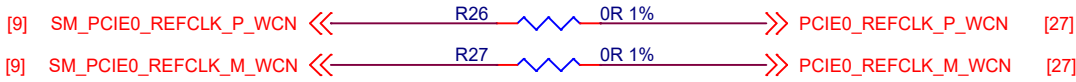
CSI lane mapping when a 4-lane interface is configured as 1-lane plus 1-lane interfaces:
- DCLK => DCLK_A
- DLN0 => DLN0_A
- DLN2 => DLN0_B
- DLN3 => DCLK_B

QCM6490 RF/PCIE

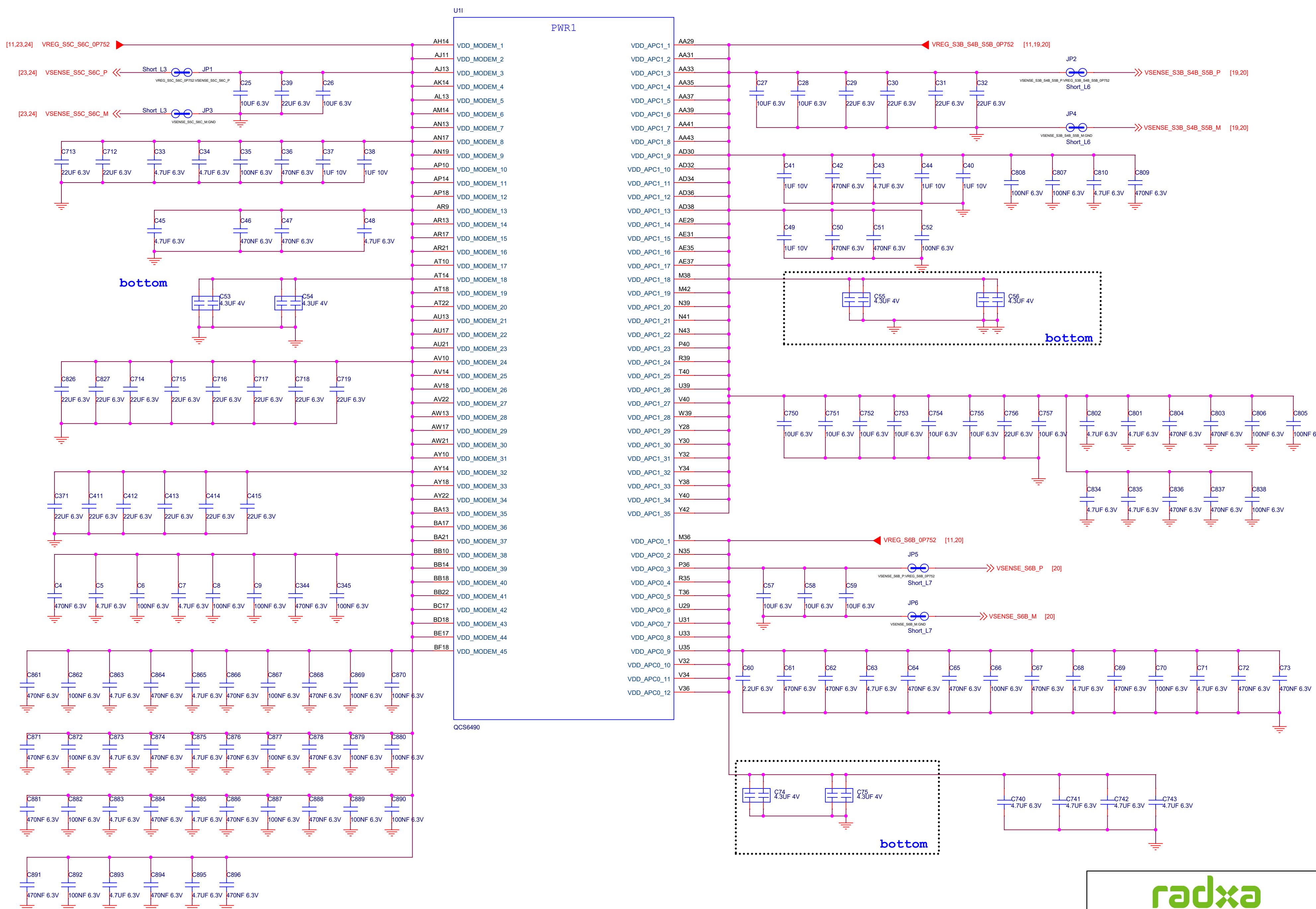
CAD note: Place res close to QCM pin



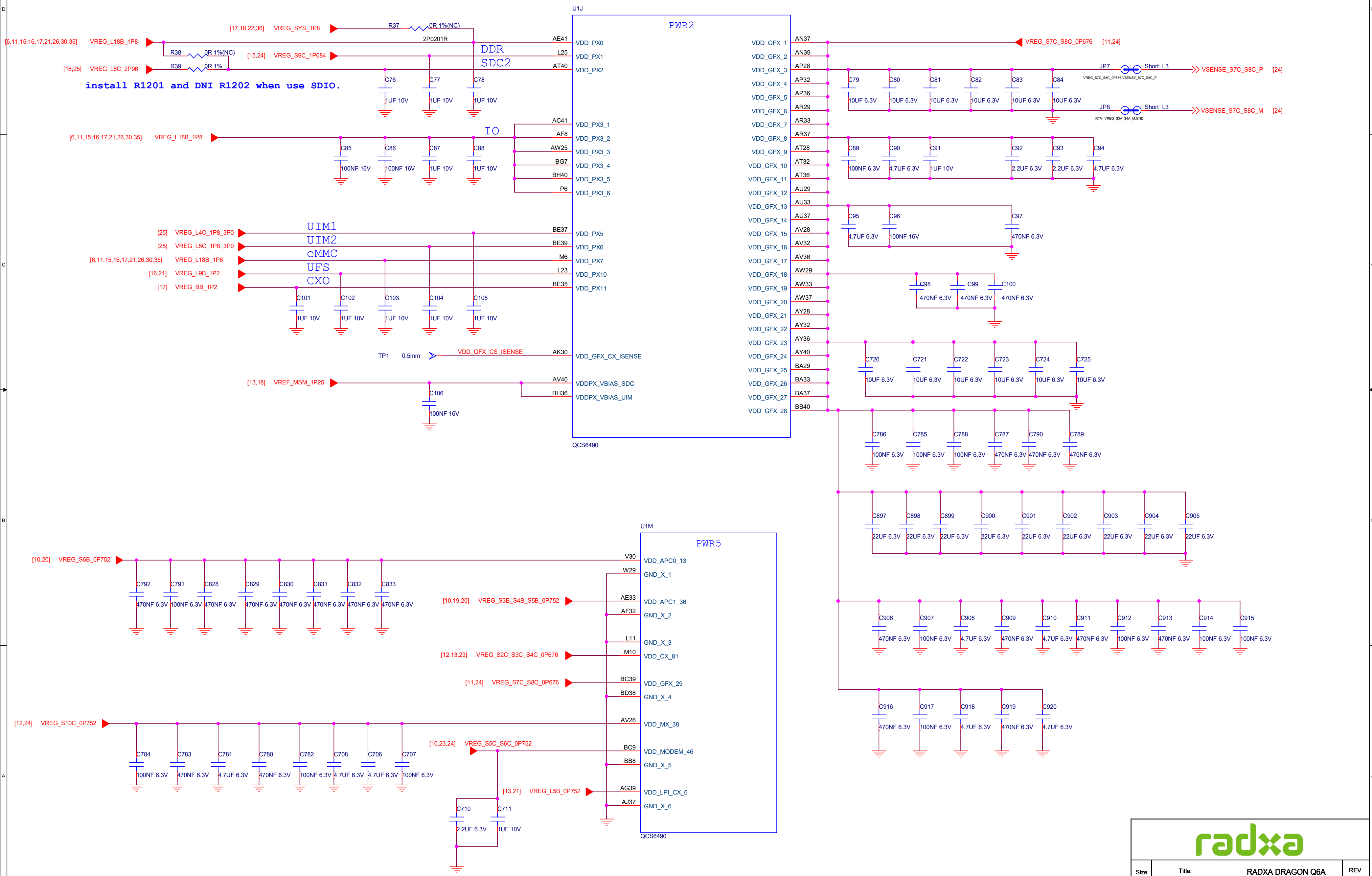
	QLINK0	QLINK1
QCS6490	GNSS (SDR735G)	DNC
QCM6490	SDR735	SMR526



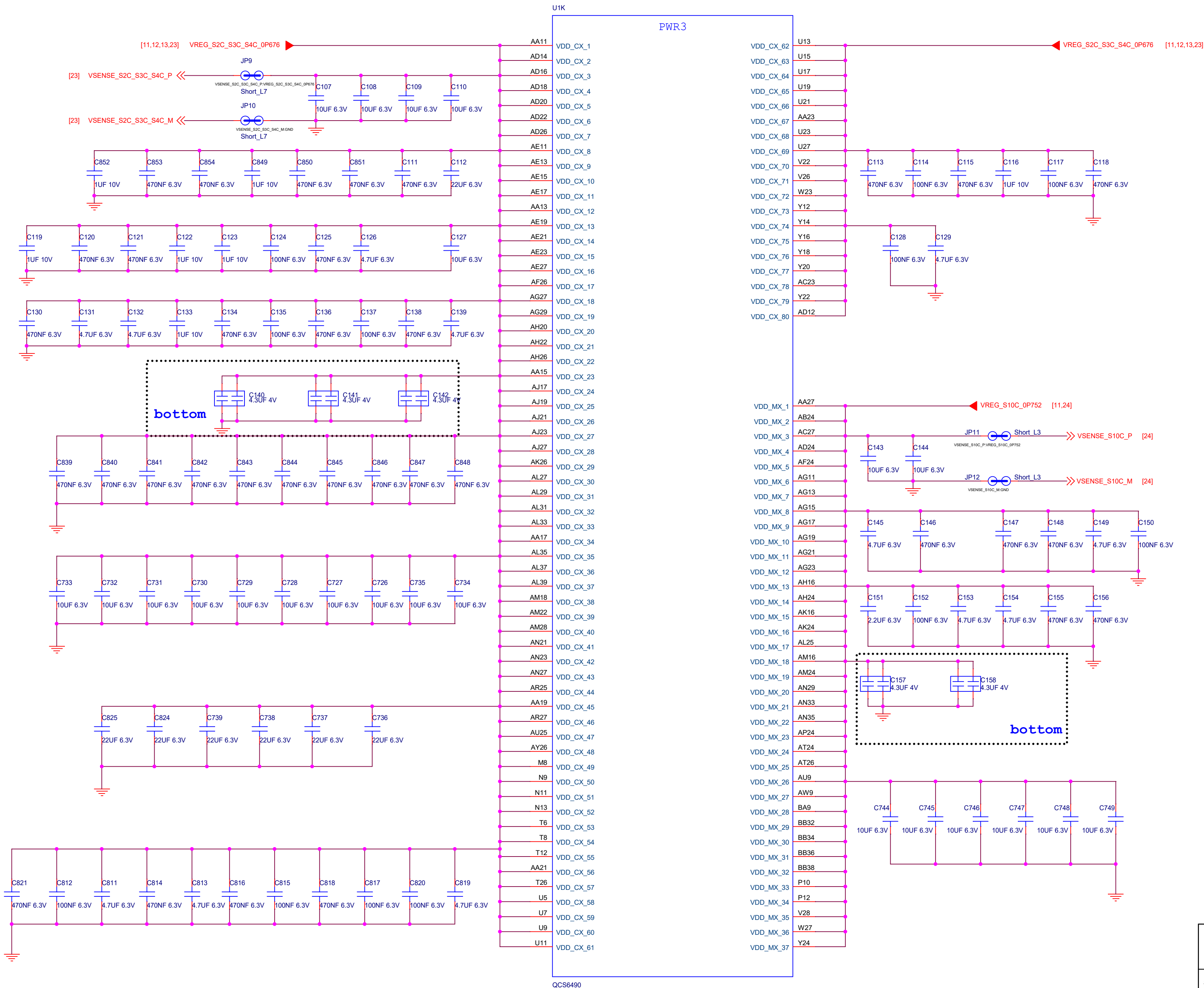
QCM6490 PWR1



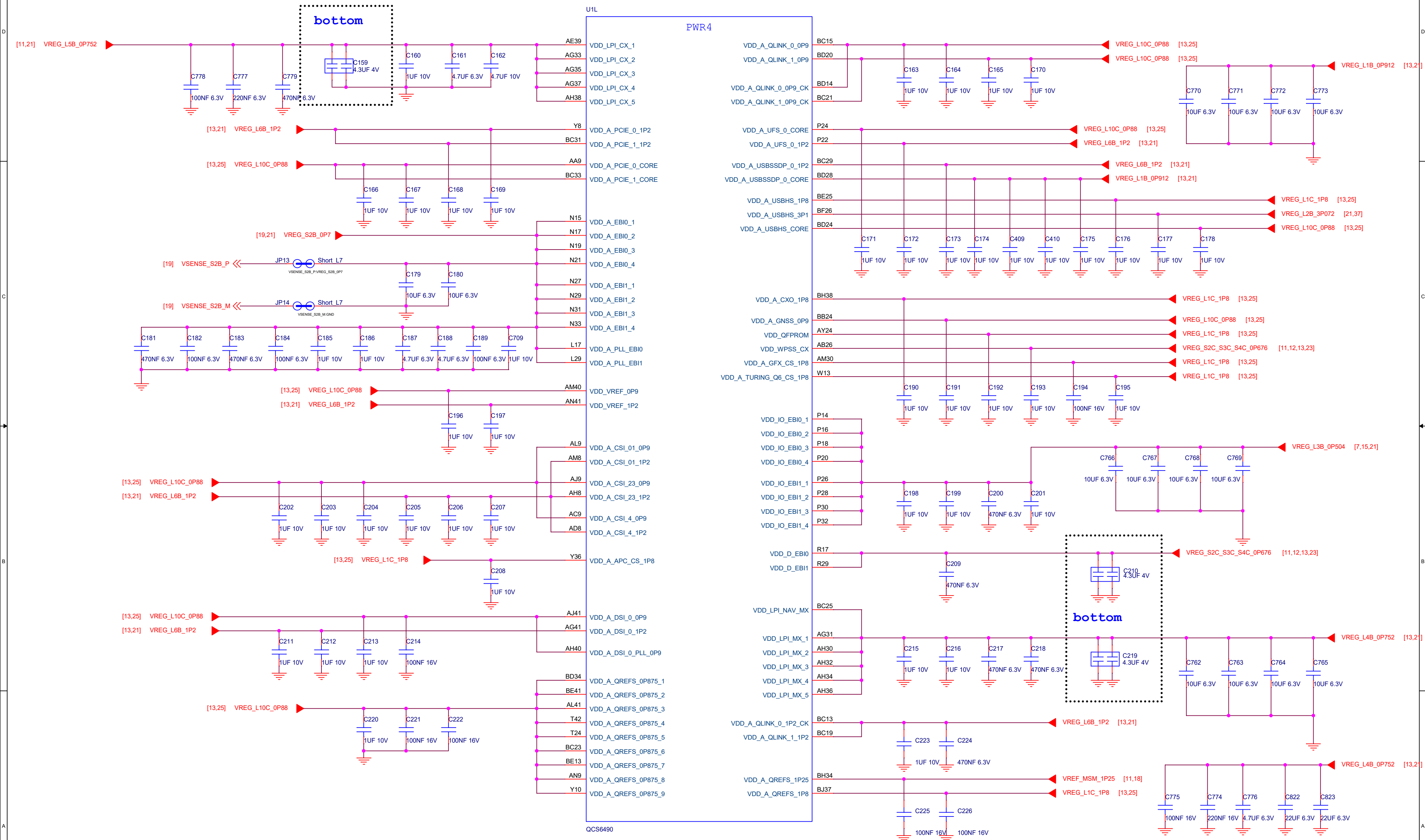
QCM6490 PWR2



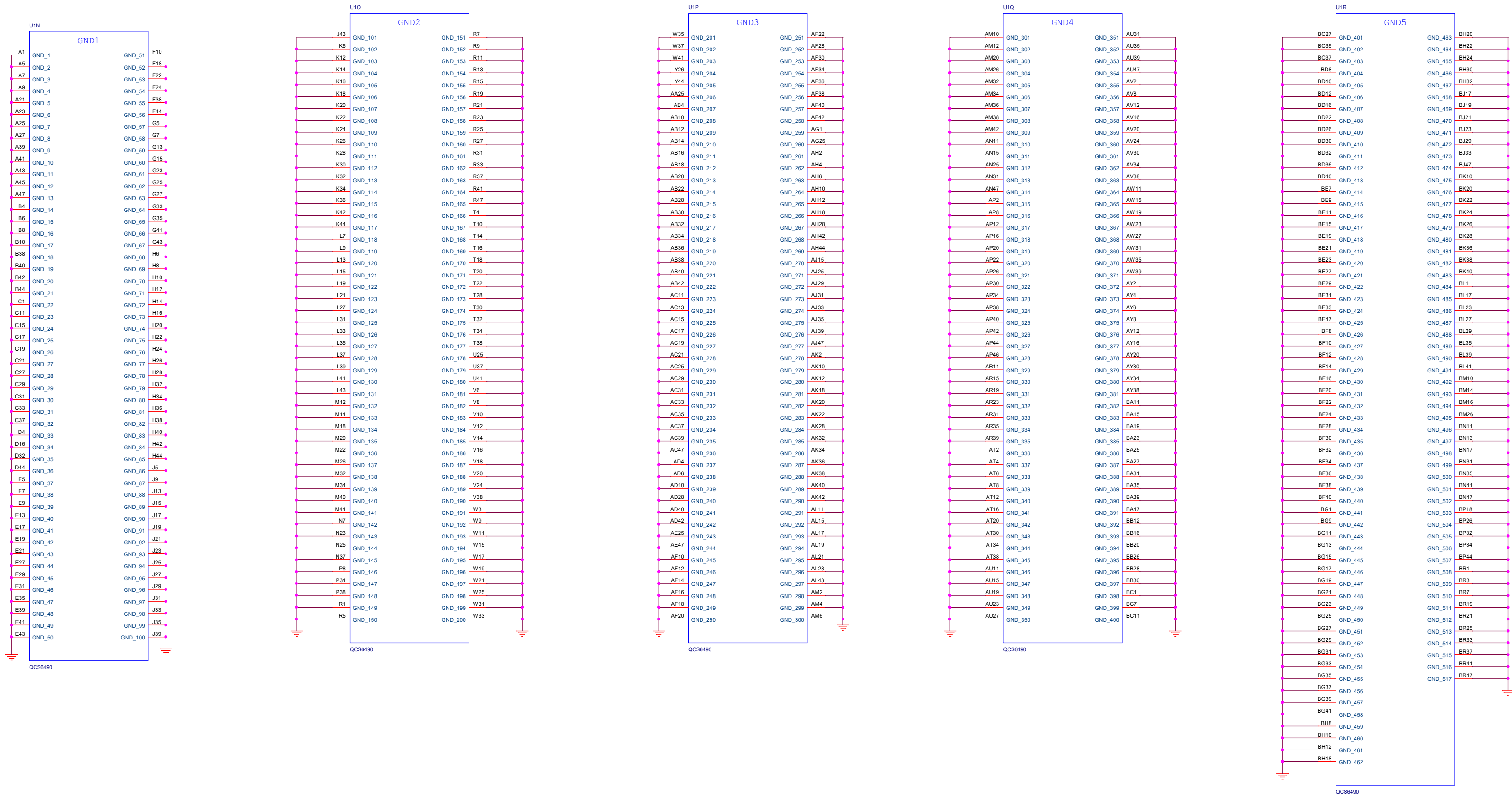
QCM6490 PWR3



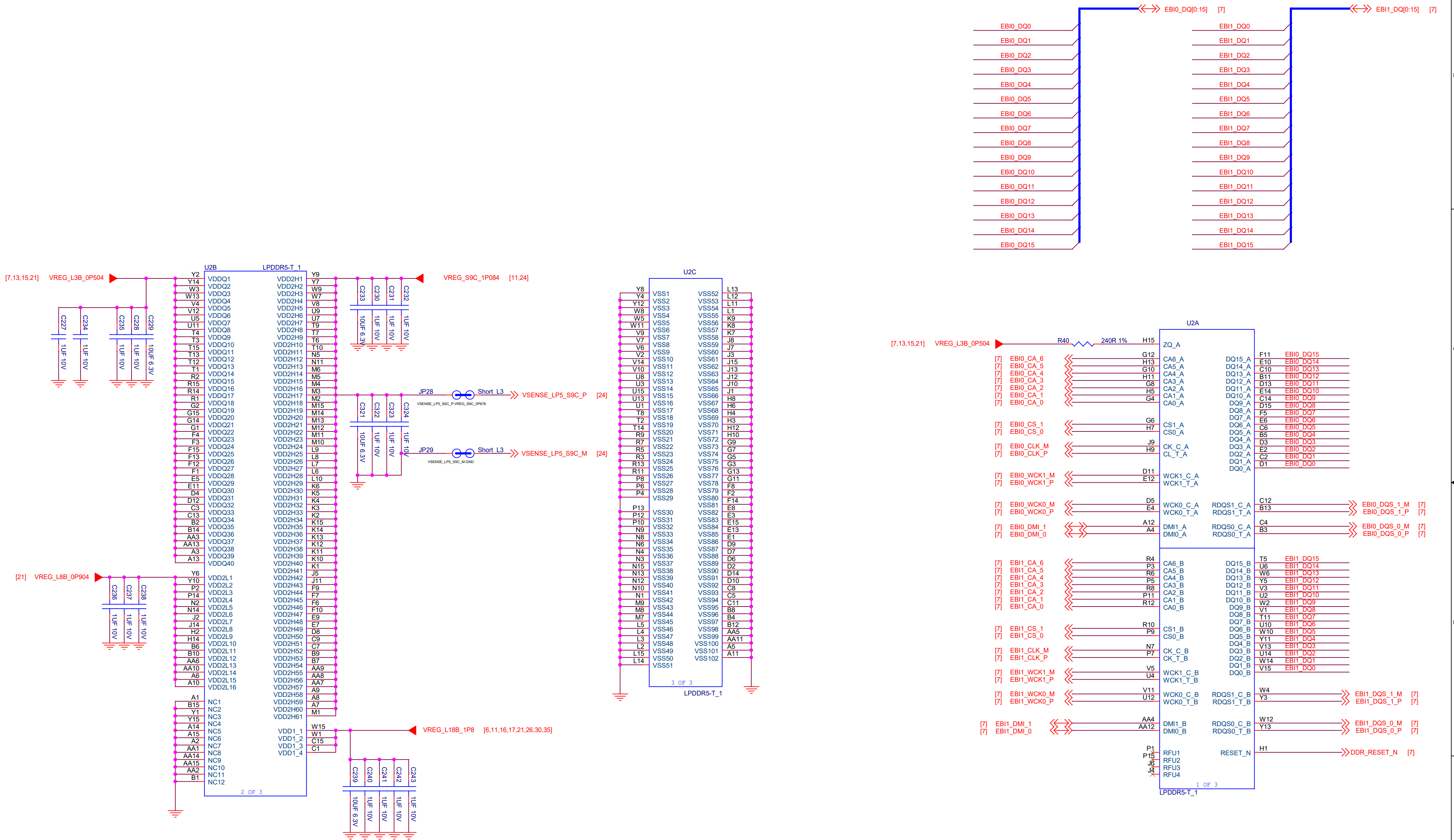
QCM6490 PWR4



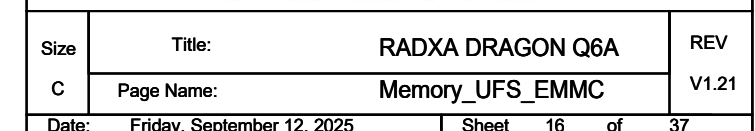
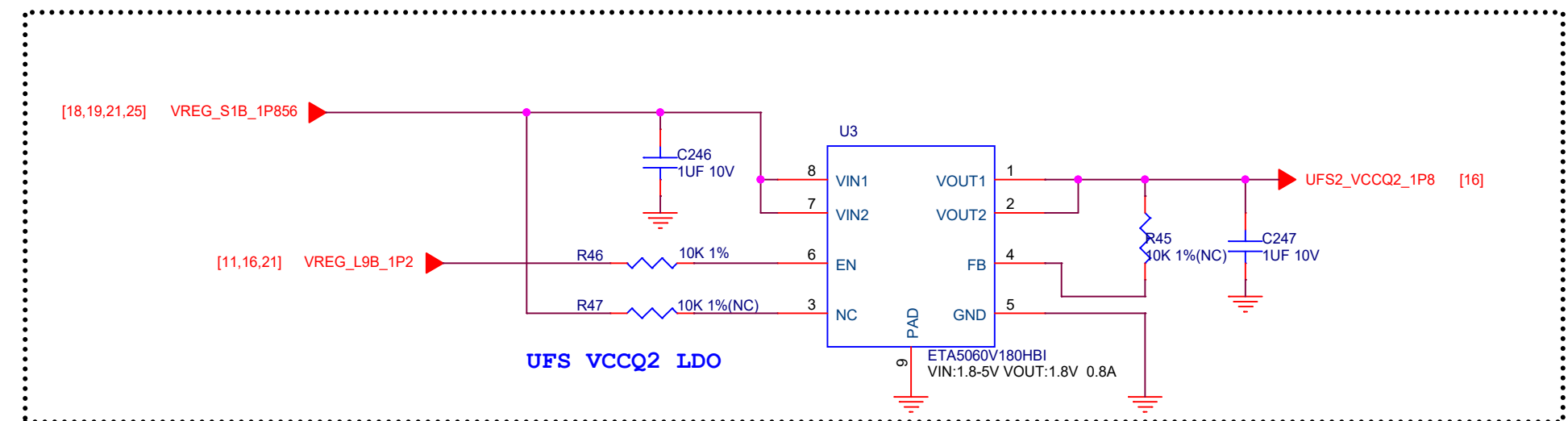
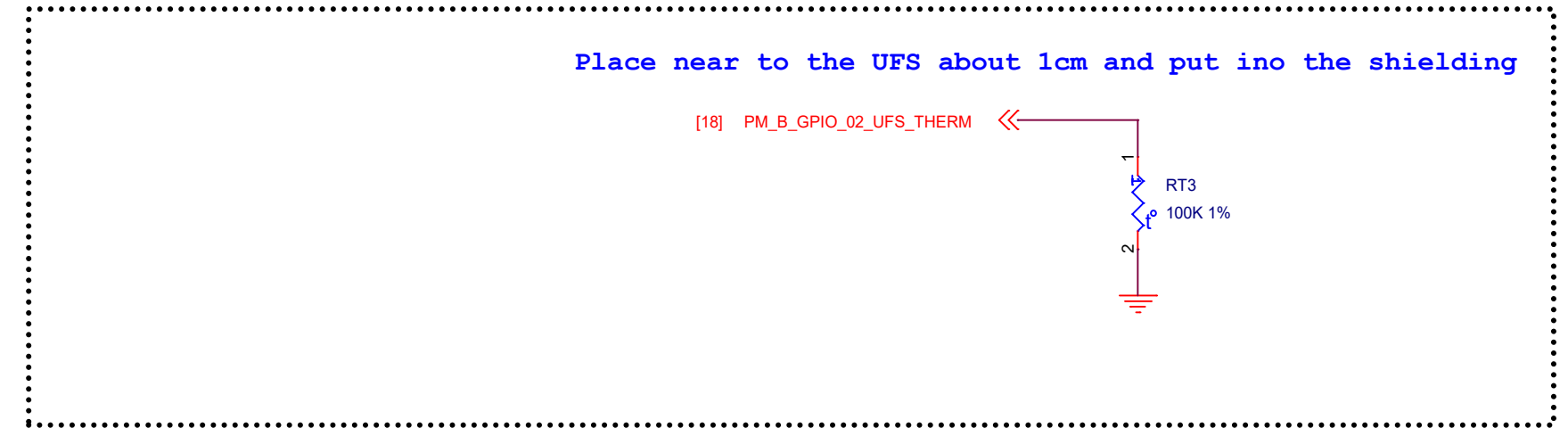
QCM6490 GND



LPDDR5

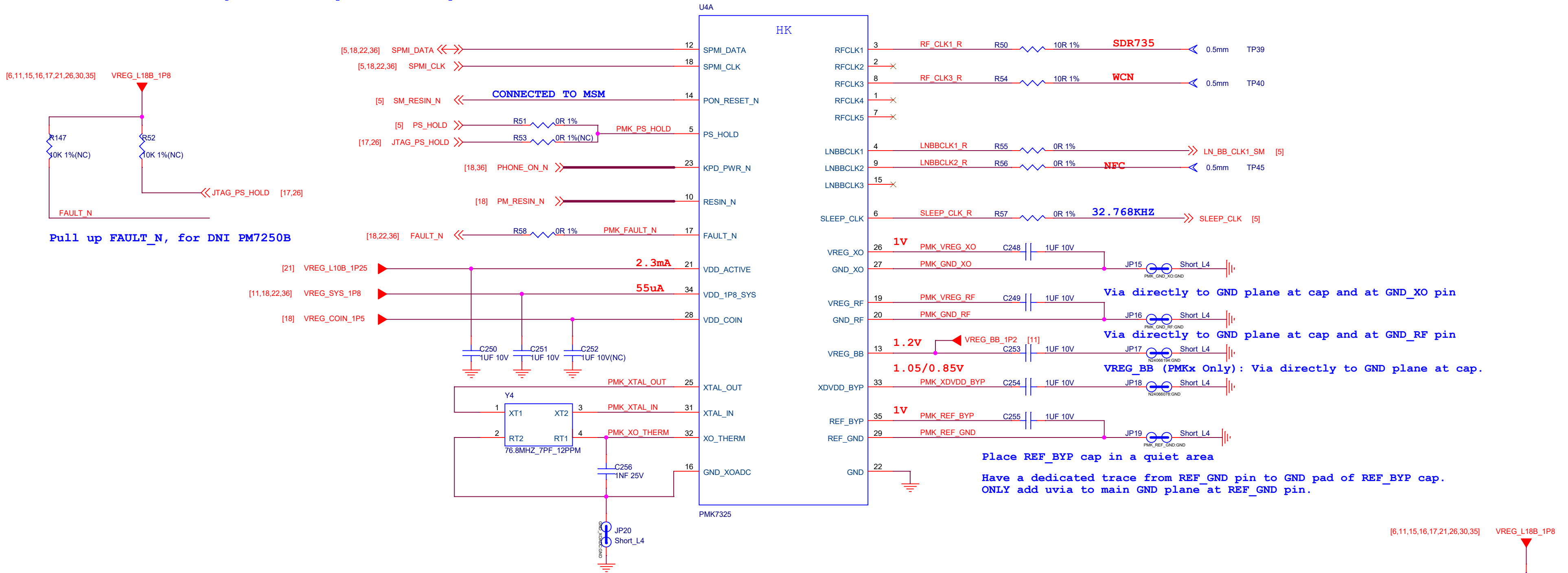


eMMC ufs



Note:
SPMI_CLK & SPMI_DATA should be routed away from noisy traces
Route signals as a diff pair as much as possible

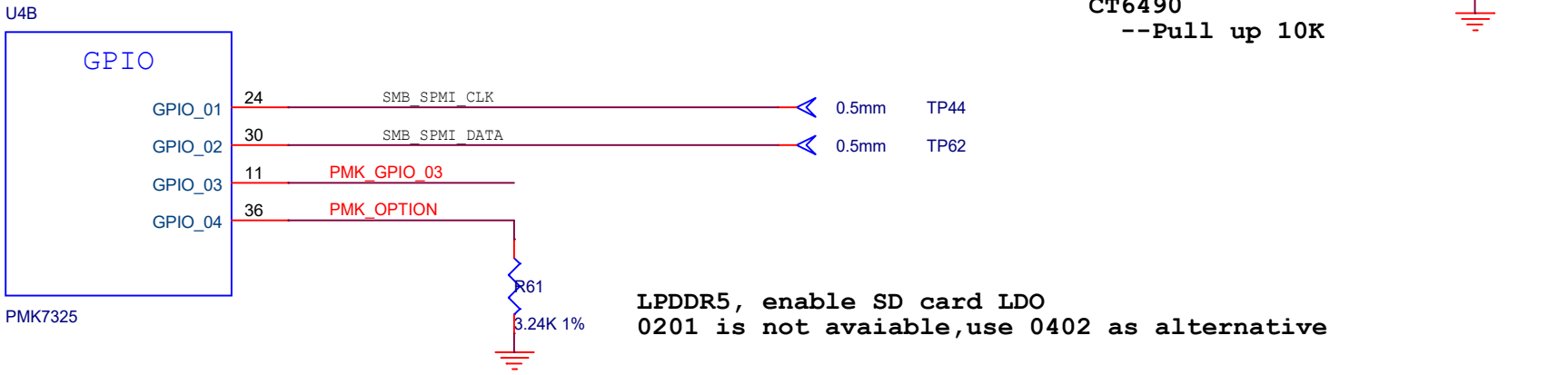
PMK7325



Layout Note: XTAL
No trace shall be present in at-least two immediate layers below XTAL.
Route XTAL IN/OUT trace with length between 3mm and 10mm

PMK_OPTION	Configuration
3.24k	LPDDR5, SD card LDO enabled
10.2k	LPDDR5, Skip SD card LDO enable
-	- (Reserved)
113k	LPDDR4x, SD card LDO enabled
147k	LPDDR4x, Skip SD card LDO enable
-	- (Reserved)

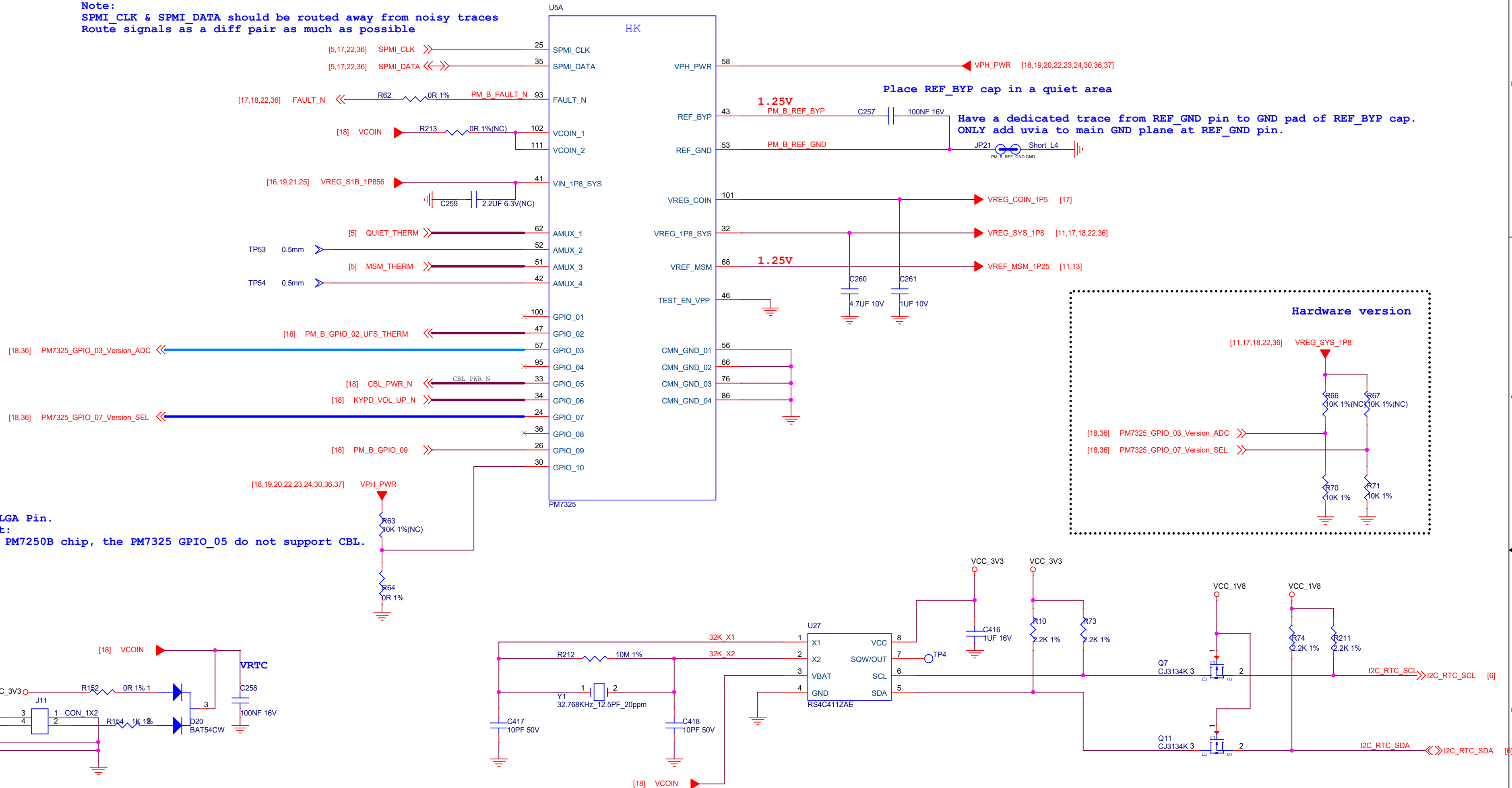
Note:
SD card boot implies the voltages for SD card will be enabled during power on sequence.
No SD card boot implies the voltages for SD card will be skipped during power on sequence.



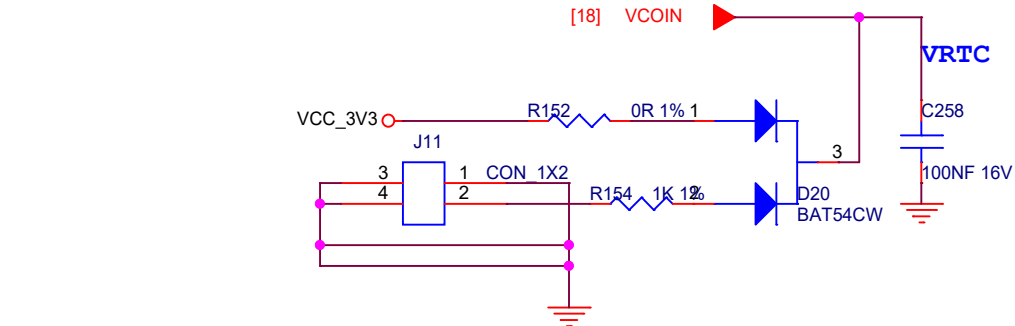
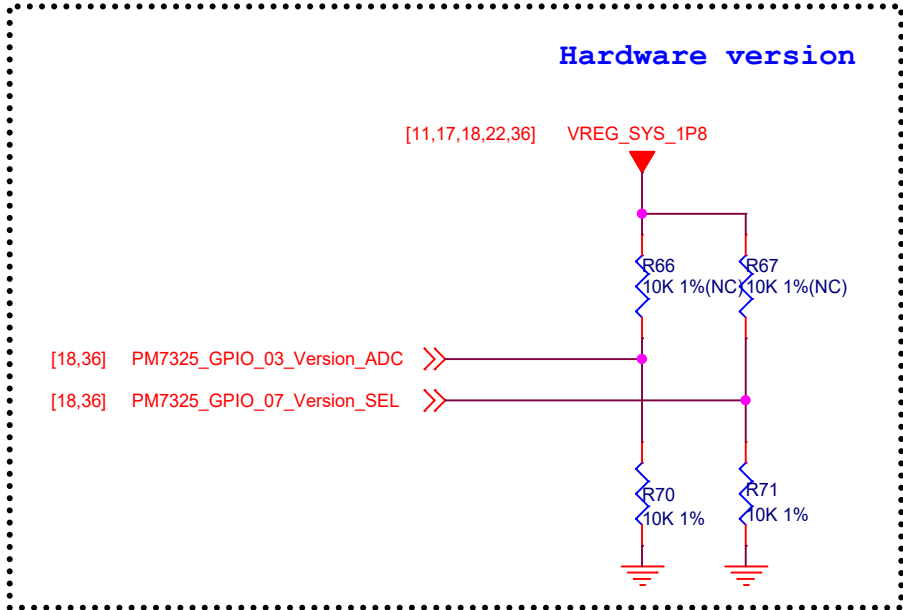
Note:
GPIO_03 is required for easy debug of PMIC faults,
the TP placement on board should be in such a way that it is easily accessible for probe

PM7325 CTRL GPIO GND

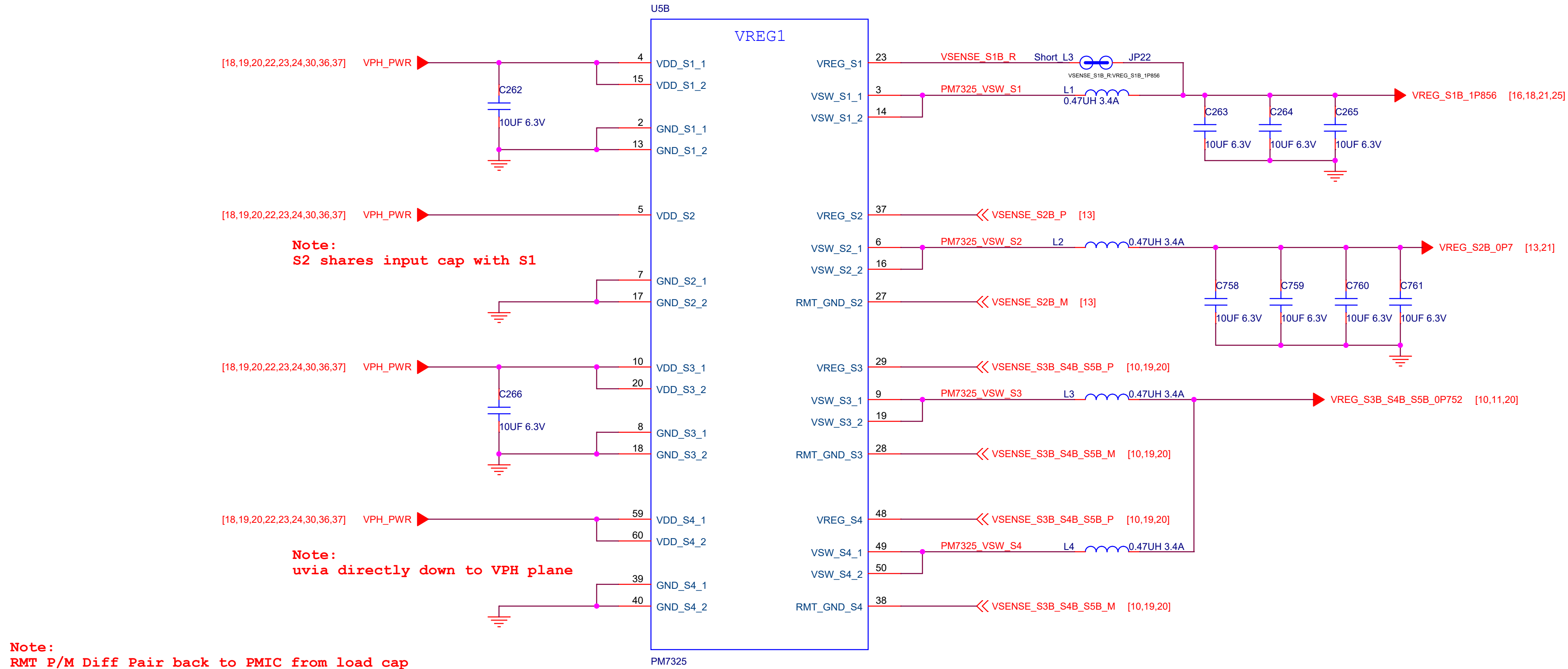
Note:
SPMI_CLK & SPMI_DATA should be routed away from noisy traces
Route signals as a diff pair as much as possible



NOTE: CBL
delete CBL net to LGA Pin.
Qualcomm CE comment:
If your device has PM7250B chip, the PM7325 GPIO_05 do not support CBL.



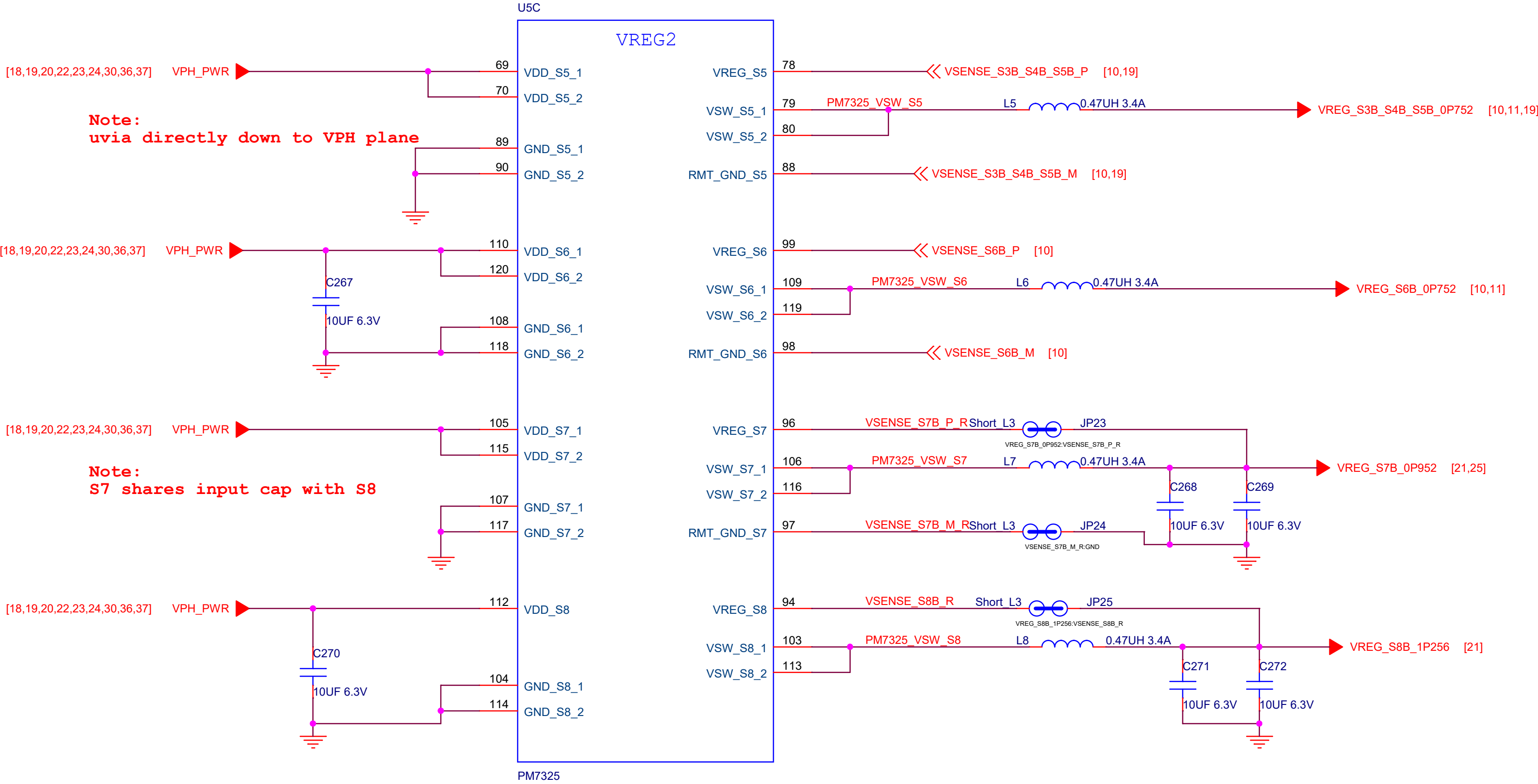
PM7325 BUCKS 1 OF 2



Regulator	type	IRATED (A)	voltage	use
S1B	HFS510	3500	1.856	HV sub regulation
S2B	FTS520	2500	0.876	EBI
S3B_S4B_S5B	FTS520	13500	0.752	APC1
S6B	FTS520	4500	0.752	APC0
S7B	FTS520	4500	0.952	LV sub regulation
S8B	HFS510	4000	1.256	MV sub regulation

Size	Title:	RADXA DRAGON Q6A	REV
	Custom Page Name:	PM7325_Bucks_S1-S4	
Date:	Friday, September 12, 2025	Sheet 19 of 37	

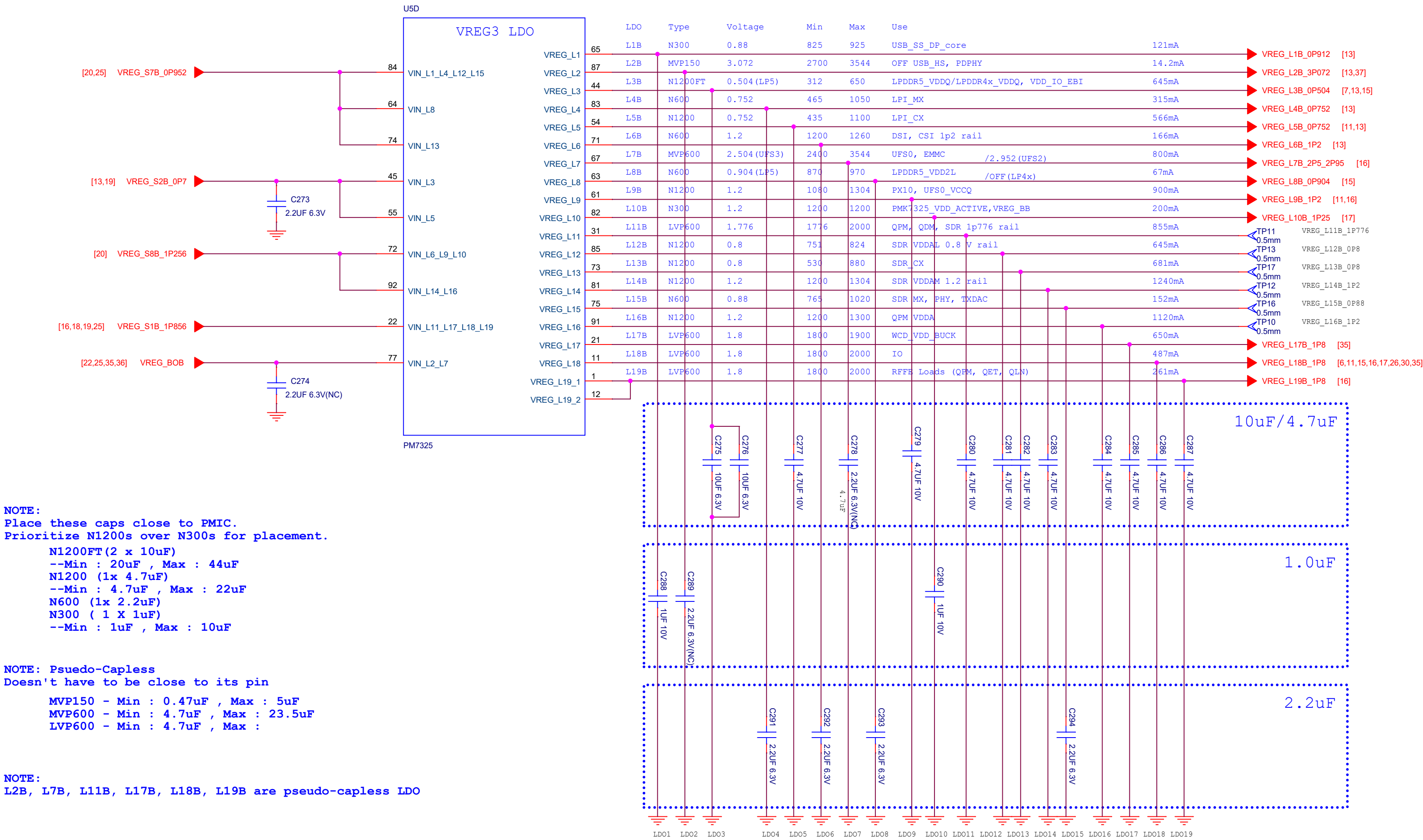
PM7325 BUCKS 2 OF 2



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Size	Title: RADXA DRAGON Q6A	REV
Custom Page Name:	PM7325_Bucks_S5-S8	V1.21
Date:	Friday, September 12, 2025	Sheet 20 of 37

PM7325 LDOs



NOTE:
Place these caps close to PMIC.
Prioritize N1200s over N300s for placement.

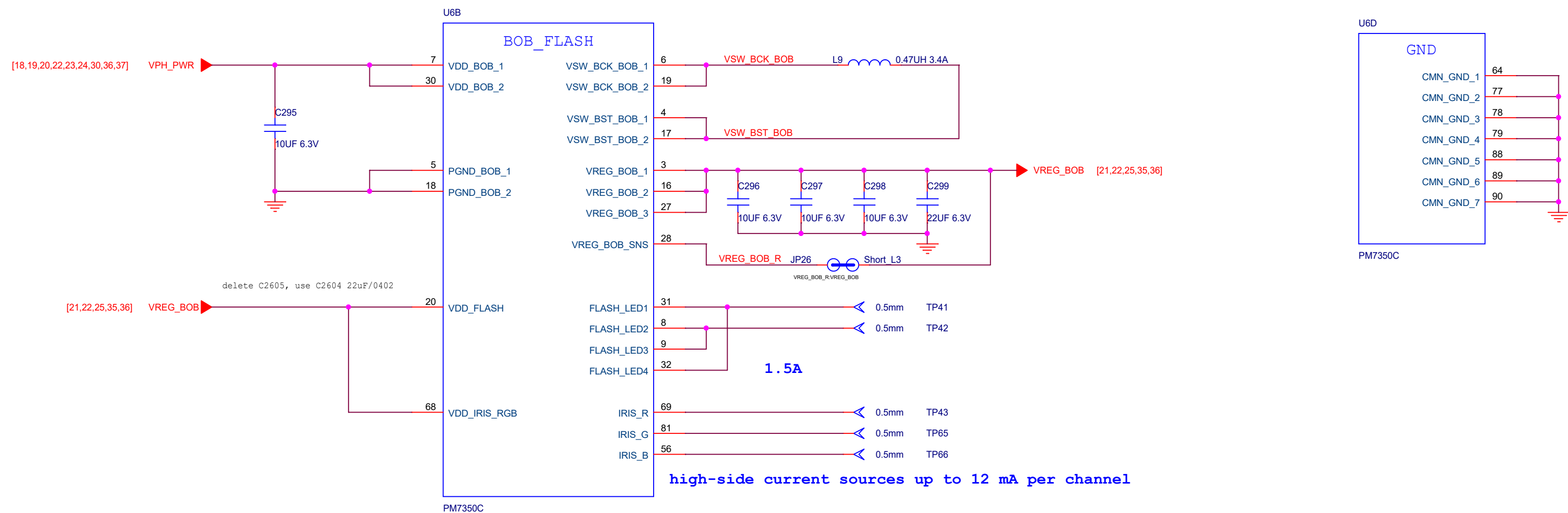
N1200FT (2 x 10uF)
--Min : 20uF , Max : 44uF
N1200 (1x 4.7uF)
--Min : 4.7uF , Max : 22uF
N600 (1x 2.2uF)
N300 (1 X 1uF)
--Min : 1uF , Max : 10uF

NOTE: Psuedo-Capless
Doesn't have to be close to its pin

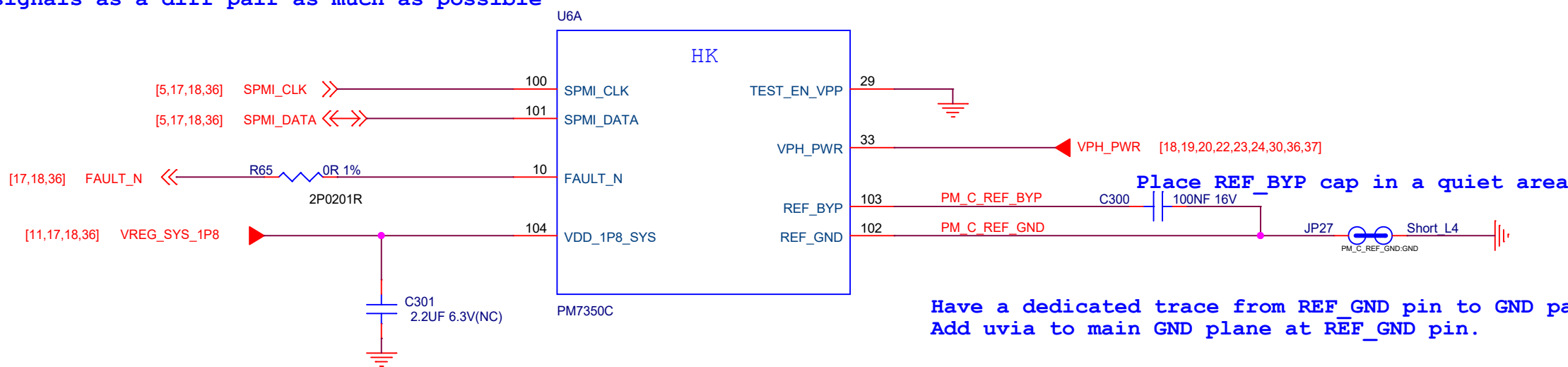
MVP150 - Min : 0.47uF , Max : 5uF
MVP600 - Min : 4.7uF , Max : 23.5uF
LVP600 - Min : 4.7uF , Max :

NOTE:
L2B, L7B, L11B, L17B, L18B, L19B are pseudo-capless LDO

PM7350C CTRL GPIO GND



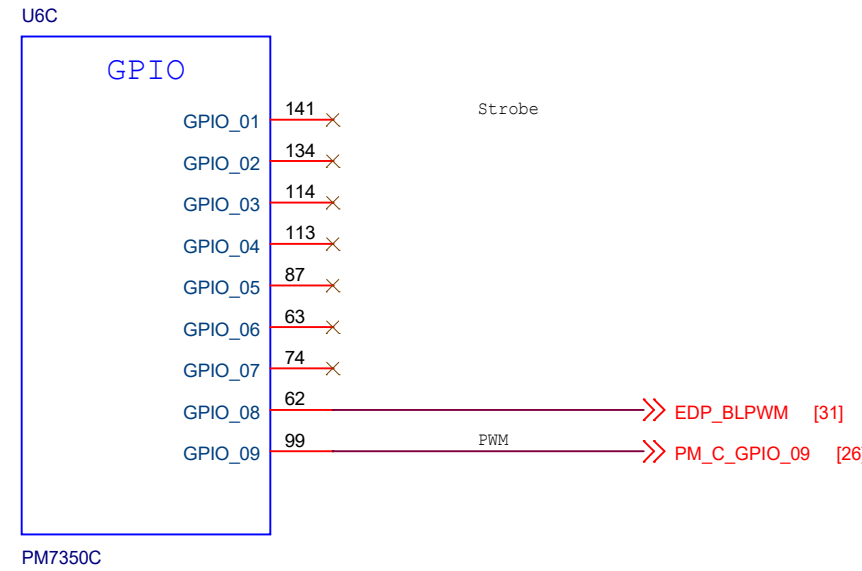
Note:
SPMI_CLK & SPMI_DATA should be routed away from noisy traces
Route signals as a diff pair as much as possible



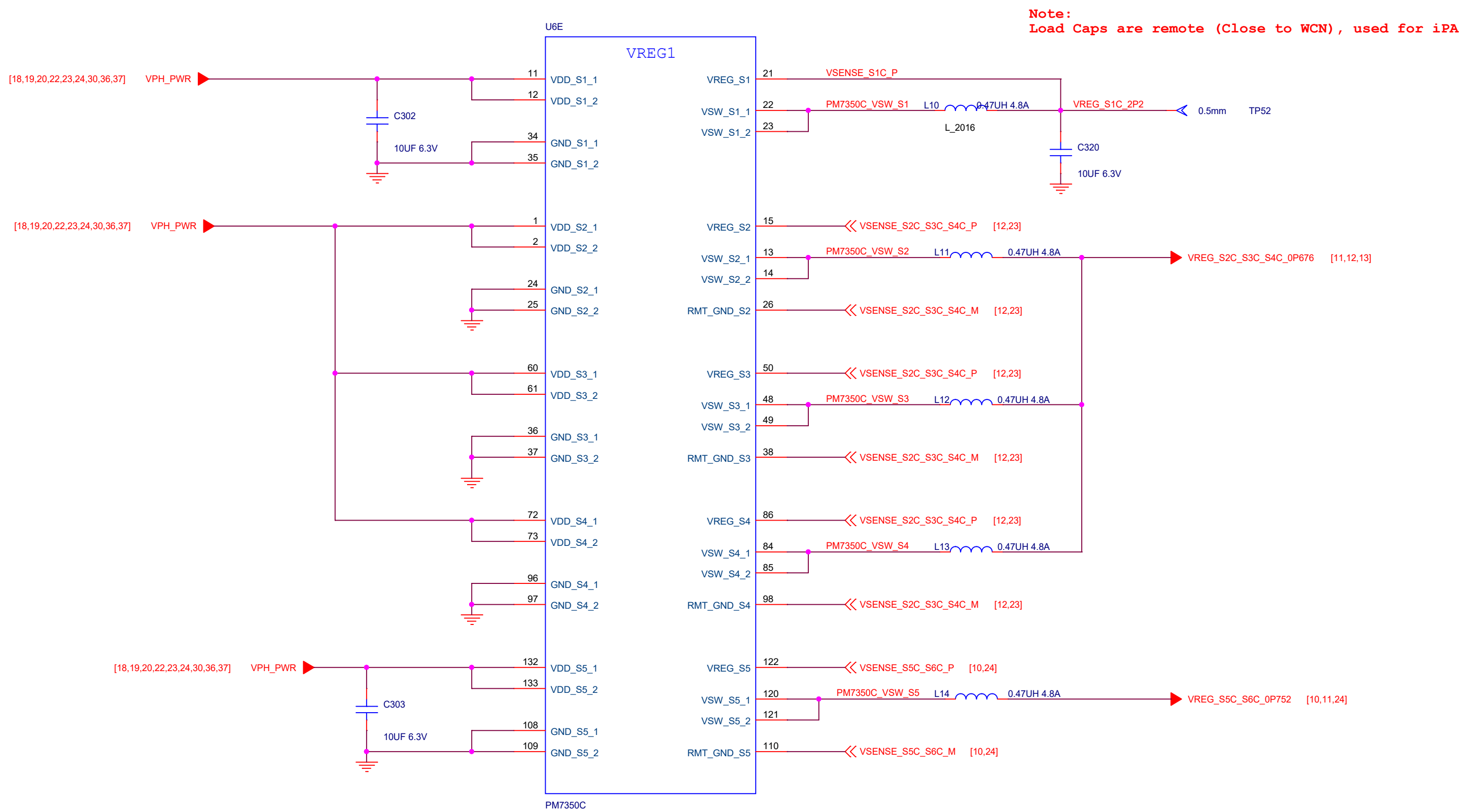
NOTE:
MV: VPH_PWR or 1.8 V
LV : 1.8 V only

GPIO	Type	Configuration	Special function for QCM6490
1	LV	AMUX	FLASH_STROBE
2	LV	AMUX	FLASH_STROBE
3	LV	AMUX	FLASH_STROBE / PM8008_1_EN
4	LV	AMUX	FLASH_STROBE / PM8008_2_EN
5	MV	AMUX	AOSS_SLEEP_INDICATOR
6	MV		
7	MV		EDP_LCD_BL_EN
8	MV	PWM	EDP_LCD_PWM
9	MV	PWM	

Please note that only GPIO_08 is available for fixed duty cycle variable frequency mode.



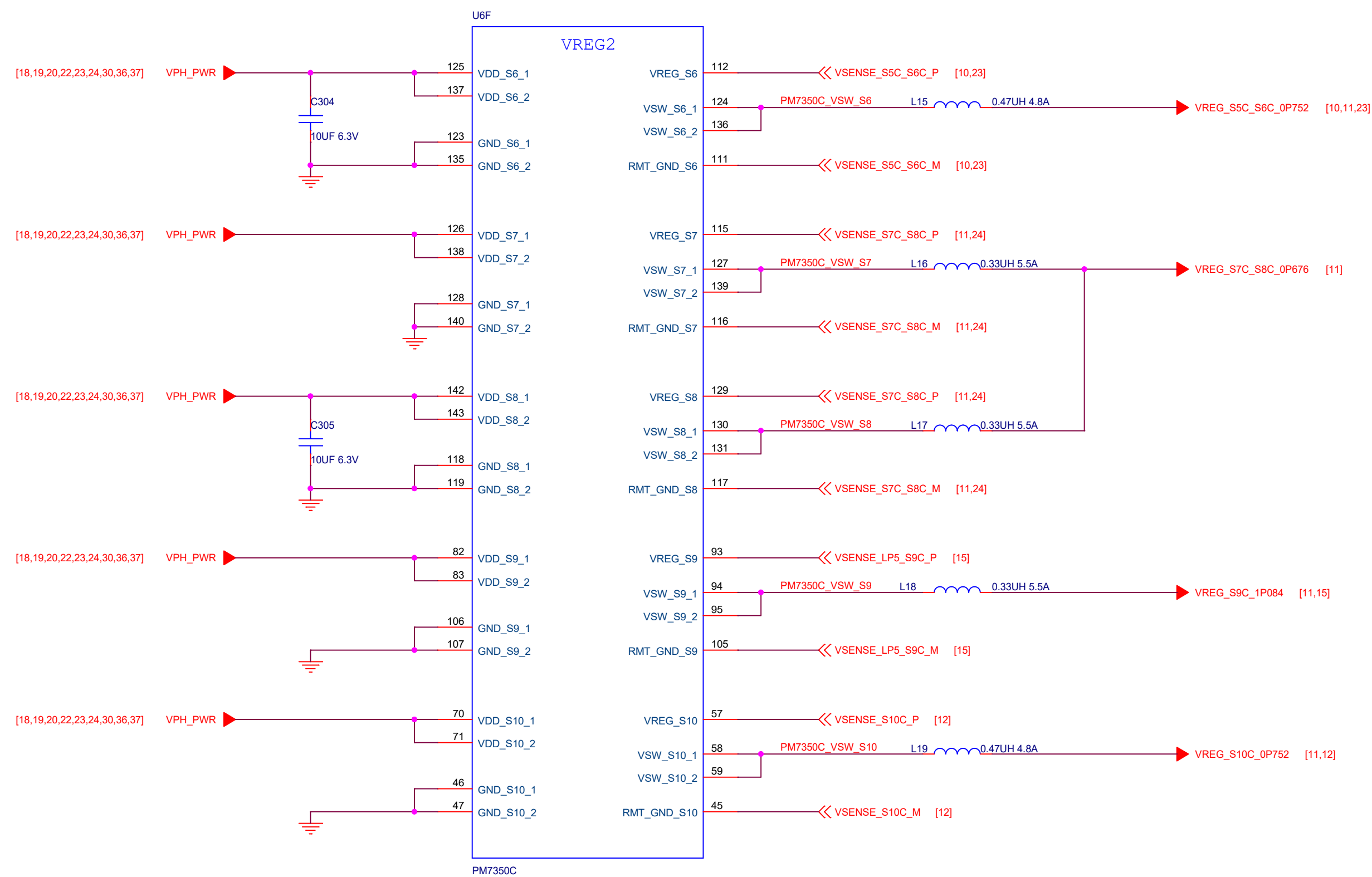
PM7350C BUCKS 1 OF 2



Note:
RMT P/M Diff Pair back to PMIC from load cap

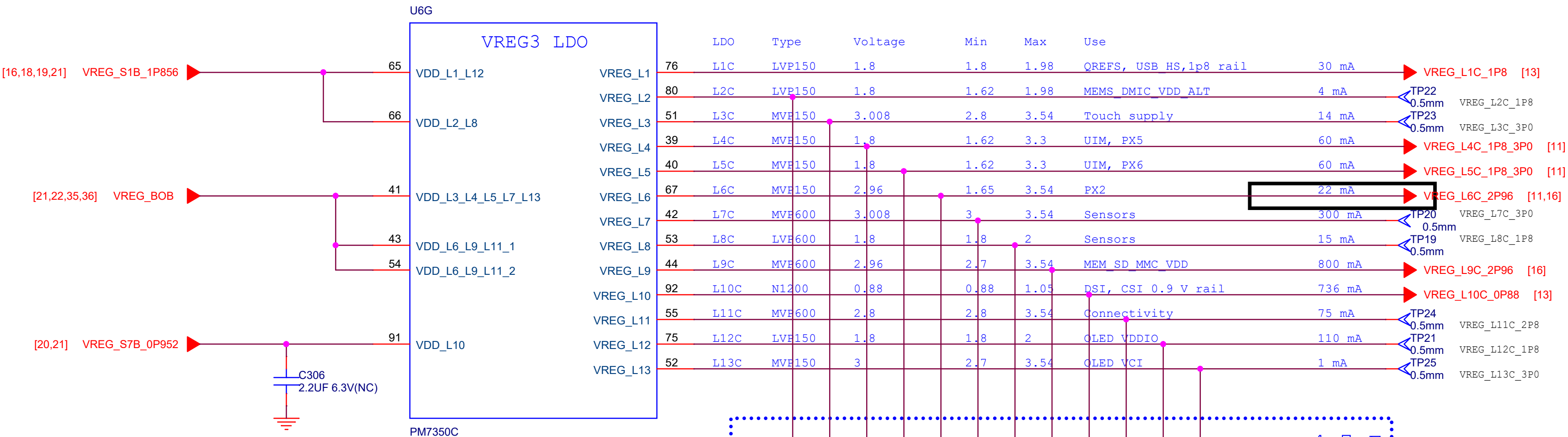
Regulator	type	IRATED (A)	voltage	use
S1C	HFS515	1.5	2.2	WCN IPA
S2C	FTS520	13.5	0.816	CX, EBI
S3C	FTS520			
S4C	FTS520			
S5C	FTS520	2	0.752	Modem
S6C	FTS520			
S7C	FTS520	4	0.752	GFX
S8C	FTS520			
S9C	FTS520	1	1.084	LP_VDD2/2H
S10C	FTS520	1	0.752	MX

PM7350C BUCKS 2 OF 2



Size	Title:	RADXA DRAGON Q6A	REV
C	Page Name:	PM7350C_Bucks_S6-S10	V1.21
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PM7350C LDOs



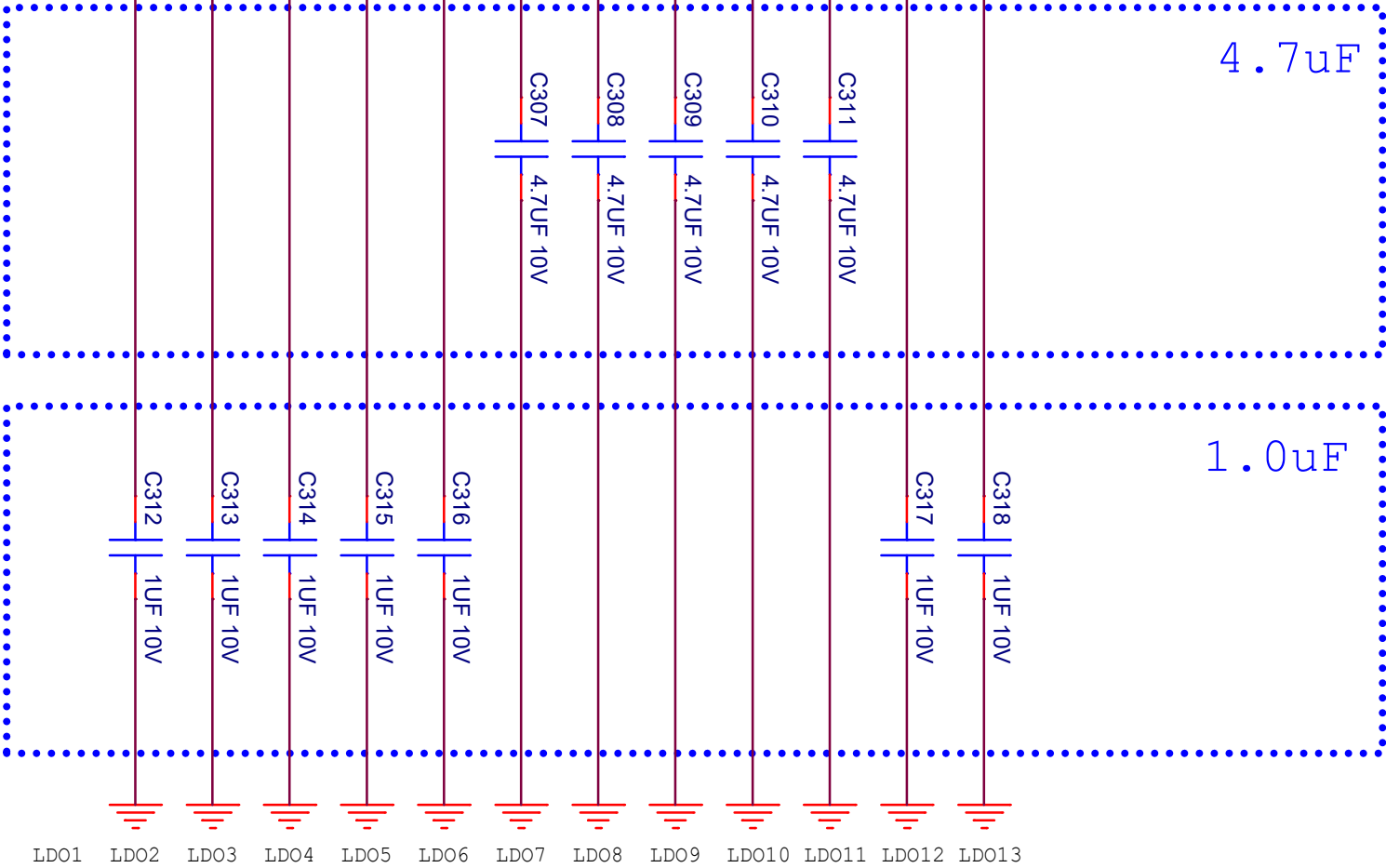
Note:
Place cap close to PMIC
DNI unless VI validates we actually need them
and/or if input ESL > 15nH

NOTE:
Add local cap based simulation result

NOTE:
N1200
Min : 4.7uF , Max : 22uF
Place these caps close to PMIC.

Psuedo-Capless:
LVP150 - Min : 1uF , Max : 5uF
MVP150 - Min : 0.47uF , Max : 5uF
MVP600 - Min : 4.7uF , Max : 23.5uF
Doesn't have to be close to its pin

Pseudo capless allows users to place the LDO output capacitor physically/electrically far from the LDO output, near the load.
The routing ESL/ESR between the PMIC pin and the remote Cout should meet the capless LDO spec.
All PMOS LDOs are considered pseudo-capless, unless it has internal PMIC load.
If an internal PMIC load, the output cap must be placed close to the PMIC.



jtag testpoint

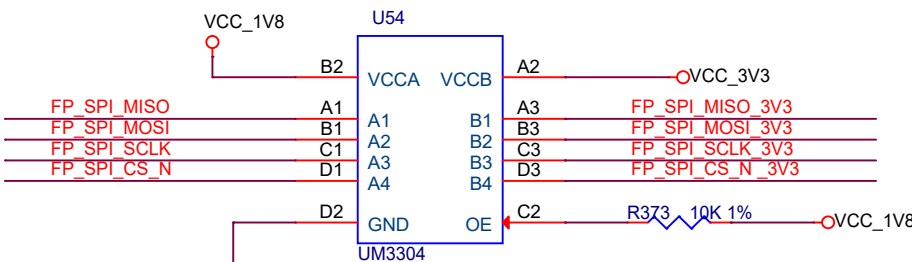
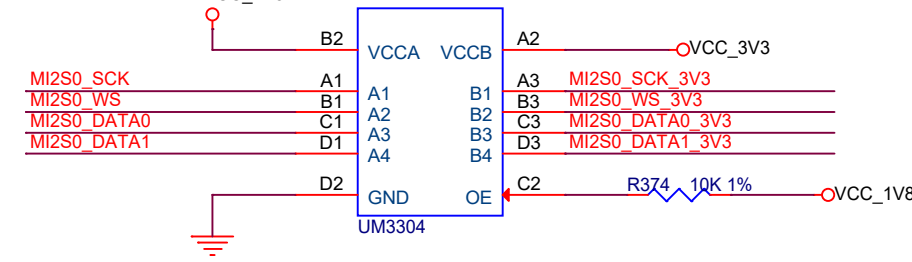
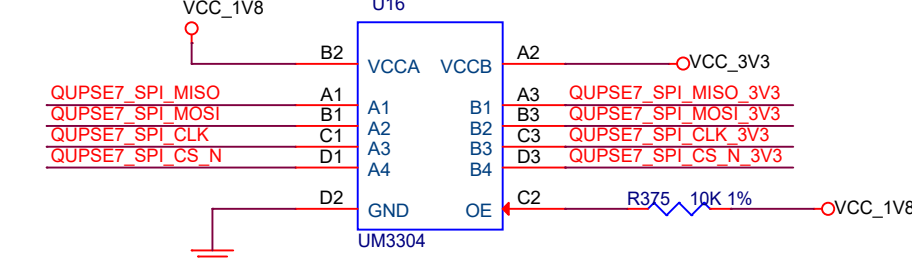
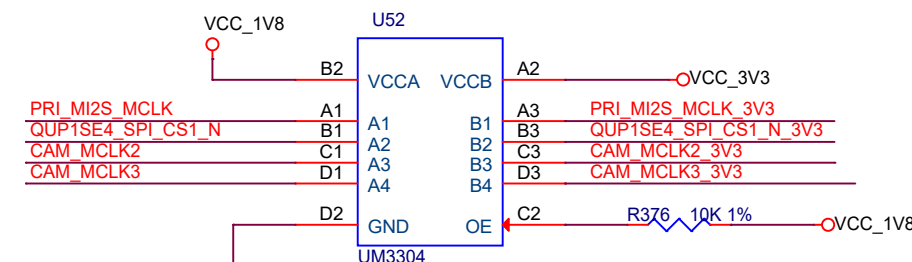
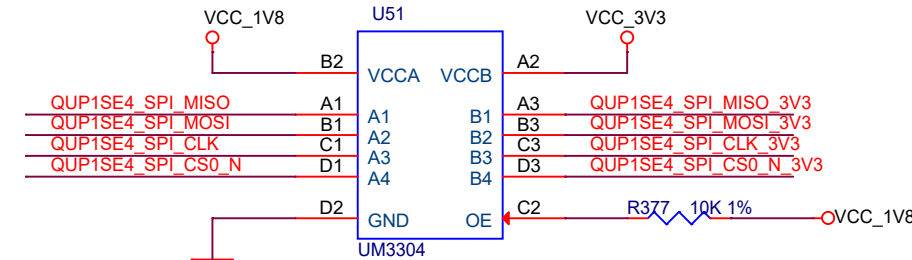
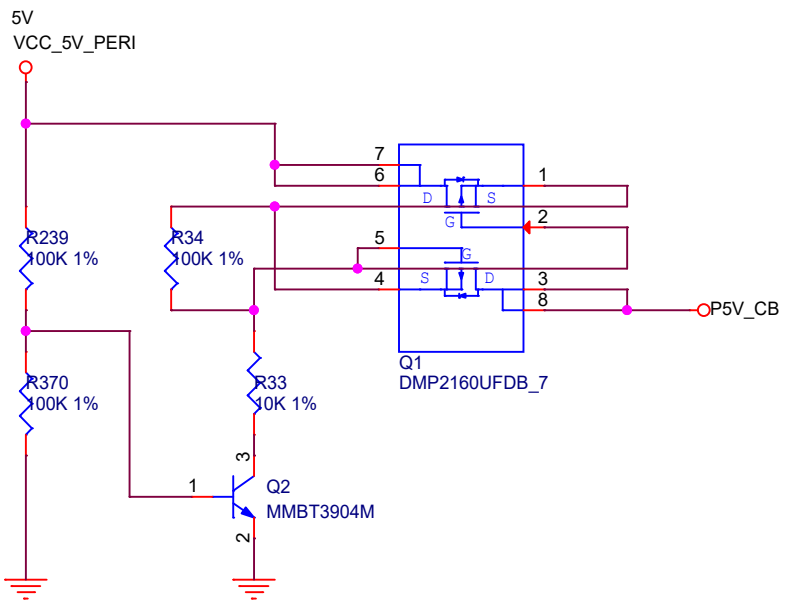
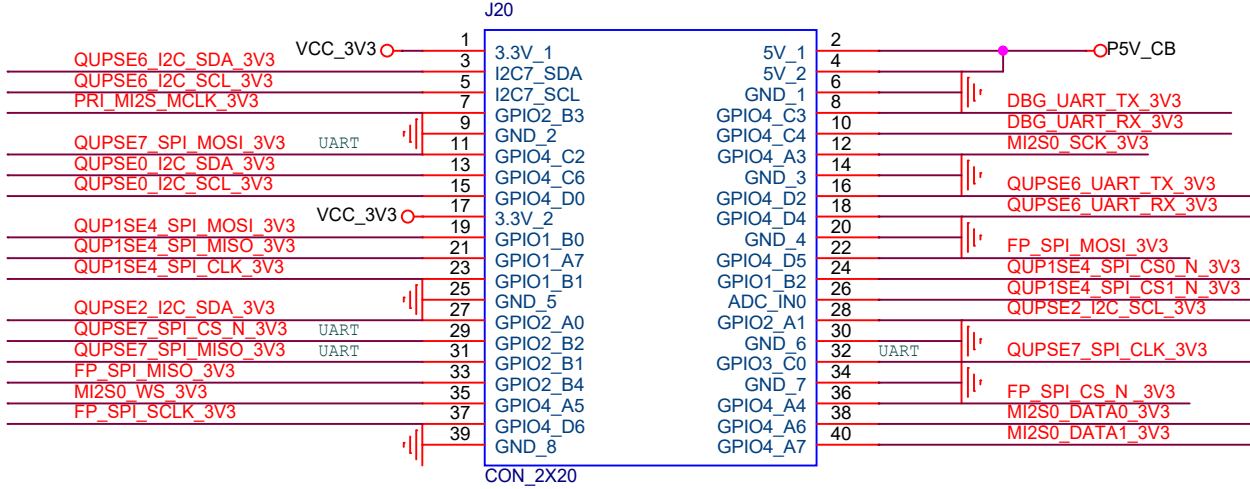
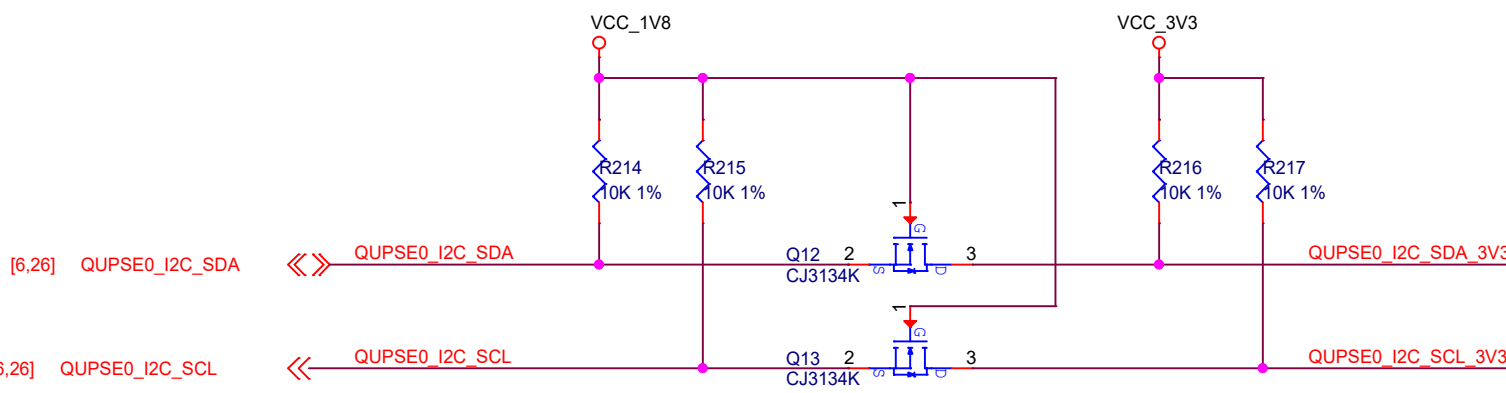
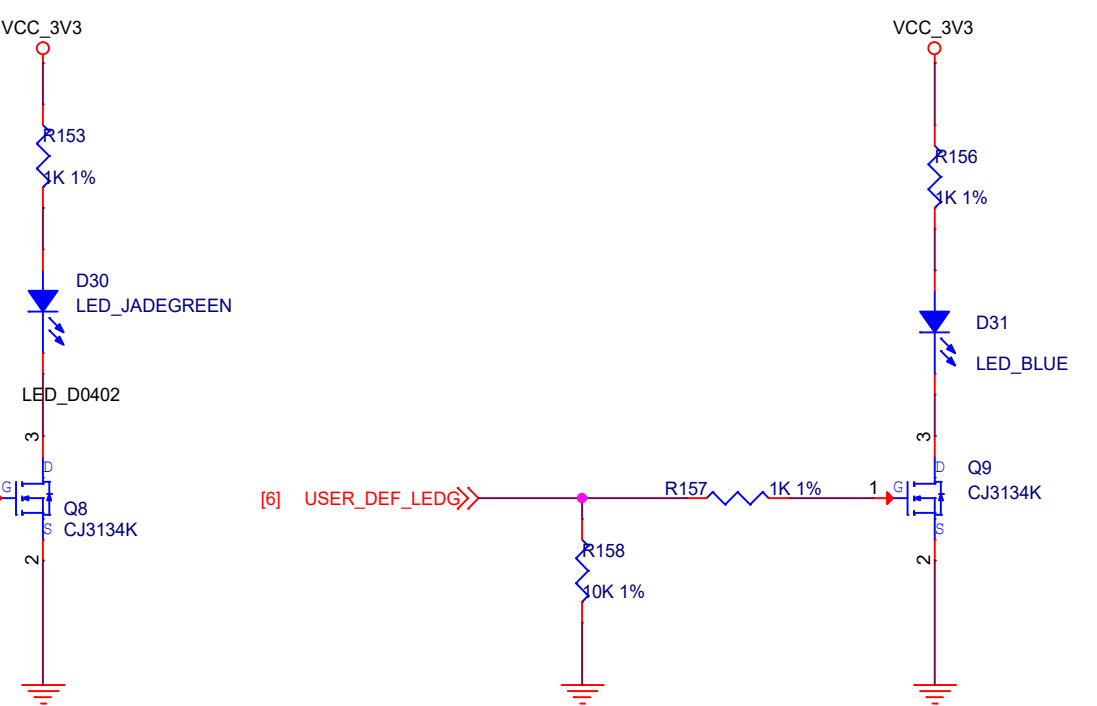
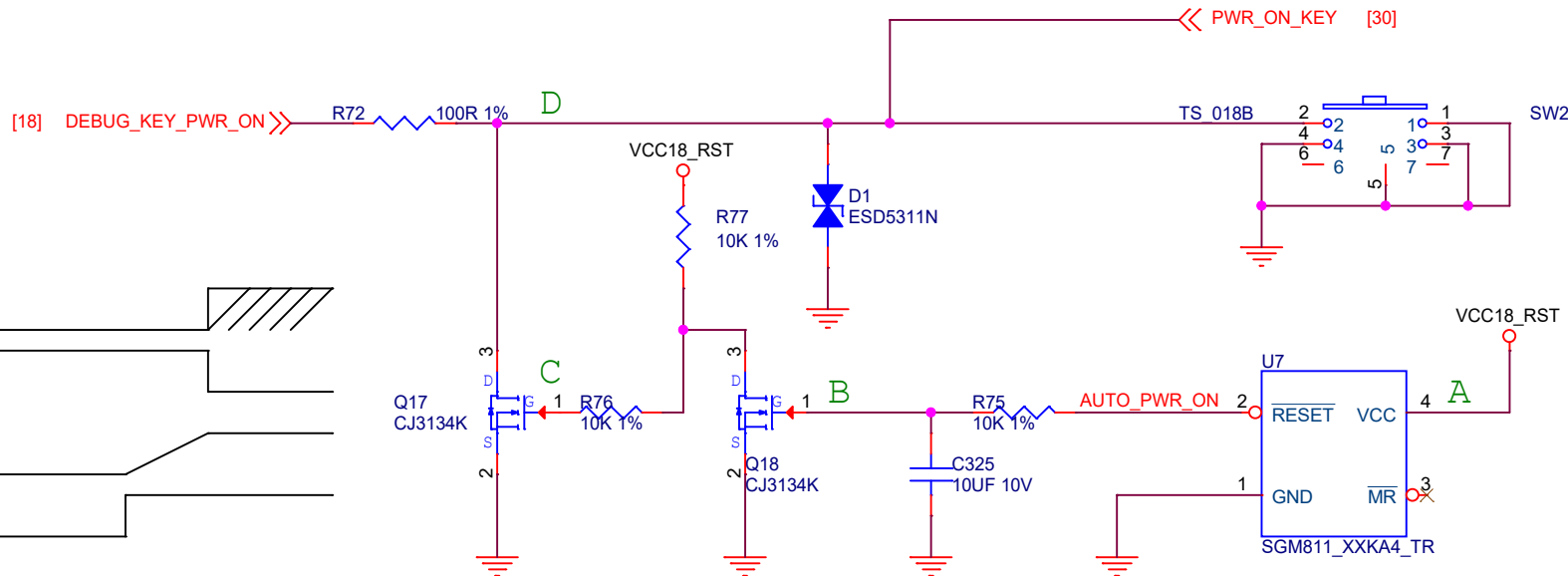
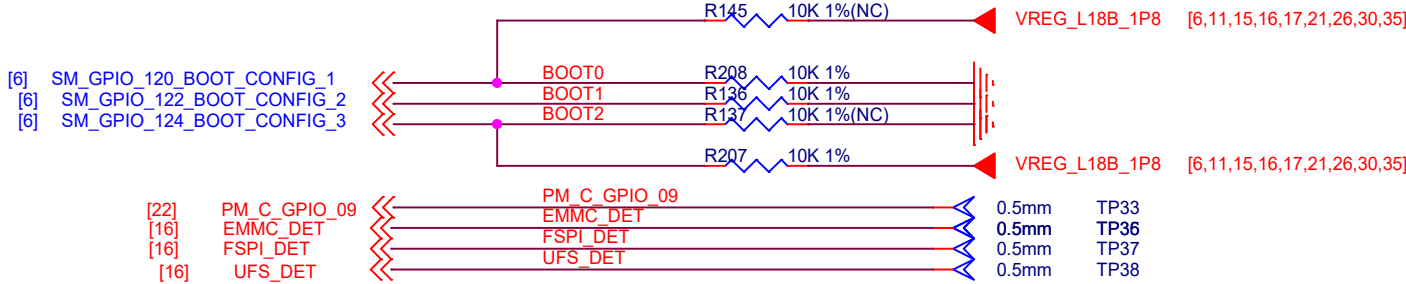
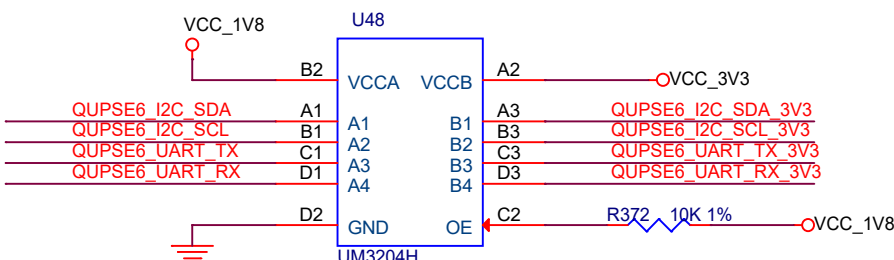
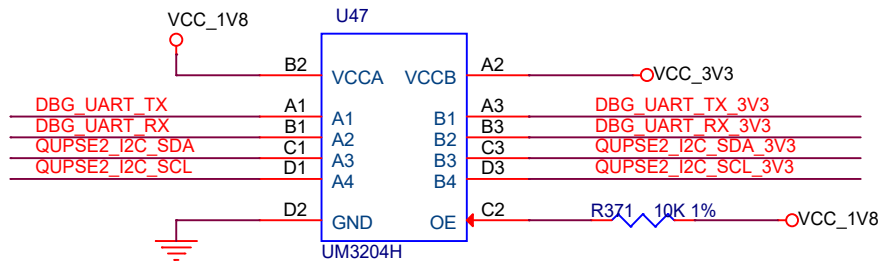
TP2 0.5mm >>> SM_RESOUT_N [5,16]
TP3 0.5mm >>> JTAG_PS_HOLD [17]

SDH FRAME&COVER
Mark

PRI_MI2S_MCLK	>>>	PRI_MI2S_MCLK	[6]
QUP1SE4_SPI_MISO	>>>	QUP1SE4_SPI_MISO	[6]
QUP1SE4_SPI_MOSI	>>>	QUP1SE4_SPI_MOSI	[6]
QUP1SE4_SPI_CLK	>>>	QUP1SE4_SPI_CLK	[6]
QUP1SE4_SPI_CS0_N	>>>	QUP1SE4_SPI_CS0_N	[6]
QUP1SE4_SPI_CS1_N	>>>	QUP1SE4_SPI_CS1_N	[6]
FP_SPI_MISO	>>>	FP_SPI_MISO	[6]
FP_SPI_MOSI	>>>	FP_SPI_MOSI	[6]
FP_SPI_SCLK	>>>	FP_SPI_SCLK	[6]
FP_SPI_CS_N	>>>	FP_SPI_CS_N	[6]
DBG_UART_TX	>>>	DBG_UART_TX	[6]
DBG_UART_RX	>>>	DBG_UART_RX	[6]
QUPSE6_I2C_SDA	>>>	QUPSE6_I2C_SDA	[6]
QUPSE6_I2C_SCL	>>>	QUPSE6_I2C_SCL	[6]
QUPSE6_UART_TX	>>>	QUPSE6_UART_TX	[6]
QUPSE6_UART_RX	>>>	QUPSE6_UART_RX	[6]
MI2S0_SCK	>>>	MI2S0_SCK	[6]
MI2S0_DATA0	>>>	MI2S0_DATA0	[6]
MI2S0_DATA1	>>>	MI2S0_DATA1	[6]
MI2S0_WS	>>>	MI2S0_WS	[6]

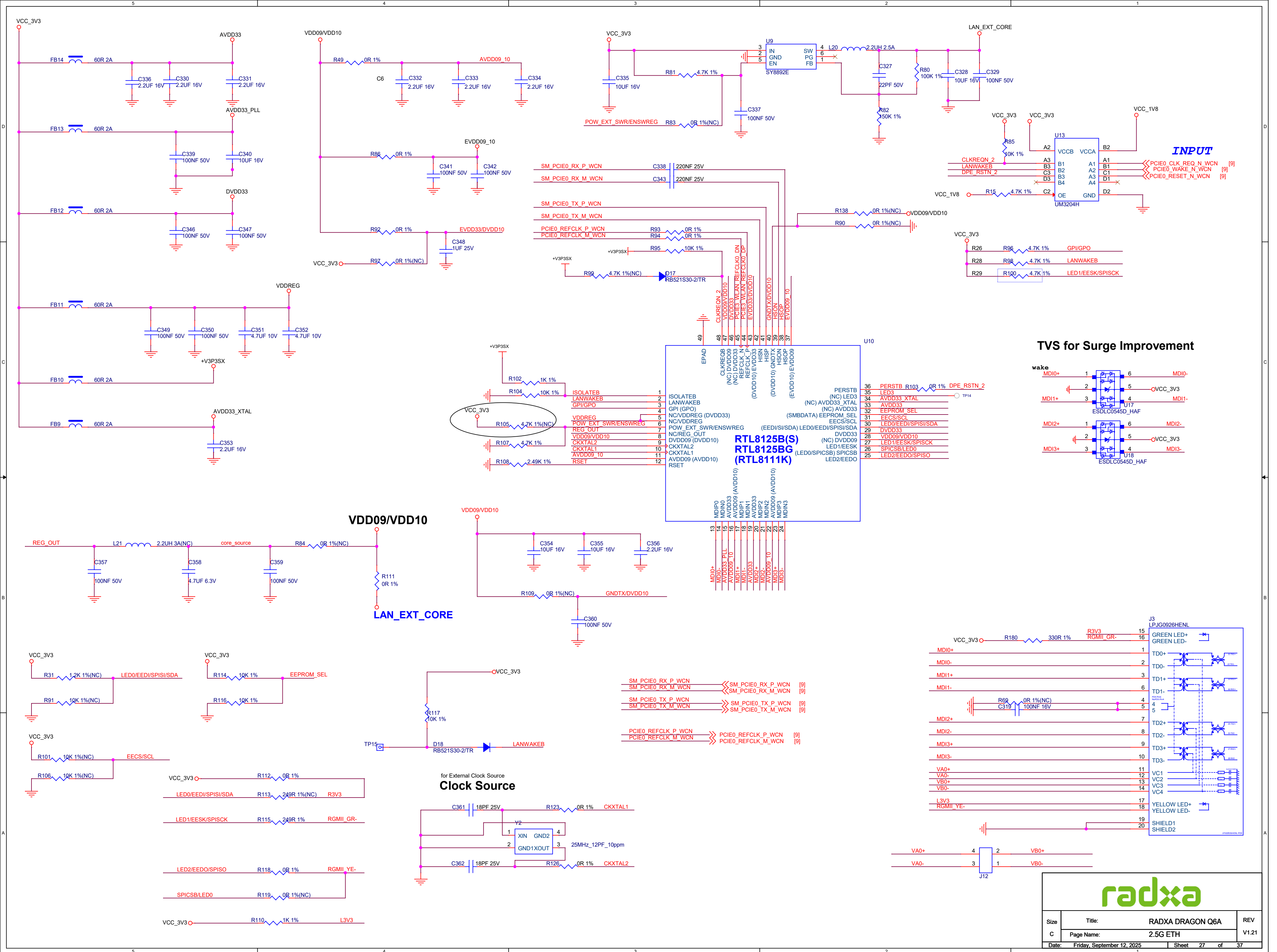
QUPSE7_SPI_MISO	>>>	QUPSE7_SPI_MISO	[6]
QUPSE7_SPI_MOSI	>>>	QUPSE7_SPI_MOSI	[6]
QUPSE7_SPI_CLK	>>>	QUPSE7_SPI_CLK	[6]
QUPSE7_SPI_CS_N	>>>	QUPSE7_SPI_CS_N	[6]
QUPSE0_I2C_SDA	>>>	QUPSE0_I2C_SDA	[6,26]
QUPSE0_I2C_SCL	>>>	QUPSE0_I2C_SCL	[6,26]
QUPSE2_I2C_SDA	>>>	QUPSE2_I2C_SDA	[6]
QUPSE2_I2C_SCL	>>>	QUPSE2_I2C_SCL	[6]

CAM_MCLK2	>>>	CAM_MCLK2	[6]
CAM_MCLK3	>>>	CAM_MCLK3	[6]
CAM_MCLK2_3V3	>>>	CAM_MCLK2_3V3	[34]
CAM_MCLK3_3V3	>>>	CAM_MCLK3_3V3	[34]



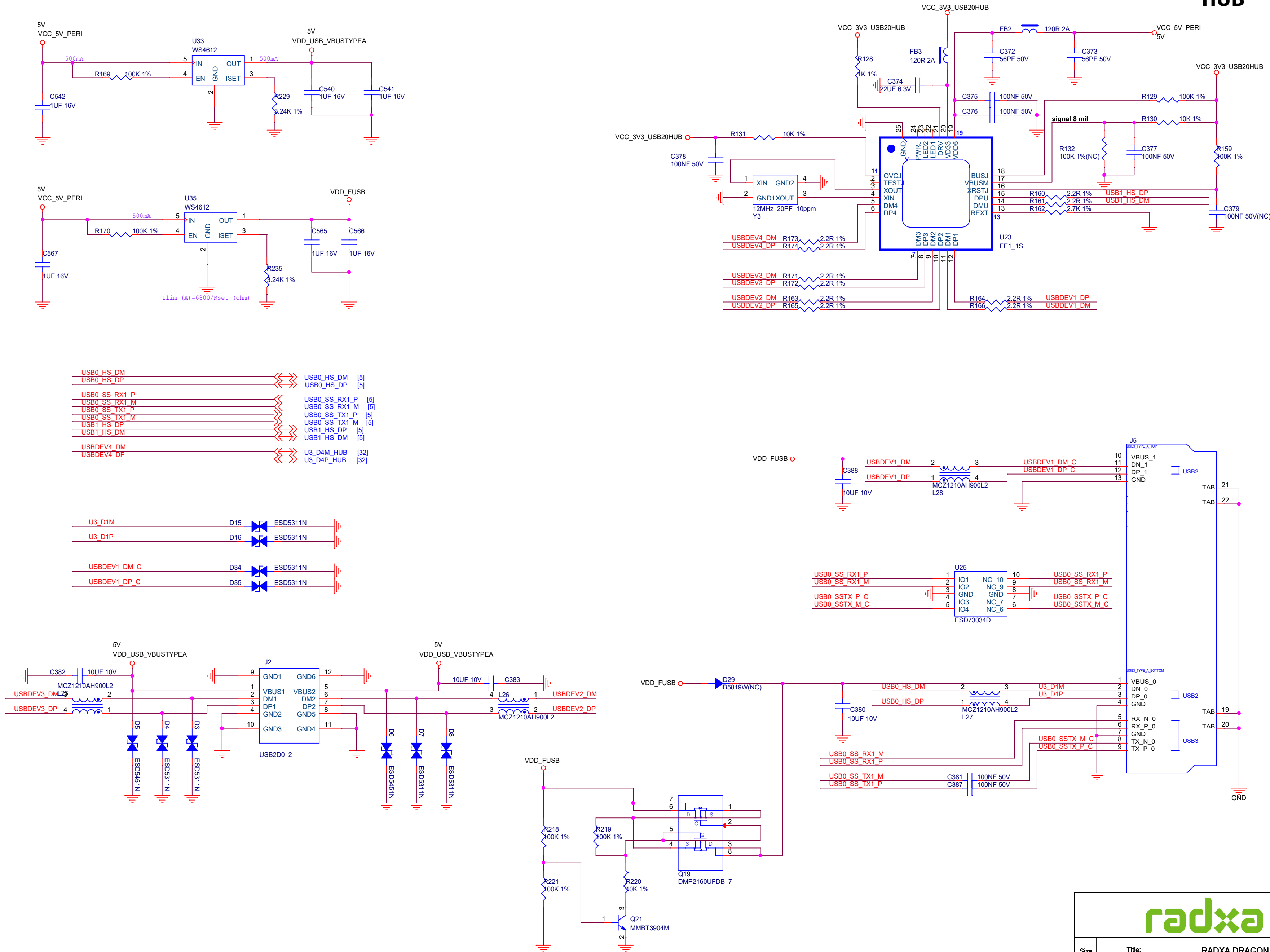
radxa

Size	Title: RADXA DRAGON Q6A	REV
C	Page Name: JTAG&TP&SHD	V1.21
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USB HUB x4 PORTS

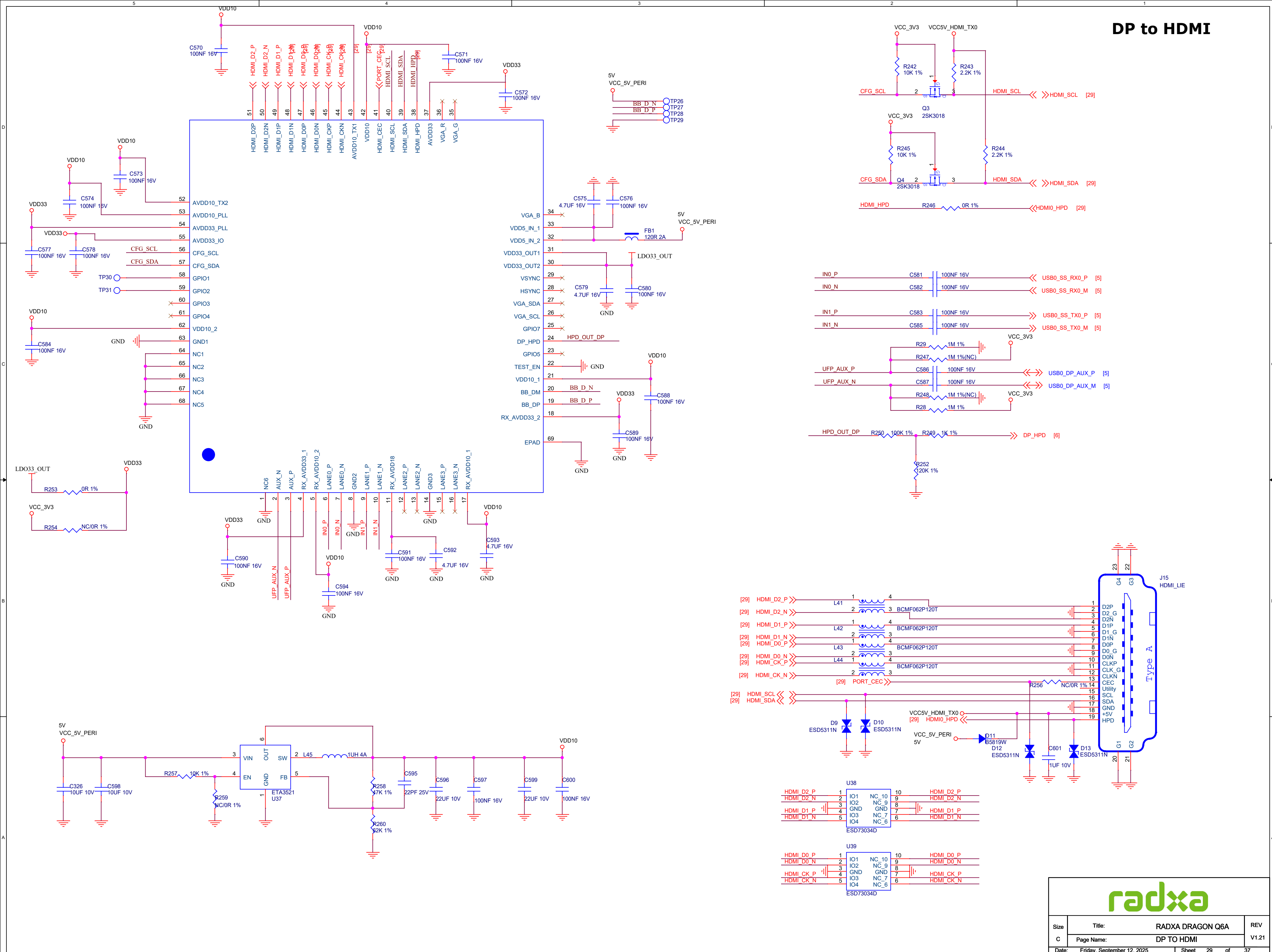
HUB



radxa

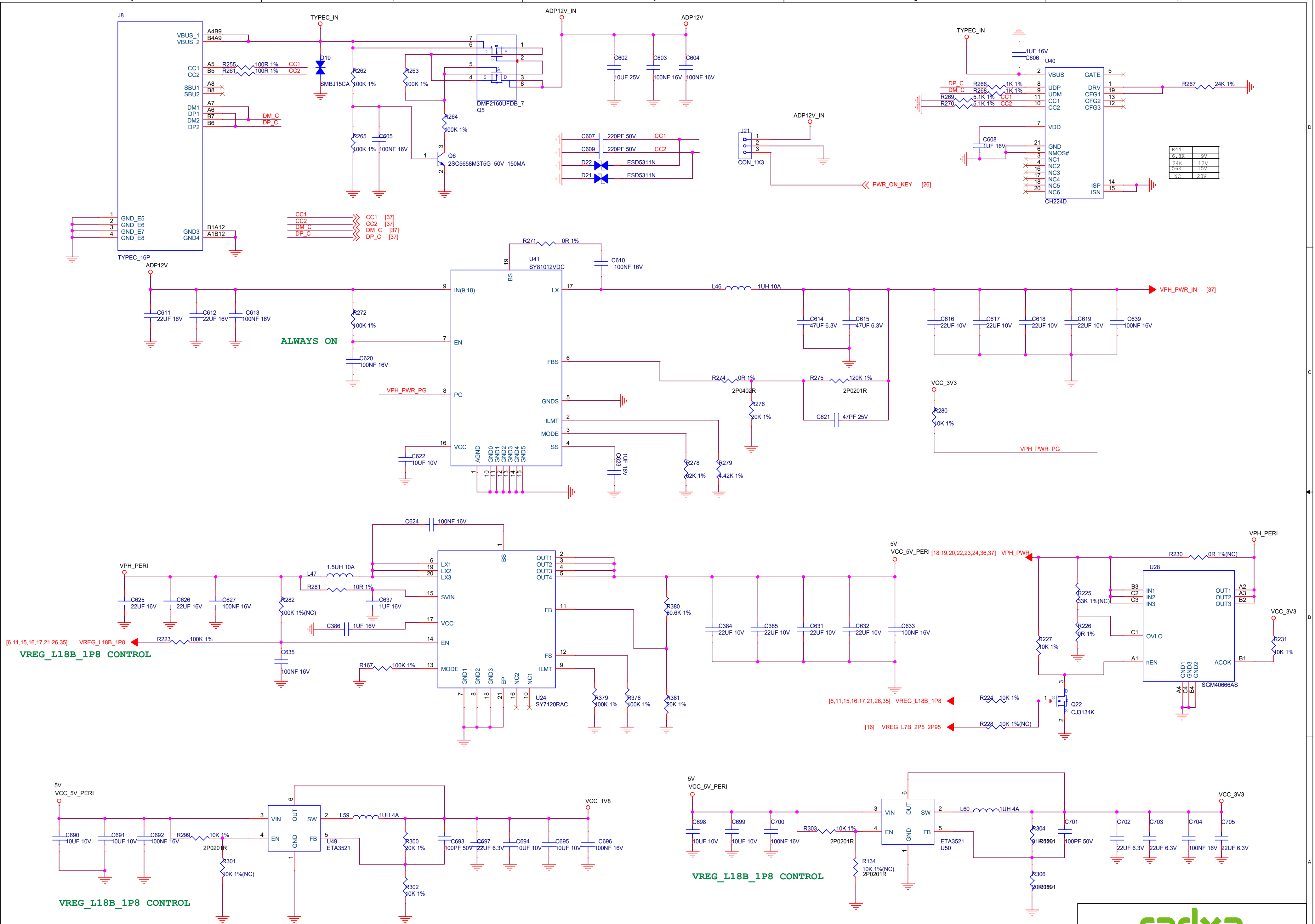
Size	Title:	RADXA DRAGON Q6A	REV
	Page Name:	USB	
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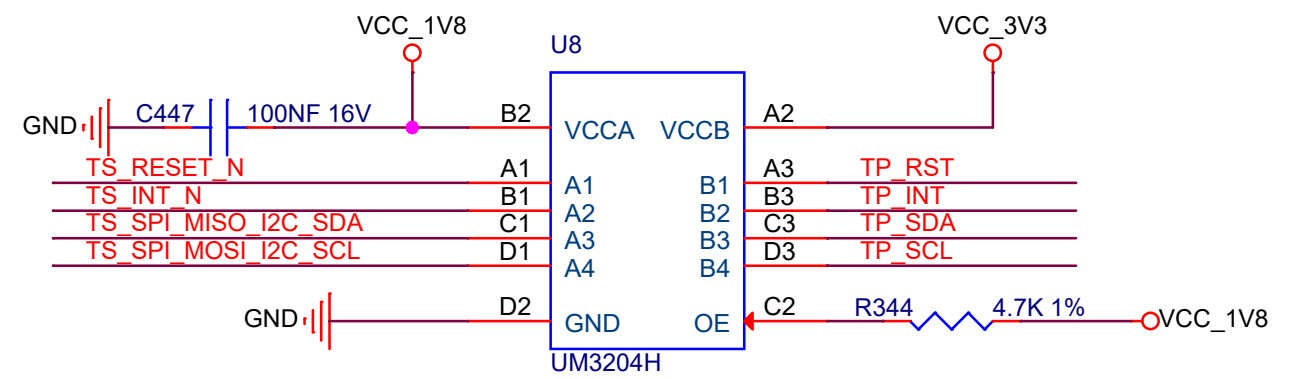
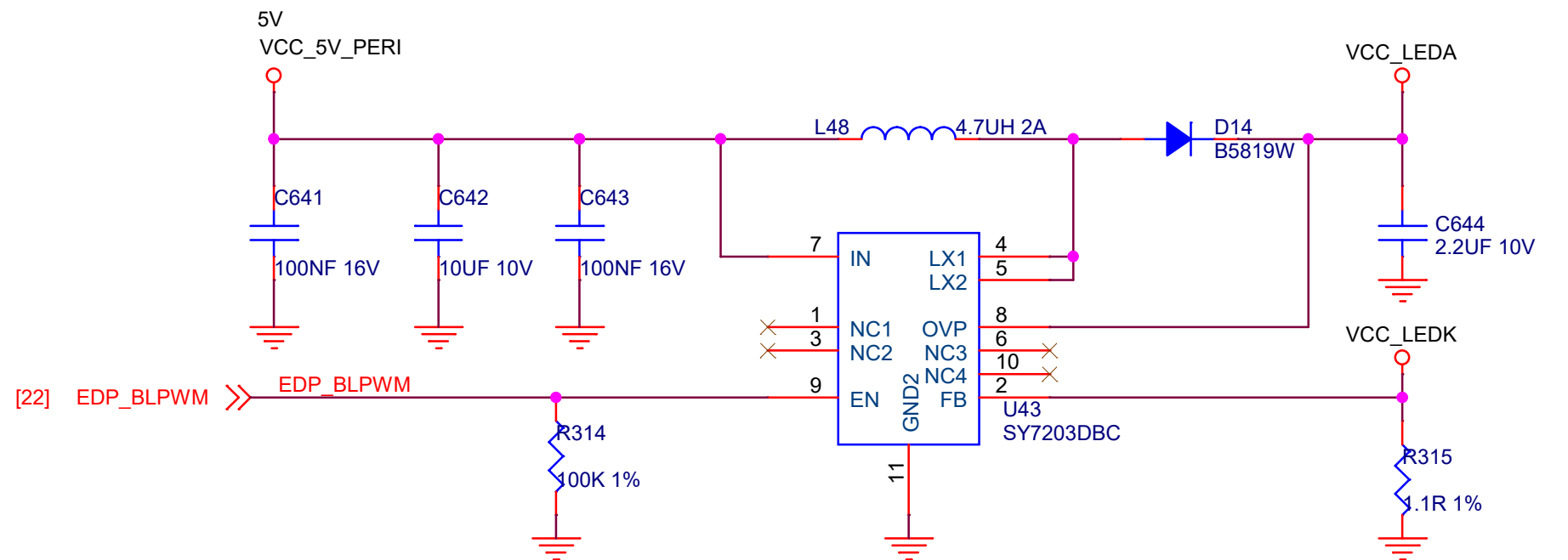
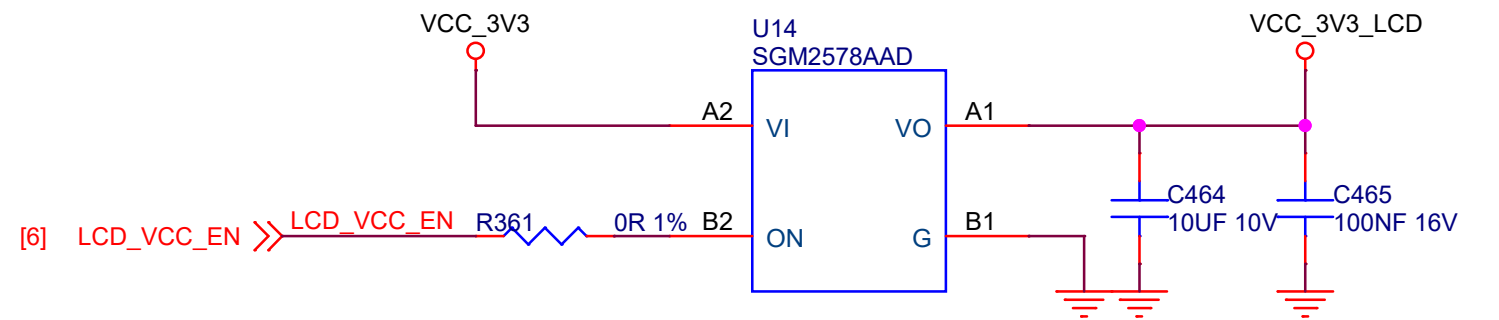
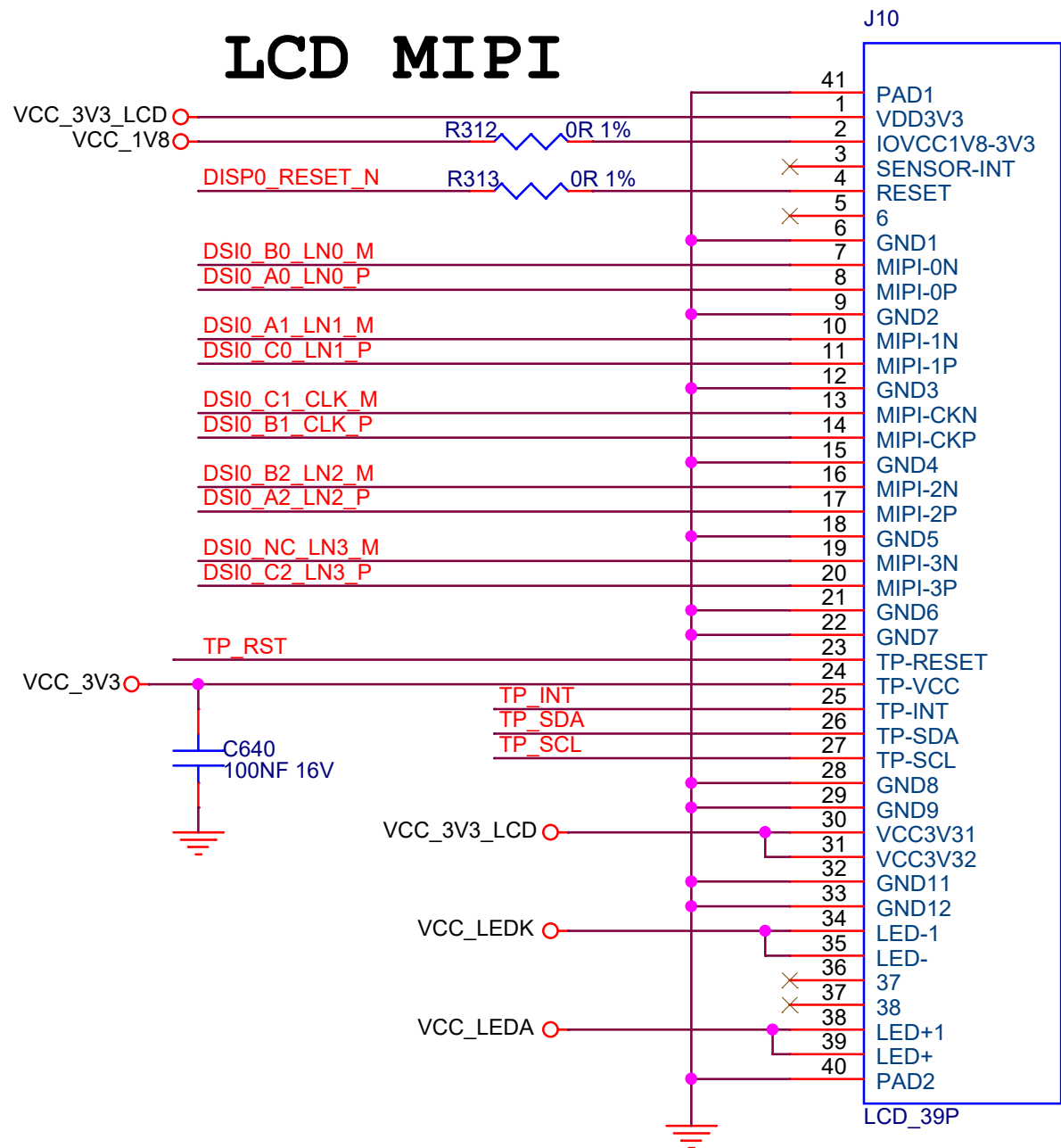
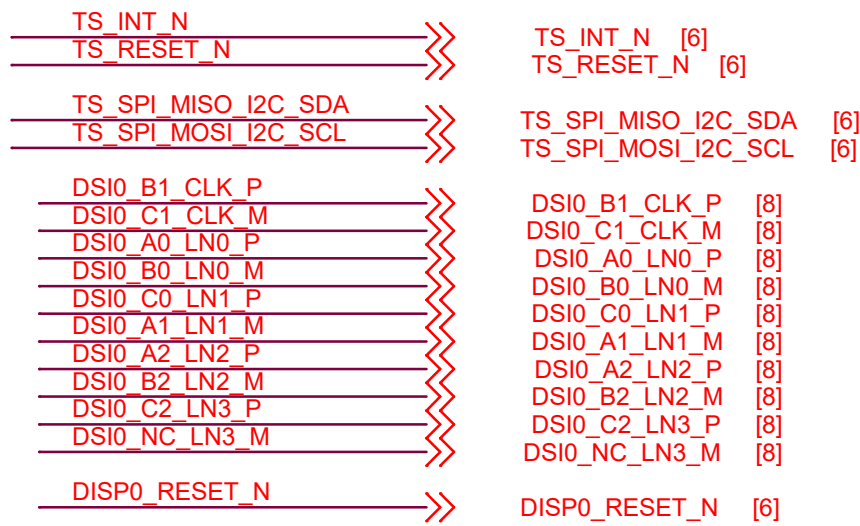
DP to HDMI



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Size	Title:	RADXA DRAGON Q6A	REV
	Page Name:	DP TO HDMI	
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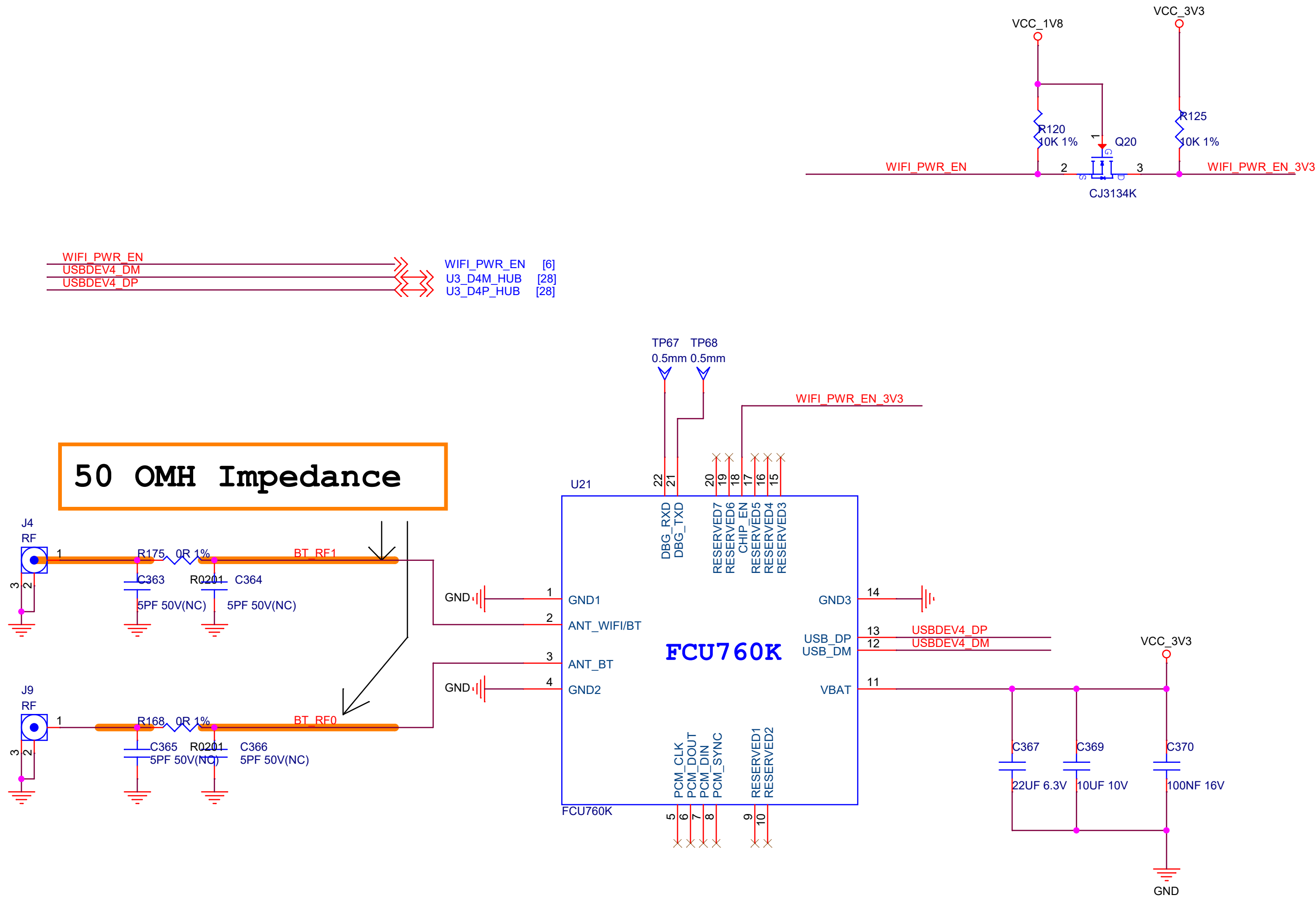




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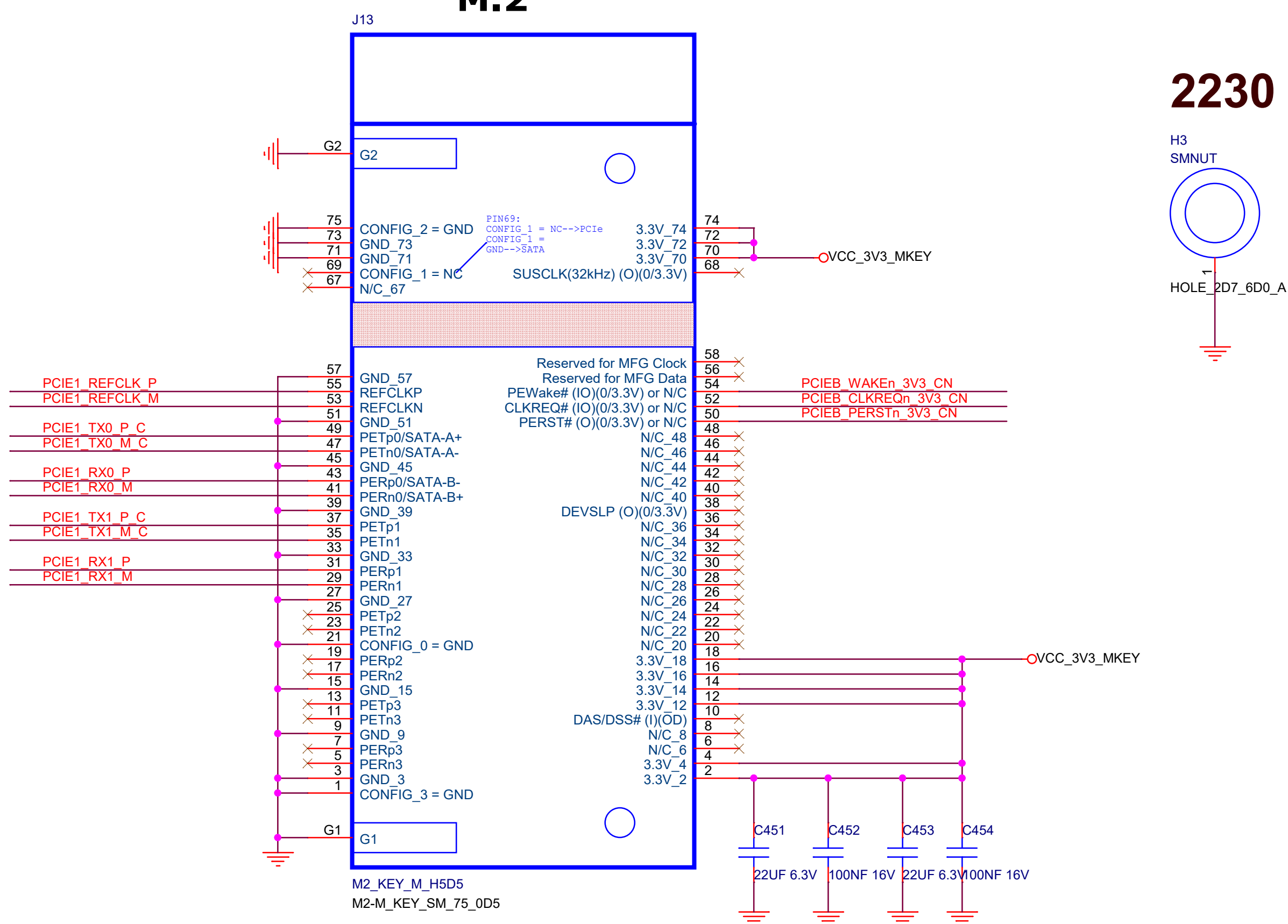
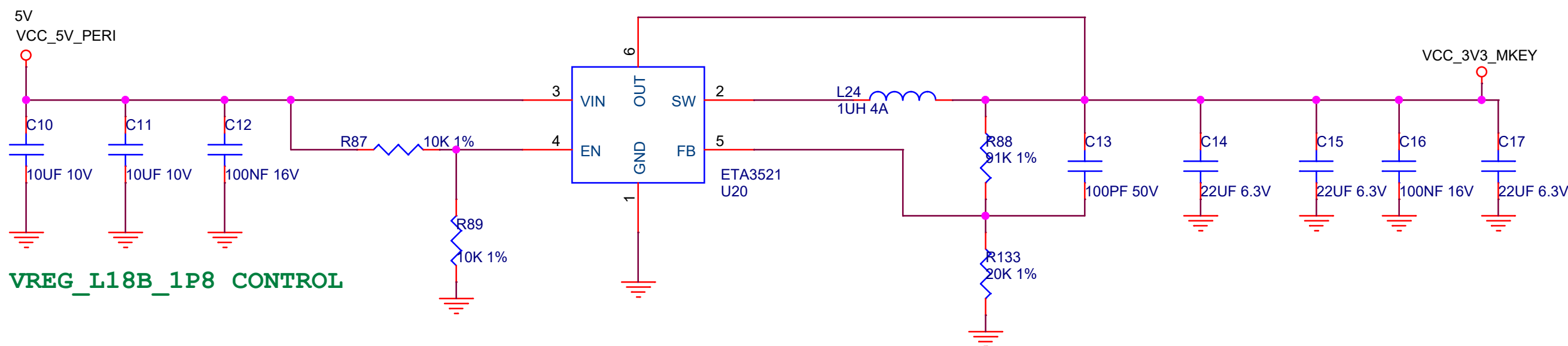
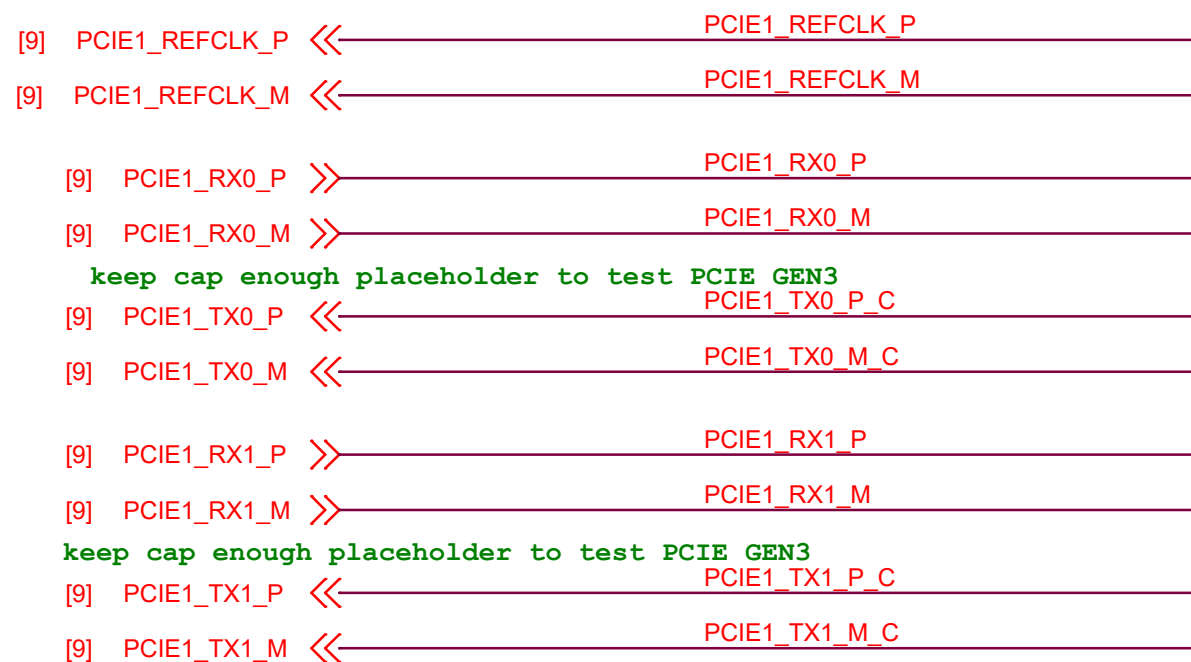
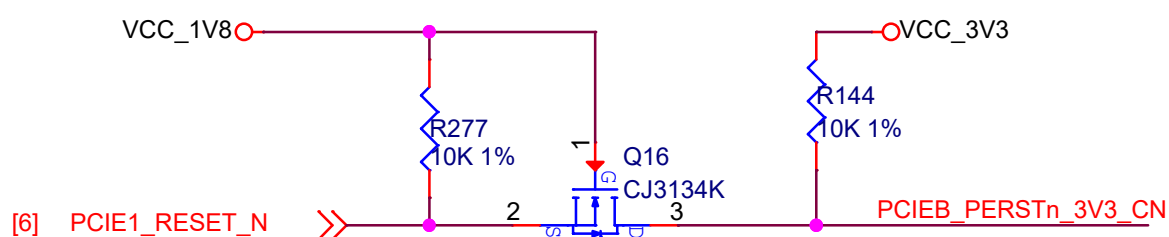
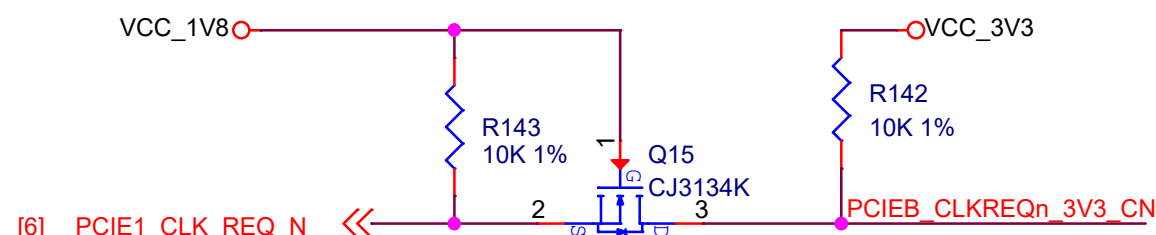
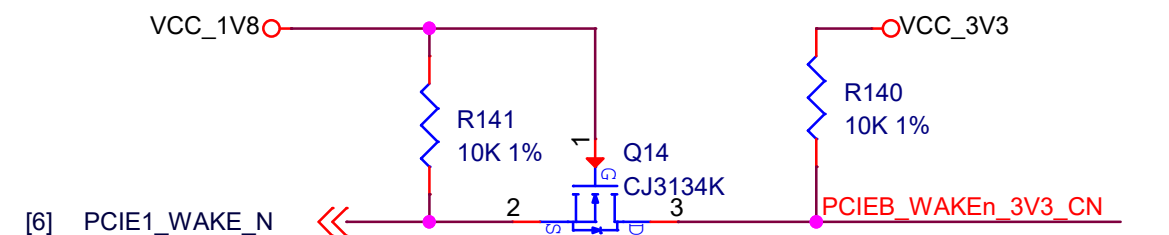
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Custom Page Name:	LCD_MIPI_EDP	V1.21
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USB2_WLAN



Size	Title: RADXA DRAGON Q6A	REV
Custom Page Name:	WIFI	V1.21
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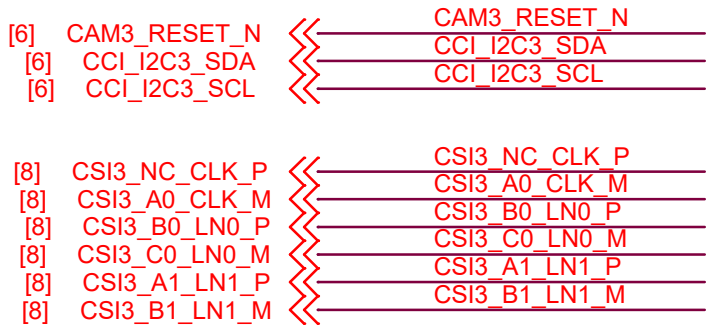
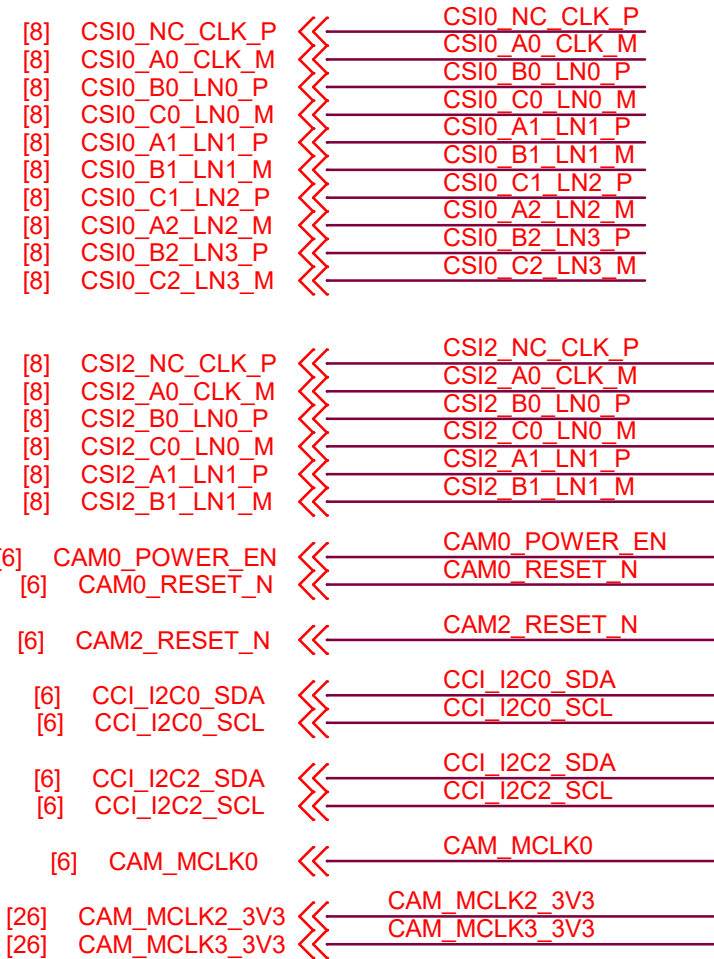
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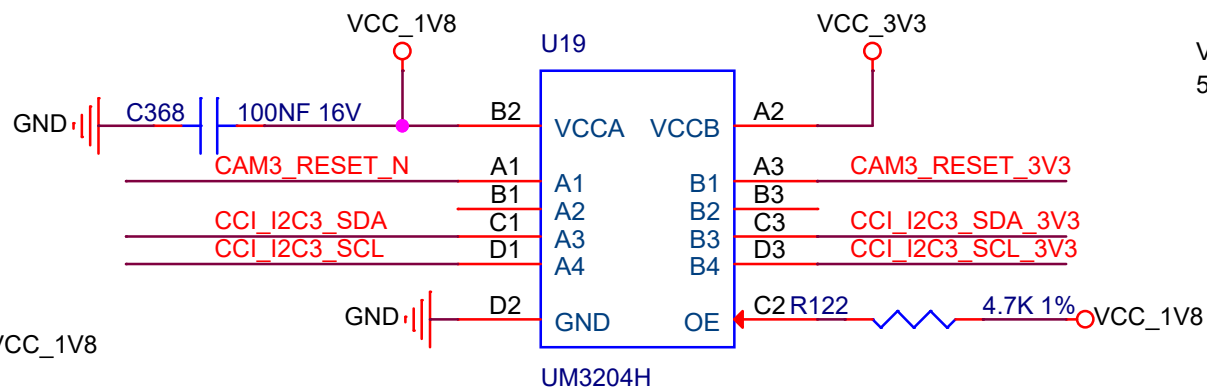
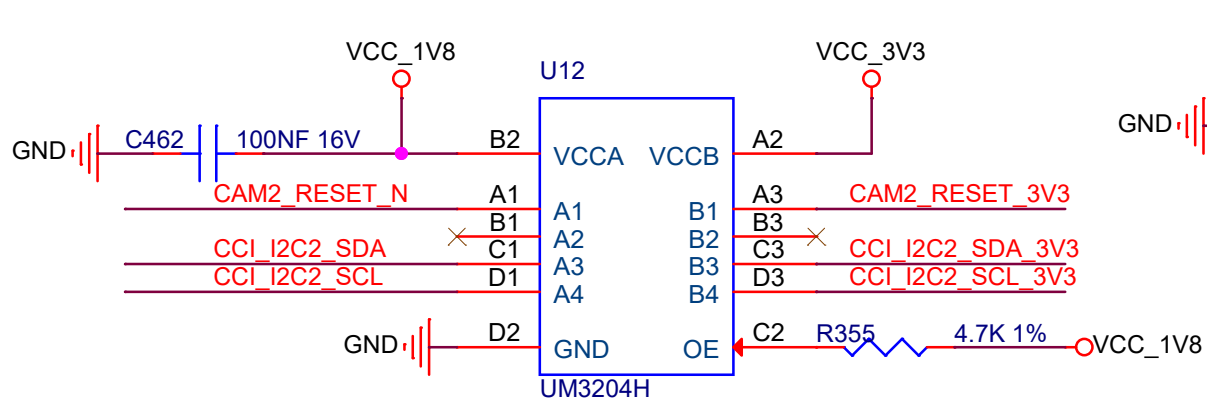
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Date:	Friday, September 12, 2025		Sheet	33	of 37

CSI0 C-PHY/D-PHY

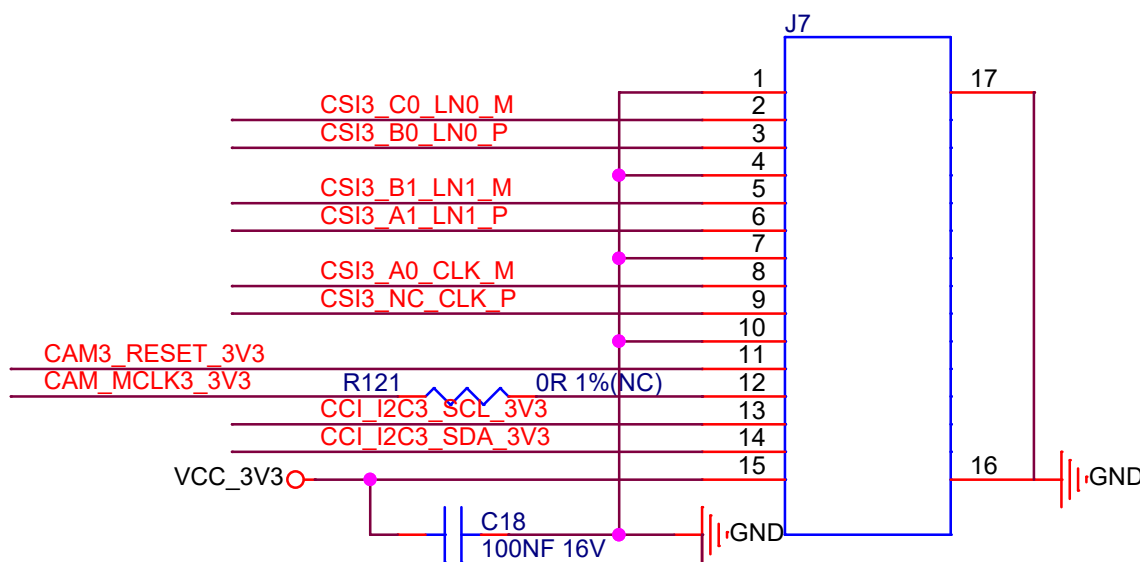
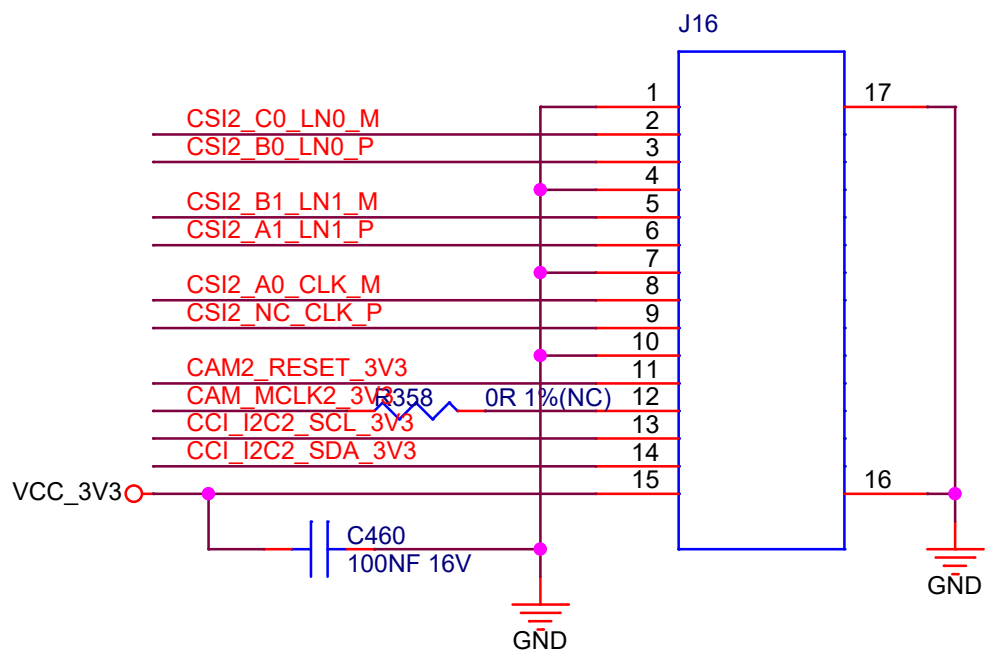
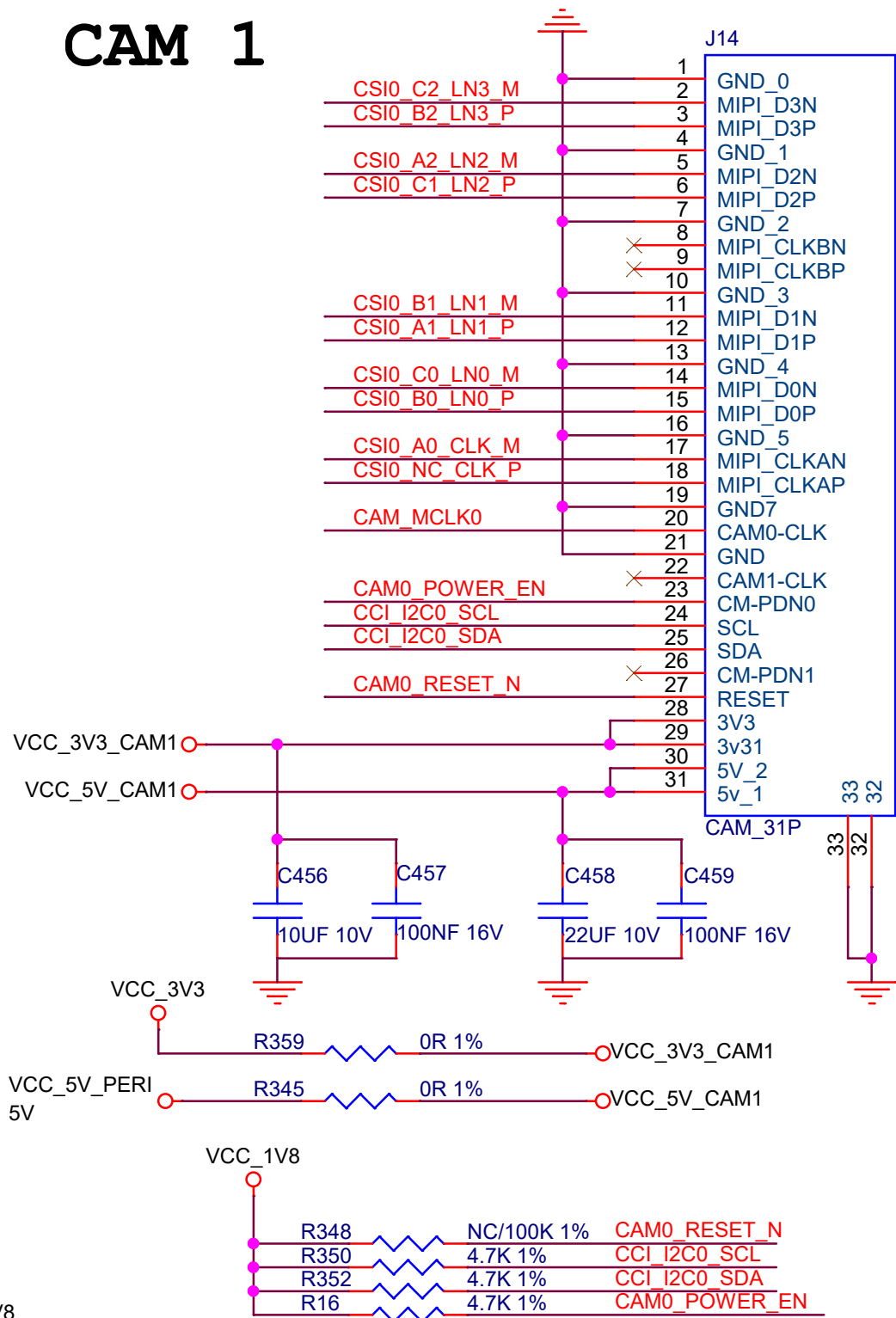
(WIDE)



CSI1 C-PHY/D-PHY

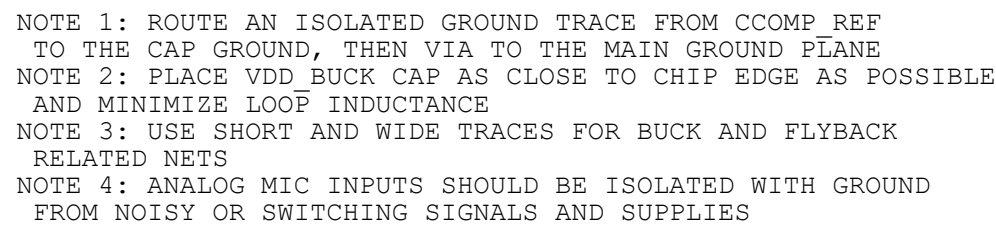


CAM 1

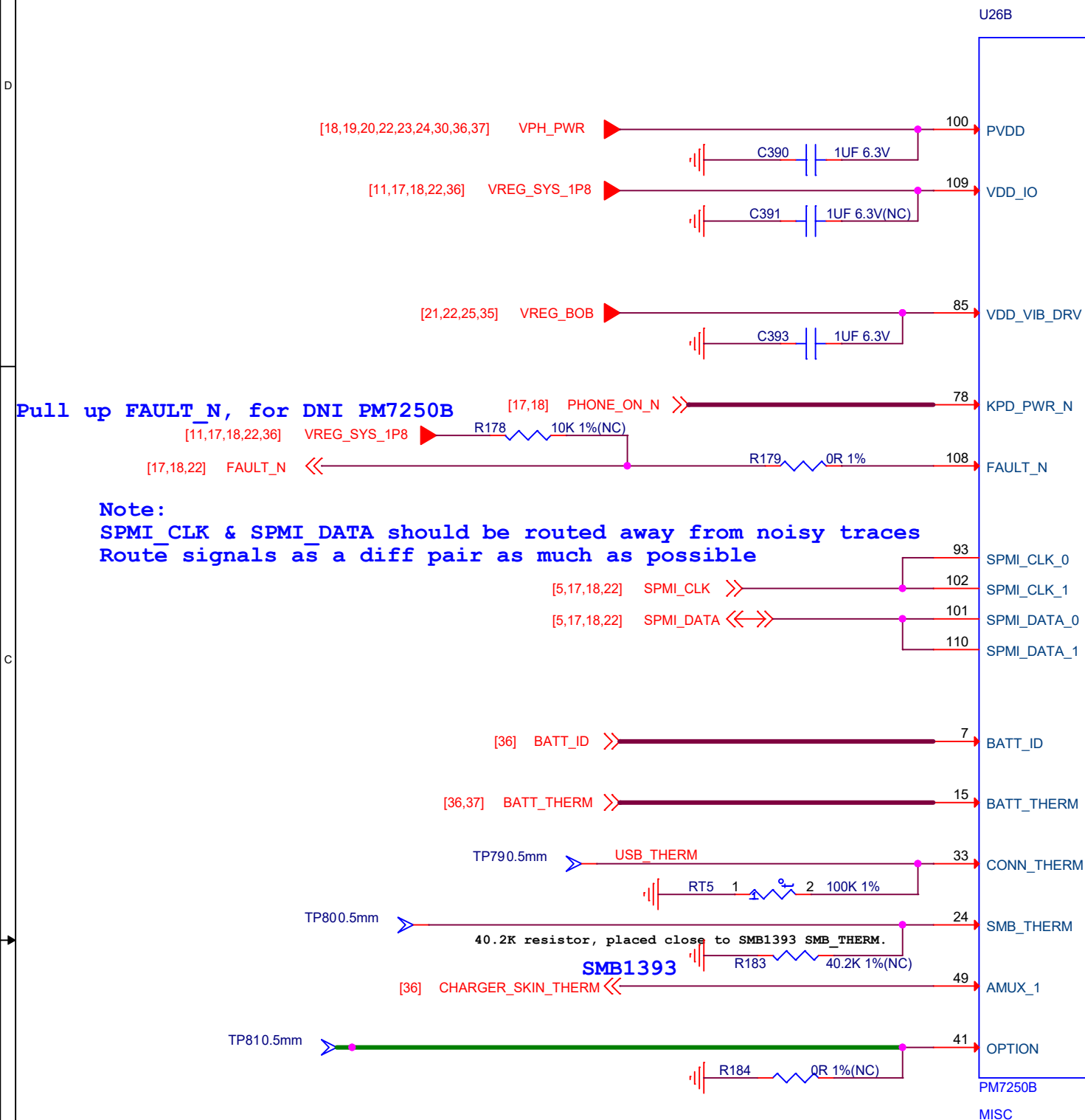


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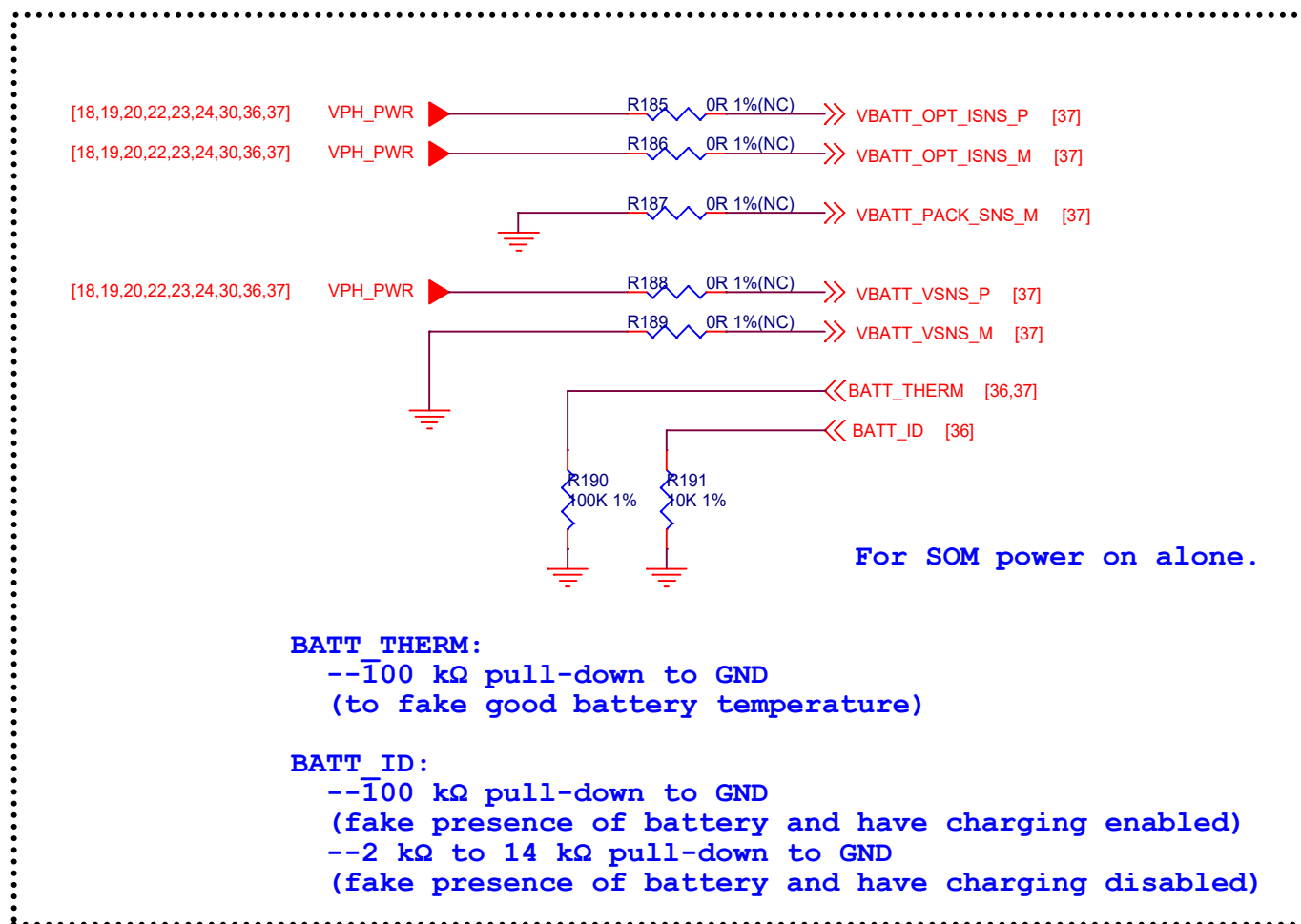
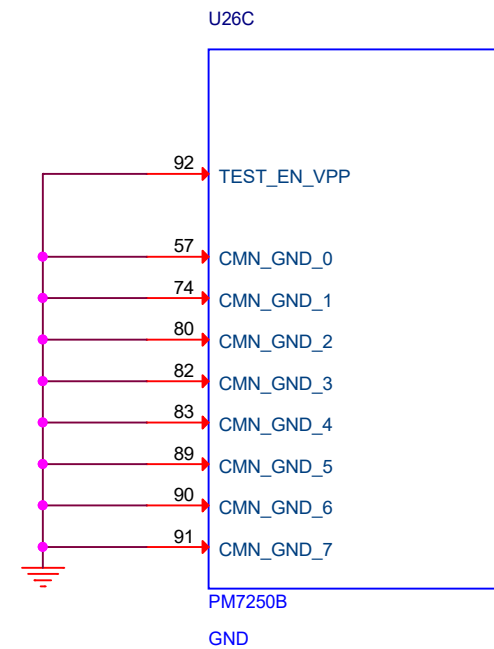
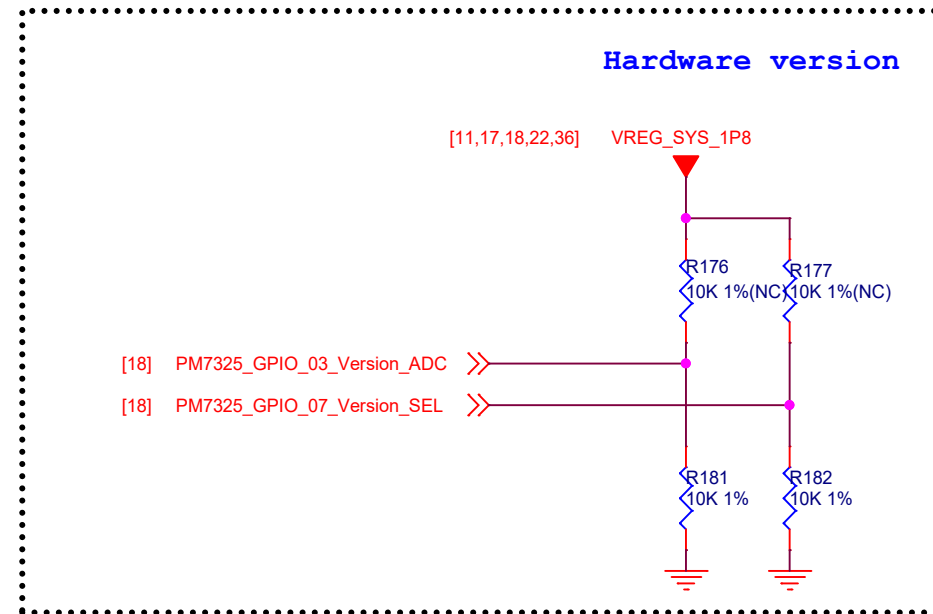
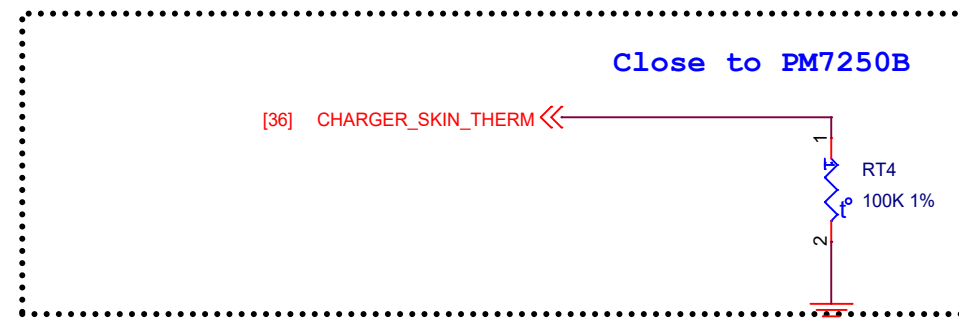
PM7250B CTRL GPIO GND



PM_OPTION:
Configuration selection for micro USB and Type-C connectors.
--DNI for Type-C and populate 0 ohm for micro USB
--Disable FMB

NOTE:
MV: VPH_PWR or 1.8 V
LV : 1.8 V only

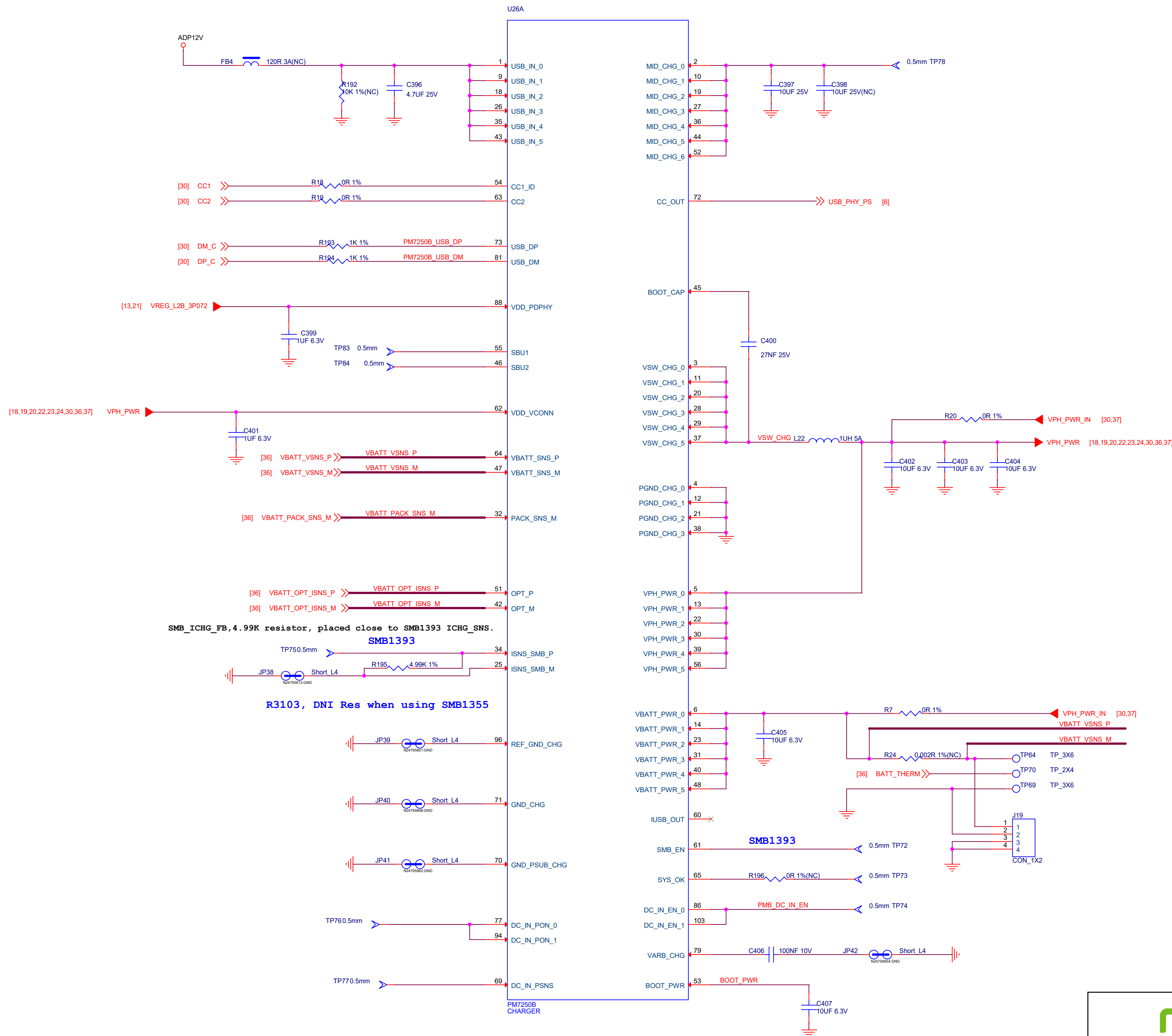
GPIO	Type	Configuration	Special function for QCM6490
1	LV	AMUX	I2C_INT
2	LV		DISPLAY_BIAS_DRIVER_EN
3	LV		KYPD_HOME
4	LV		
5	MV	AMUX	mmW monitor
6	MV		SMB_STAT
7	MV		
8	MV	AMUX	camera temperature
9	LV		Factory mode boot 1
10	LV		Factory mode boot 2
11	LV	AMUX	
12	LV	AMUX	mmW monitor



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PM7250B CHG FG



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