

54321

VERSION HISTORY

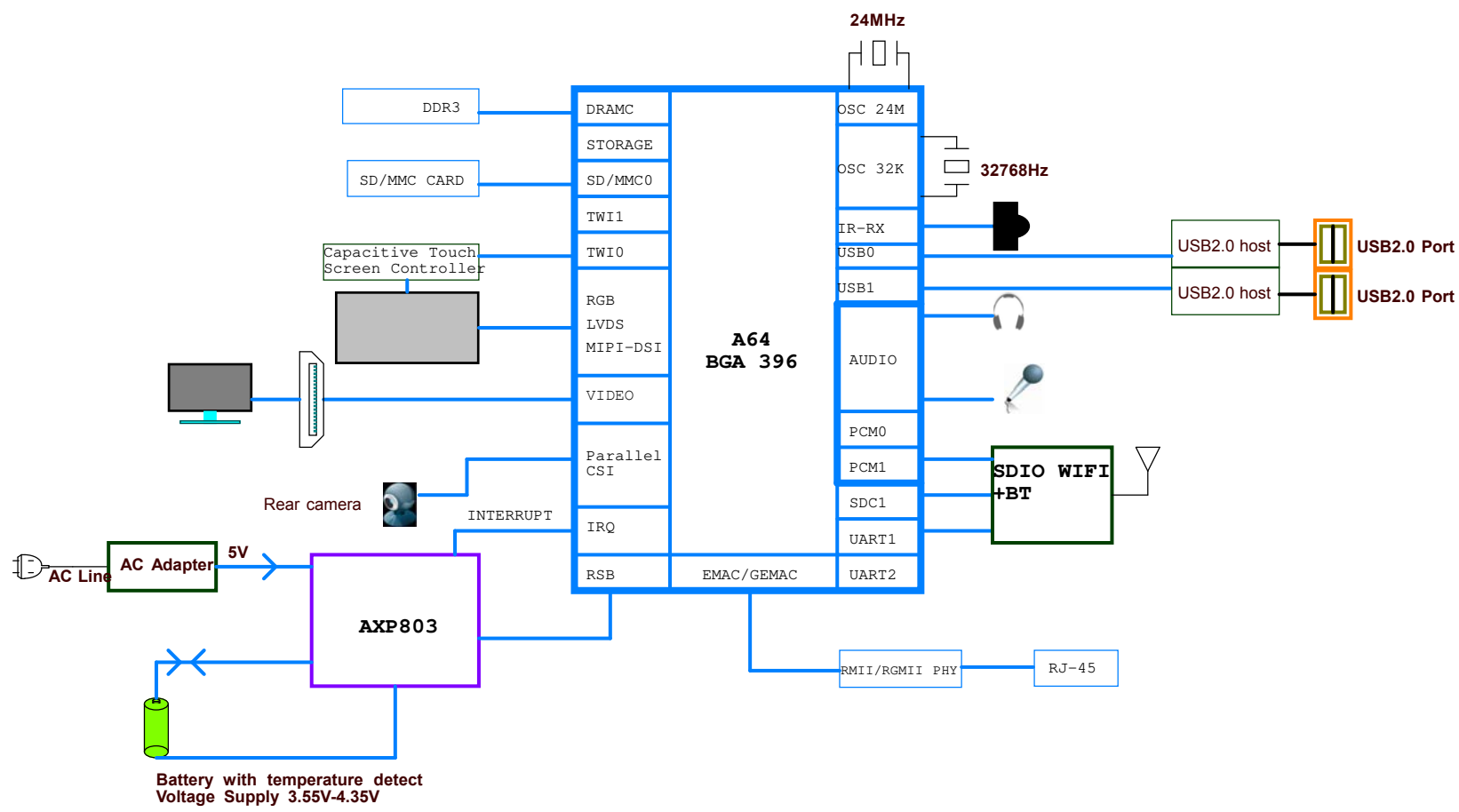
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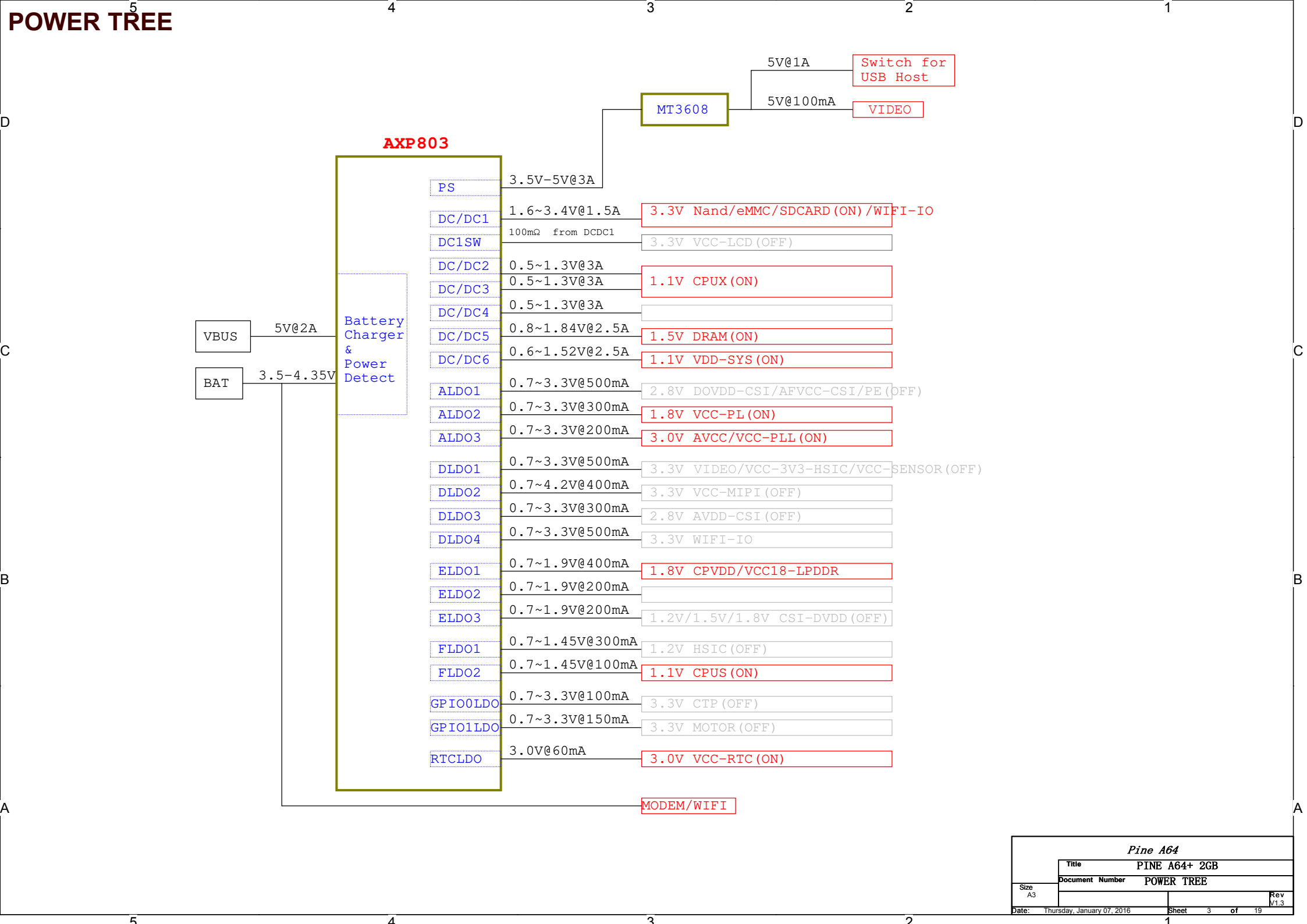
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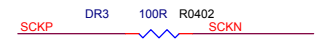
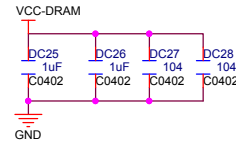
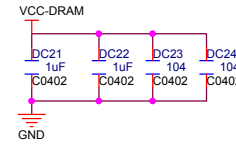
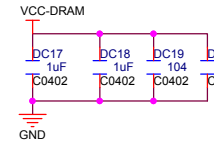
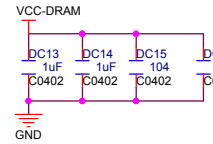
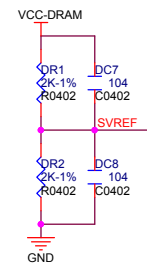
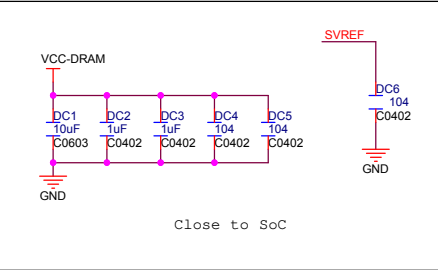
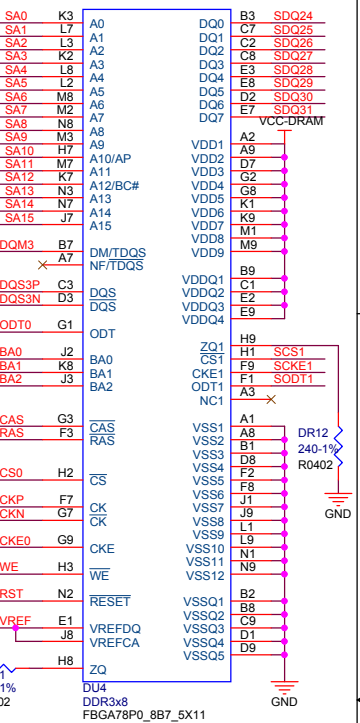
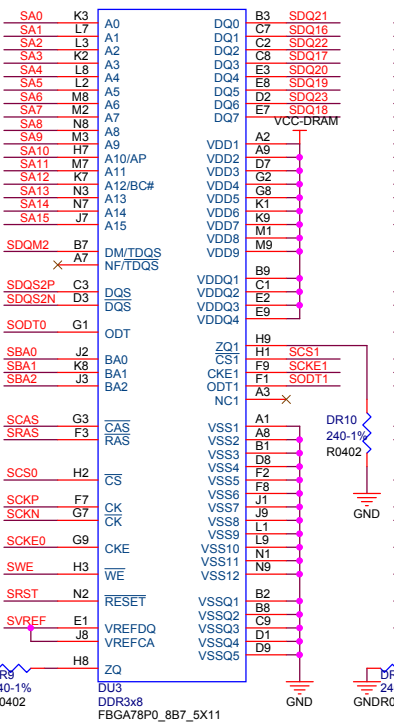
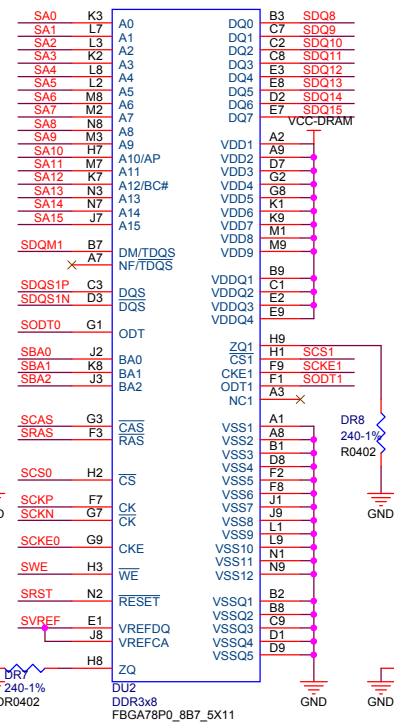
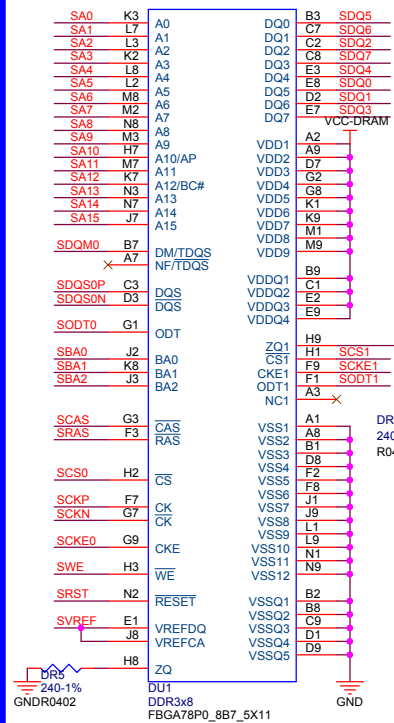
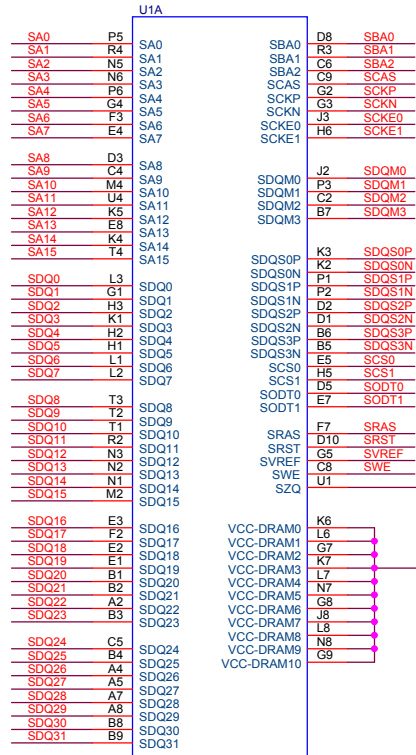
Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Release version	2015-04-22			
Ver 1.3	Added USB port power option	2016-01-13			

BLOCK DIAGRAM

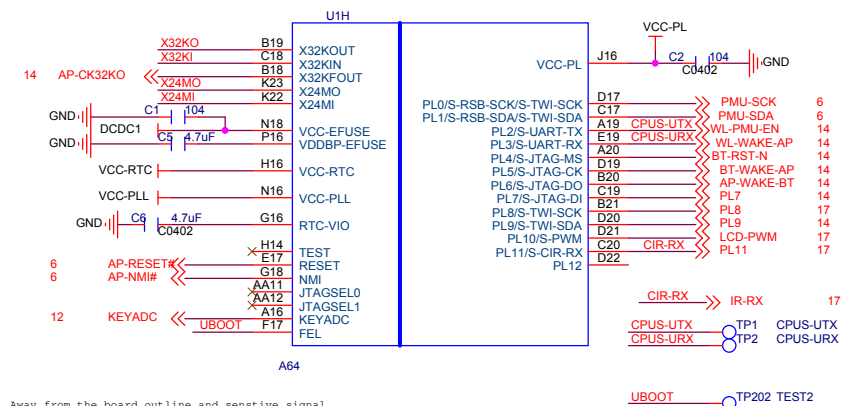




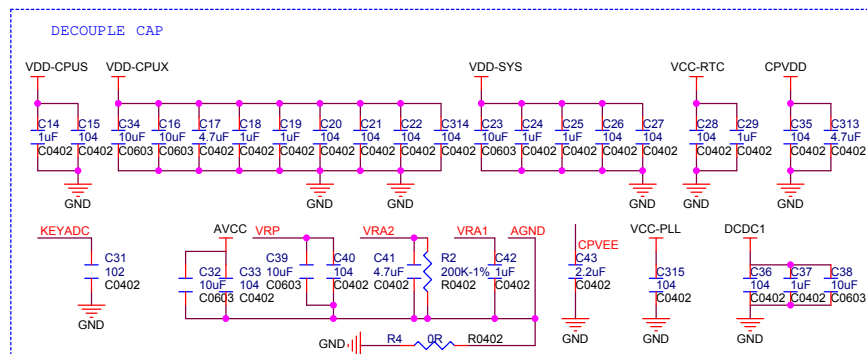
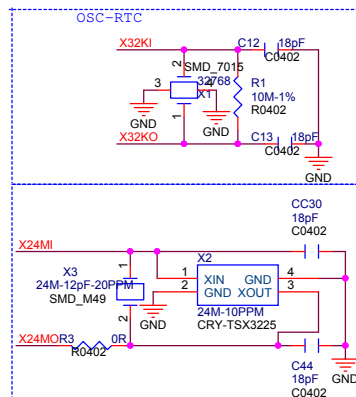
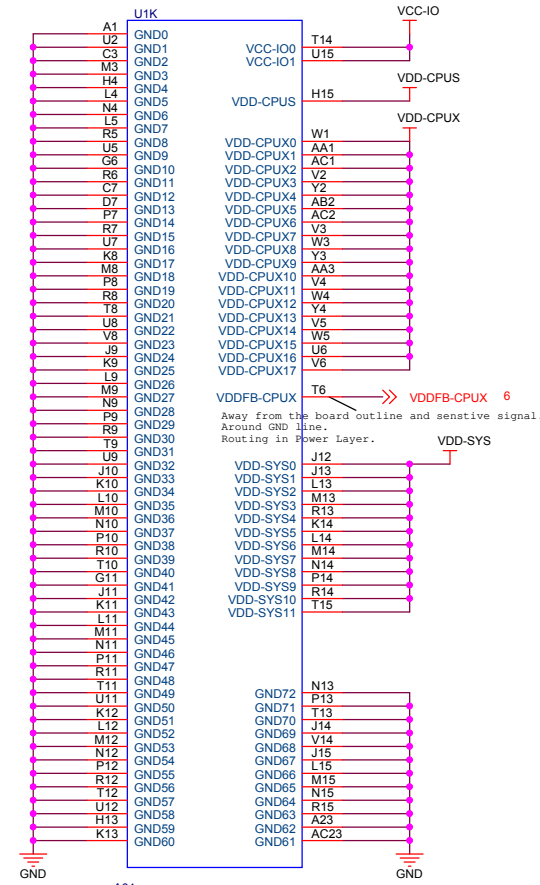
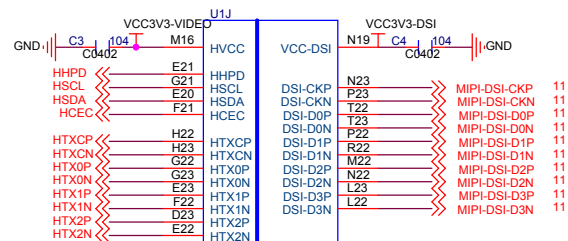
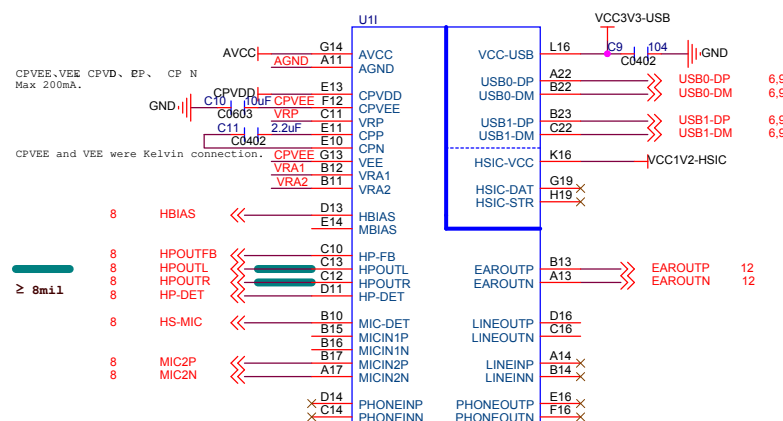
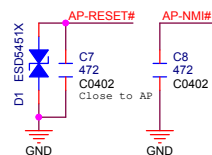
DDR3 8bx4



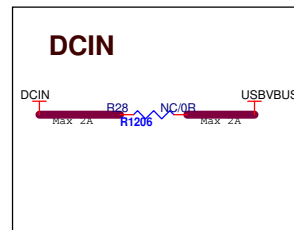
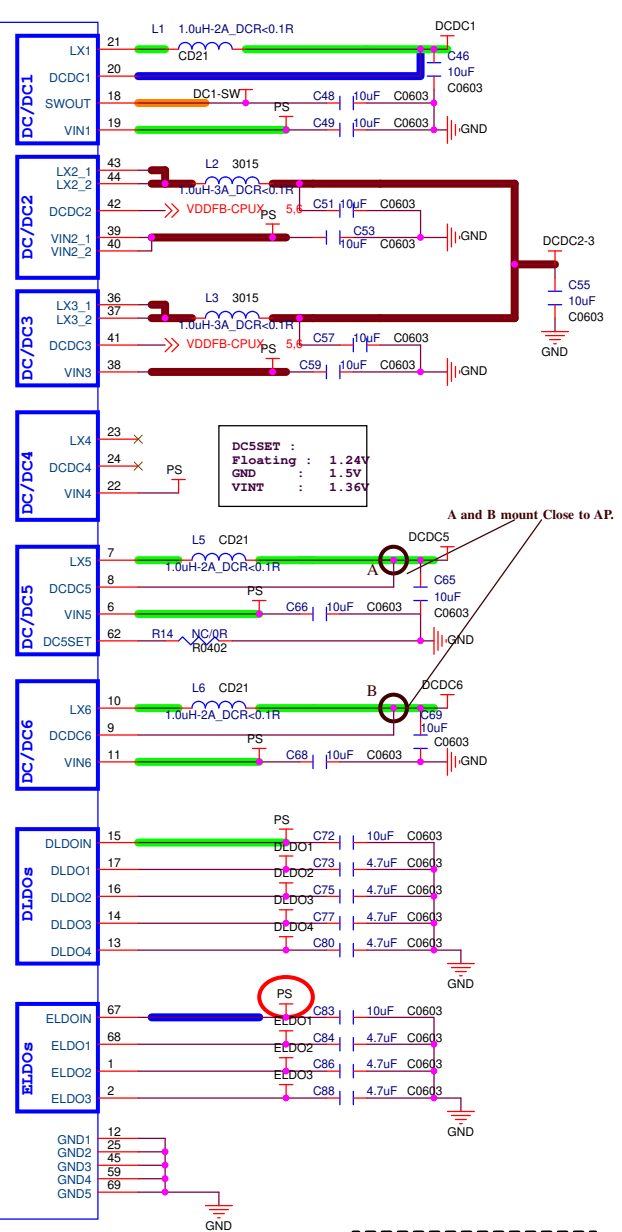
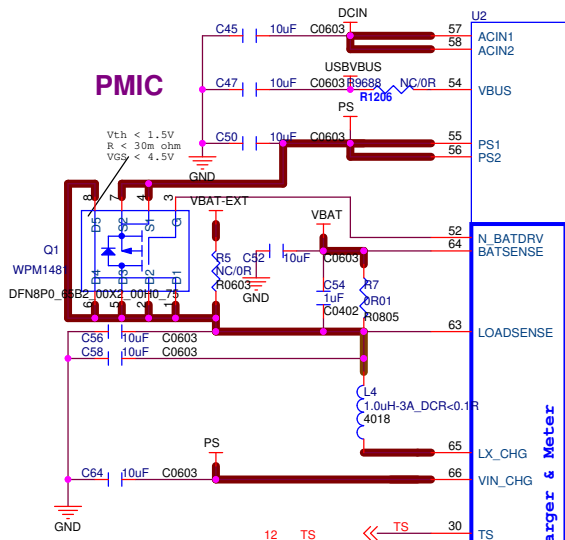
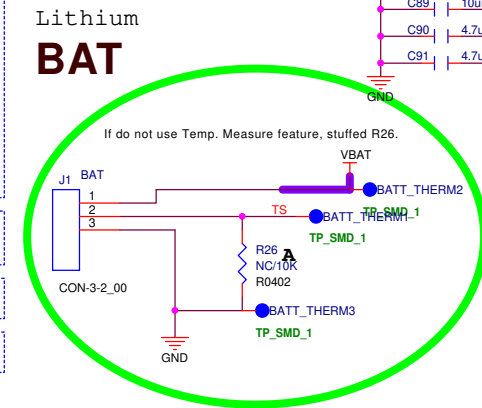
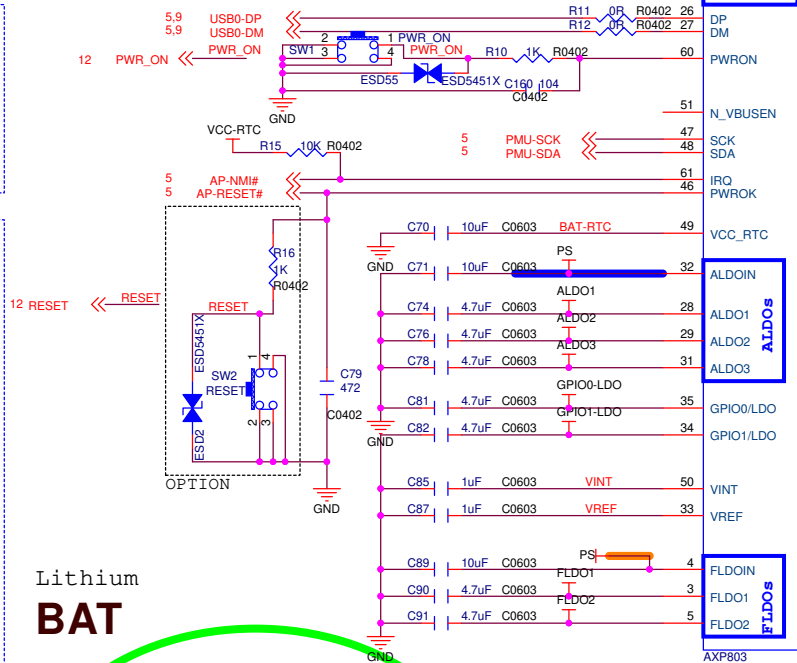
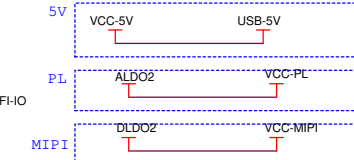
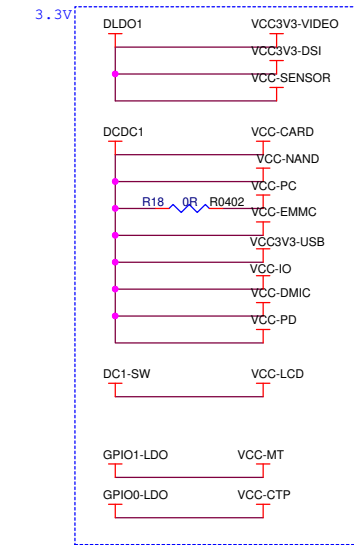
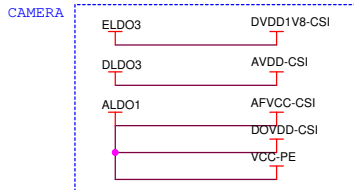
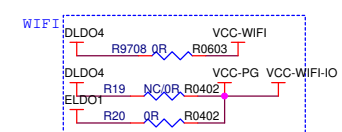
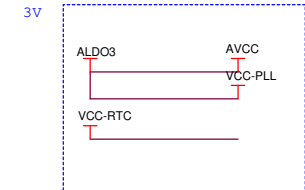
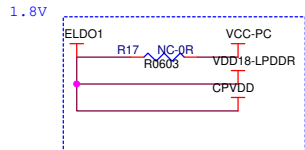
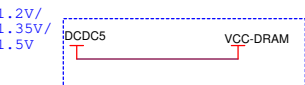
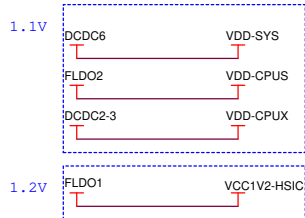
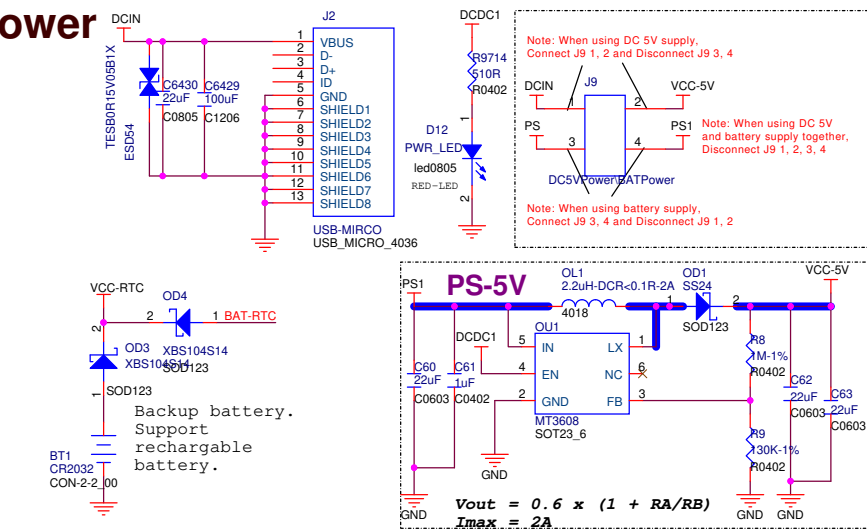
CPU



Away from the board outline and sensitive signal.
Around GND line.

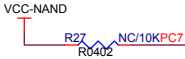
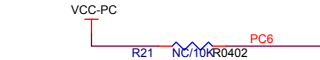
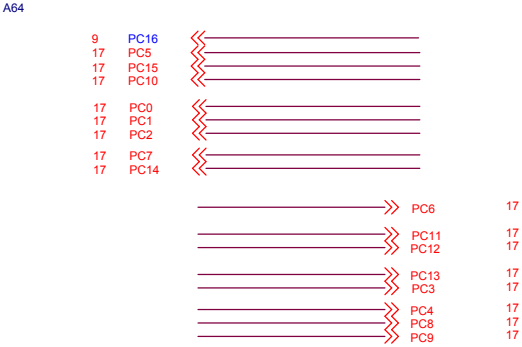
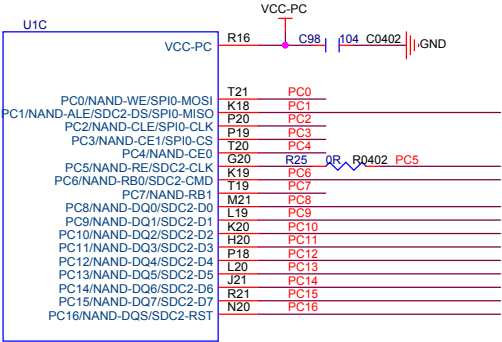


Power



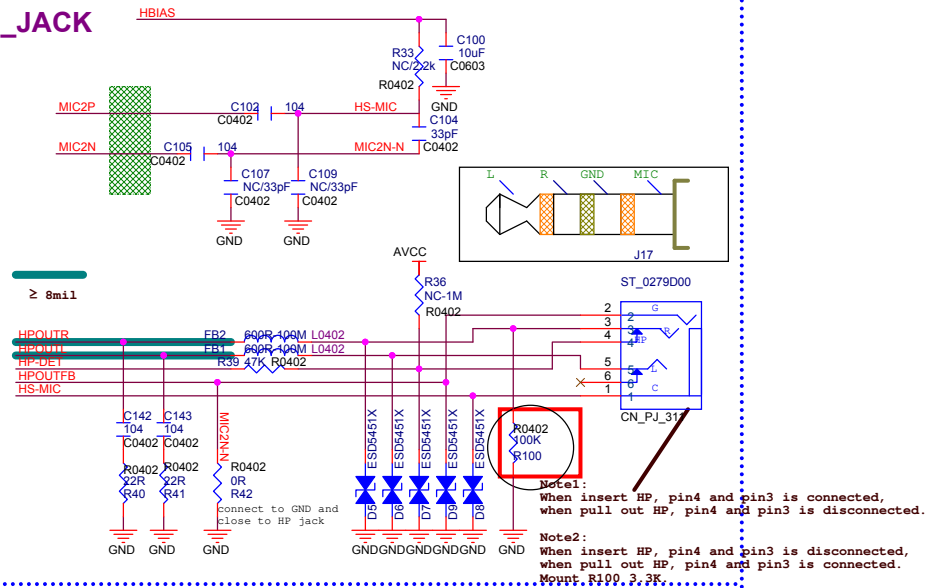
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				Title PINE A64+ 2GB			
				Document Number POWER			
Size A3				Rev V1.3			
Date: Wednesday, January 13, 2016				Sheet 6 of 19			

NAND/eMMC



AUDIO

HP_JACK



5 HBIAS << _____

5 HP-DET << _____

5 HPOUTL << _____

5 HPOUTR << _____

5 MIC2N << _____

5 MIC2P << _____

5 HS-MIC << _____

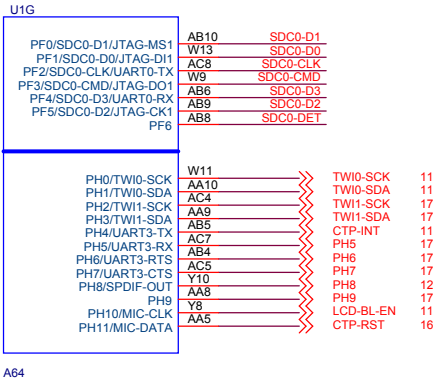
5 EAROUTP << _____

5 EAROUTN << _____

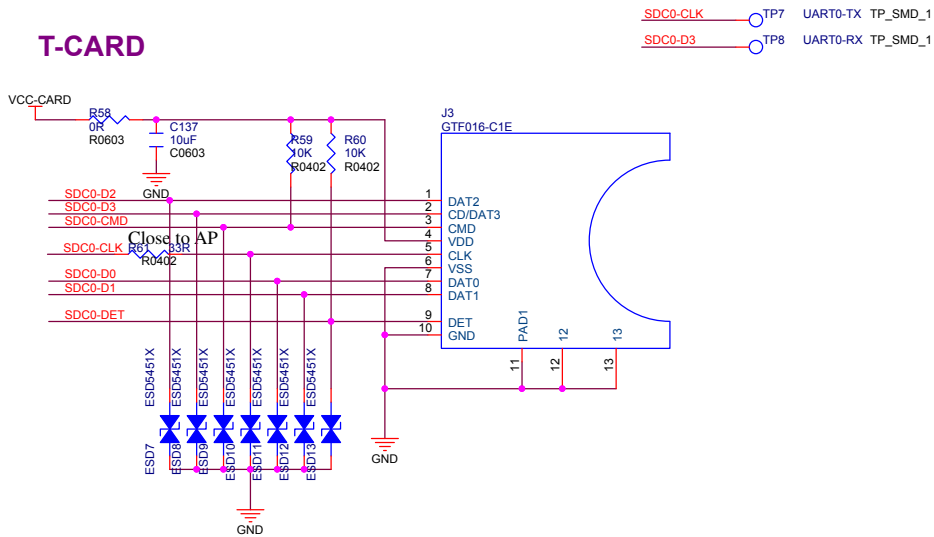
AVCC _____

VCC-5V _____

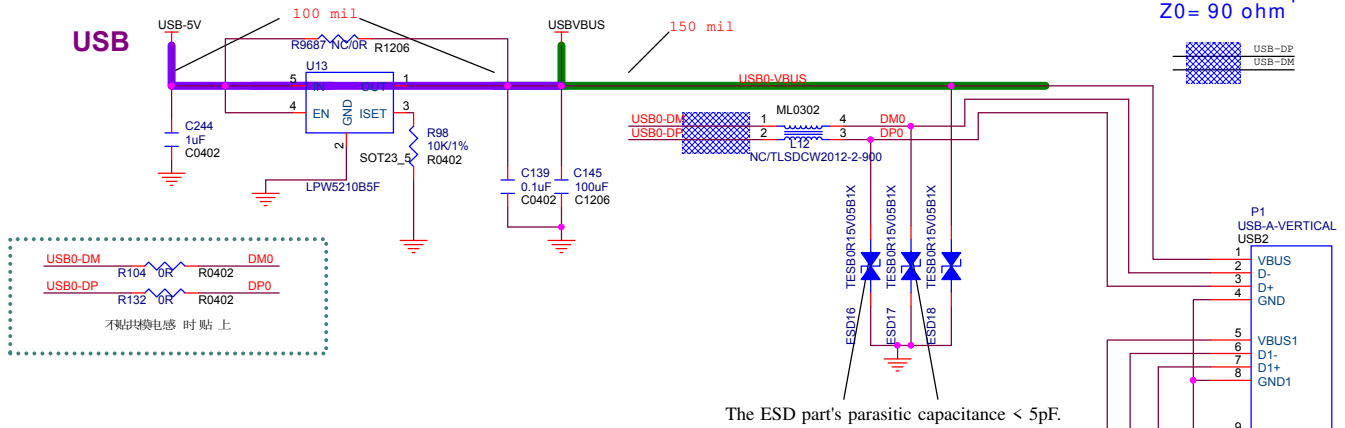
T-CADD/USB



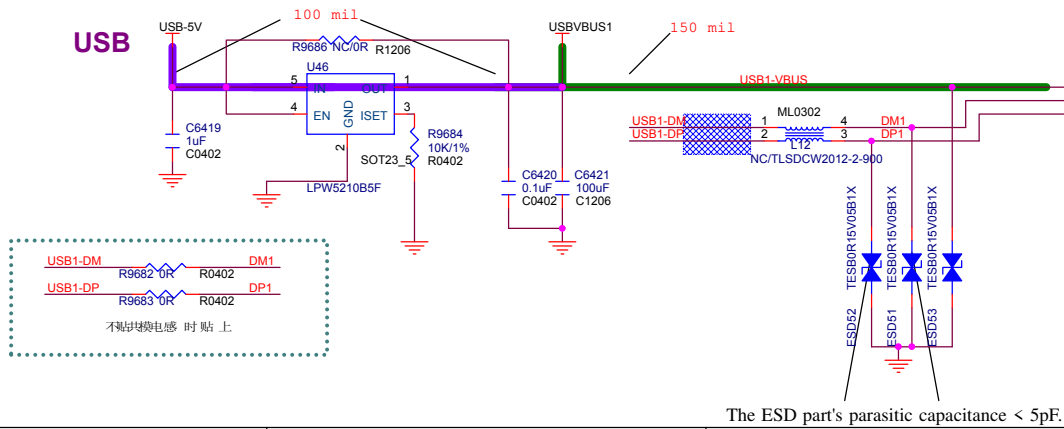
T-CARD



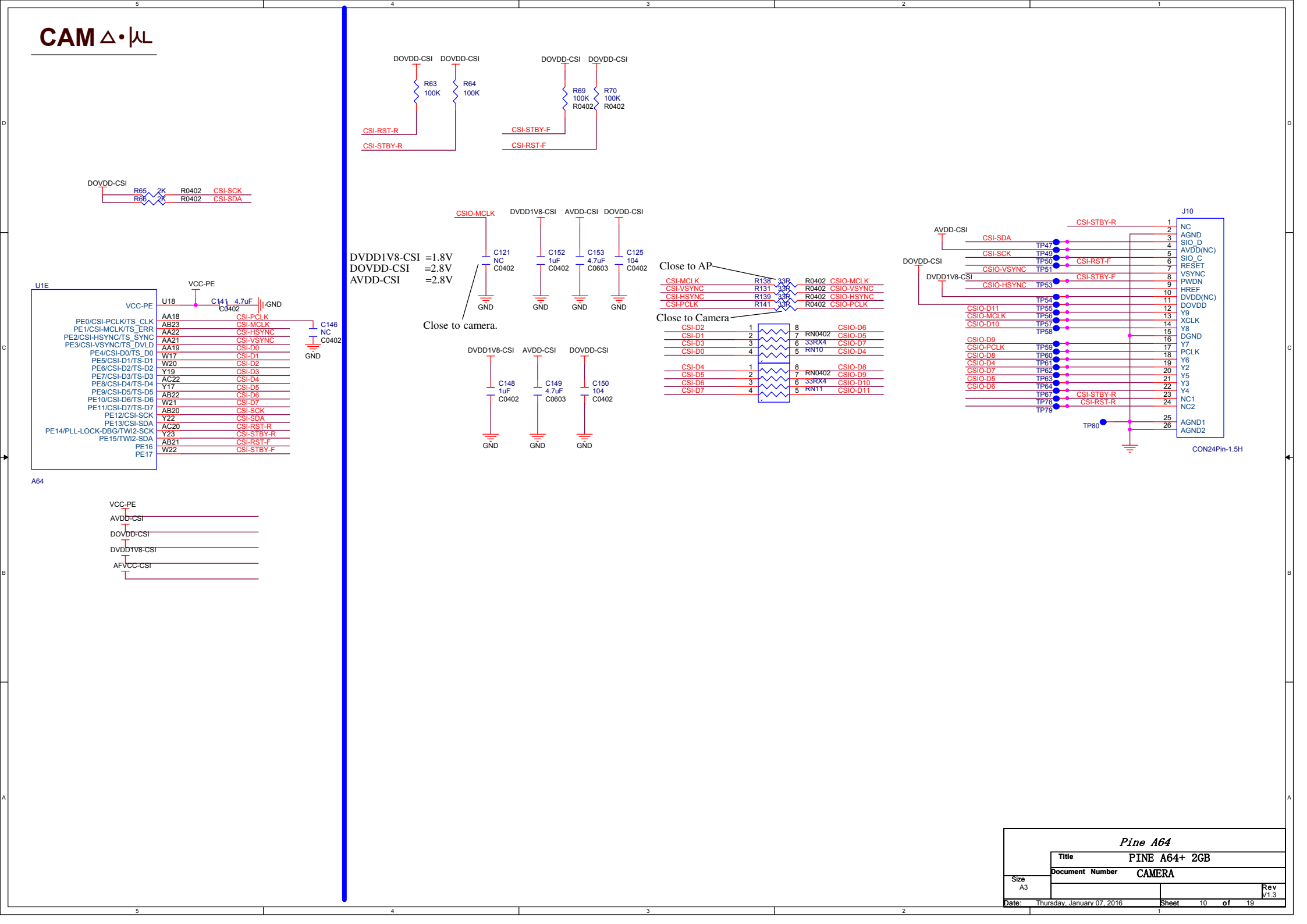
USB



USB



Pine A64			
Title		PINE A64+ 2GB	
Document Number		T-CARD/USB	
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[illegible]

CAM $\Delta \cdot \mu L$

U1E

VCC-PE

PE0/CSI-PCLK/TS_CLK
PE1/CSI-MCLK/TS_ERR
PE2/CSI-HSYNC/TS_SYNC
PE3/CSI-VSYNC/TS_DVLD
PE4/CSI-D0/TS_D0
PE5/CSI-D1/TS-D1
PE6/CSI-D2/TS-D2
PE7/CSI-D3/TS-D3
PE8/CSI-D4/TS-D4
PE9/CSI-D5/TS-D5
PE10/CSI-D6/TS-D6
PE11/CSI-D7/TS-D7
PE12/CSI-SCK
PE13/CSI-SDA
PE14/PLL-LOCK-DBG/TWI2-SCK
PE15/TWI2-SDA
PE16
PE17

AA18
AA22
AA21
AA19
W17
W20
Y19
AC22
Y17
AB22
W21
AB20
Y22
AC20
Y23
AB21
W22

CSI-PCLK
CSI-MCLK
CSI-HSYNC
CSI-VSYNC
CSI-D0
CSI-D1
CSI-D2
CSI-D3
CSI-D4
CSI-D5
CSI-D6
CSI-D7
CSI-SCK
CSI-SDA
CSI-RST-R
CSI-STBY-R
CSI-RST-F
CSI-STBY-F

C141 4.7uF
C146 NC
C0402

A64

VCC-PE
AVDD-CSI
DOVDD-CSI
DVDD1V8-CSI
AFVCC-CSI

DOVDD-CSI
R63 100K
R64 100K
CSI-RST-R
CSI-STBY-R

DOVDD-CSI
R69 100K
R70 100K
R0402
R0402
CSI-STBY-F
CSI-RST-F

DVDD1V8-CSI = 1.8V
DOVDD-CSI = 2.8V
AVDD-CSI = 2.8V

CSI-MCLK
C121 NC
C0402
Close to camera.

DVDD1V8-CSI
C148 1uF
C0402
GND

AVDD-CSI
C149 4.7uF
C0603
GND

DOVDD-CSI
C150 104
C0402
GND

Close to AP

CSI-MCLK
R138 33P
R131 33P
R139 33P
R141 33P
R0402
R0402
R0402
R0402
CSI-MCLK
CSI-VSYNC
CSI-HSYNC
CSI-PCLK

Close to Camera

CSI-D2
CSI-D1
CSI-D3
CSI-D0
CSI-D4
CSI-D5
CSI-D6
CSI-D7

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RN0402
33RX4
RN10
RN0402
33RX4
RNT1
CSI-D6
CSI-D5
CSI-D4
CSI-D3
CSI-D2
CSI-D1
CSI-D0
CSI-D7
CSI-D6
CSI-D5
CSI-D4
CSI-D3
CSI-D2

AVDD-CSI
DOVDD-CSI
DVDD1V8-CSI

TP47
TP49
TP50
TP51
TP53
TP54
TP55
TP56
TP57
TP58
TP59
TP60
TP61
TP62
TP63
TP64
TP67
TP79

CSI-SDA
CSI-SCK
CSI-VSYNC
CSI-HSYNC
CSI-D11
CSI-MCLK
CSI-D10
CSI-D9
CSI-PCLK
CSI-D8
CSI-D4
CSI-D7
CSI-D5
CSI-D6
CSI-STBY-R
CSI-RST-R

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NC
AGND
SIO_D
AVDD(NC)
SIO_C
RESET
VSYNC
PWDN
HREF
DVDD(NC)
DOVDD
Y8
XCLK
Y9
DGND
Y7
PCLK
Y6
Y2
Y5
Y4
NC1
NC2
AGND1
AGND2

CON24Pin-1.5H

Pine A64

Title PINE A64+ 2GB

Document Number CAMERA

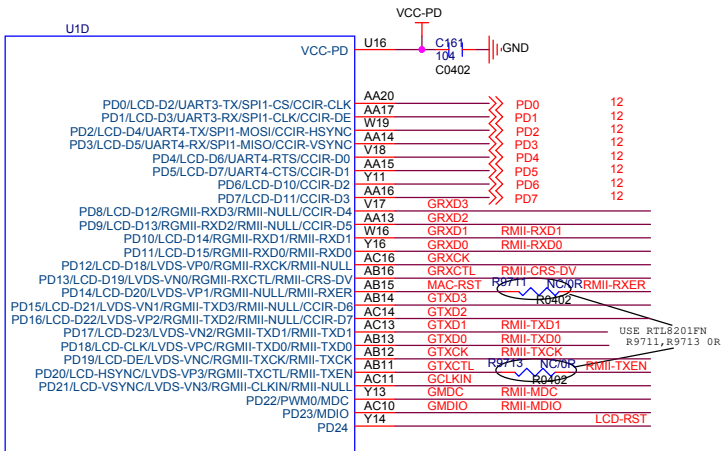
Size A3

Date: Thursday, January 07, 2016

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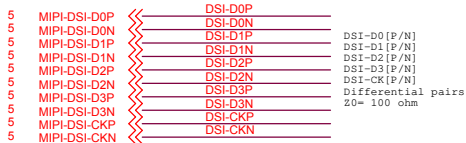
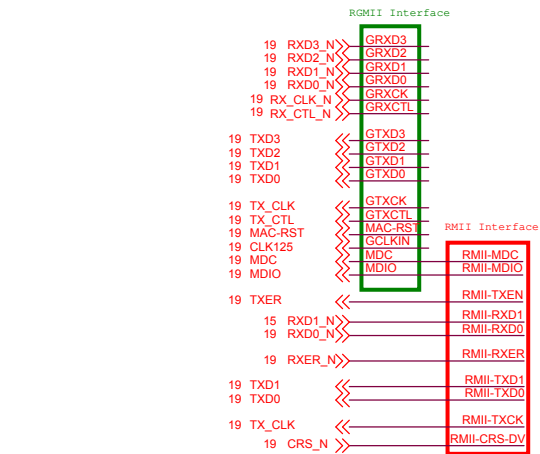
Rev V1.3

LCD

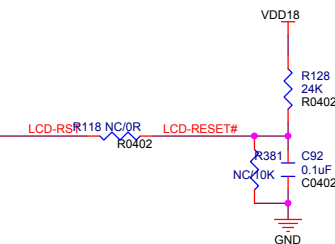
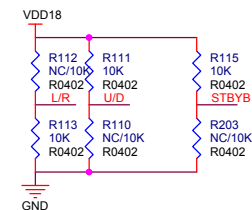
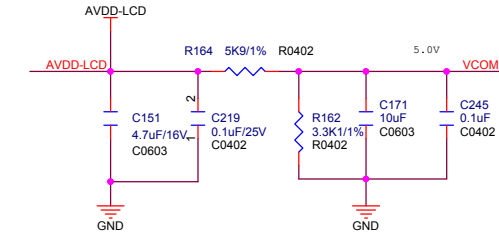


A64

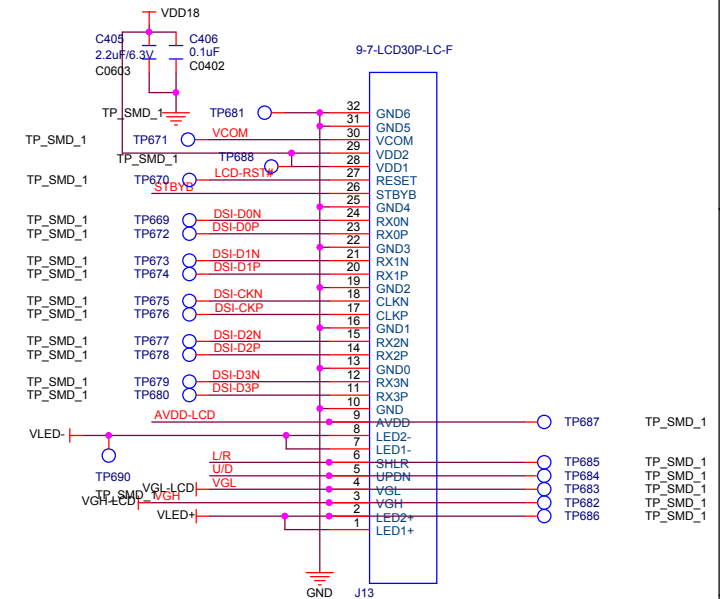
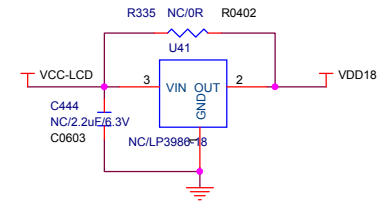
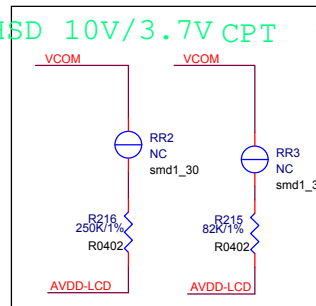
11 LCD-RST << LCD-RST



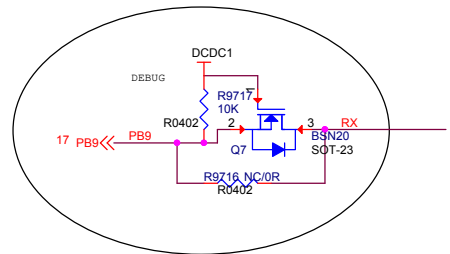
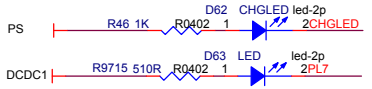
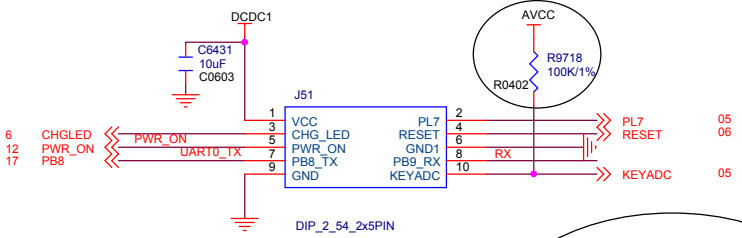
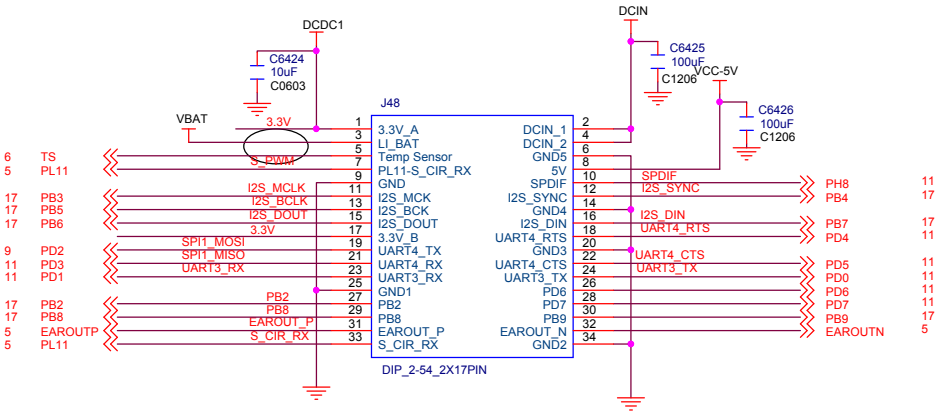
MIPI-LCD



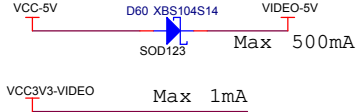
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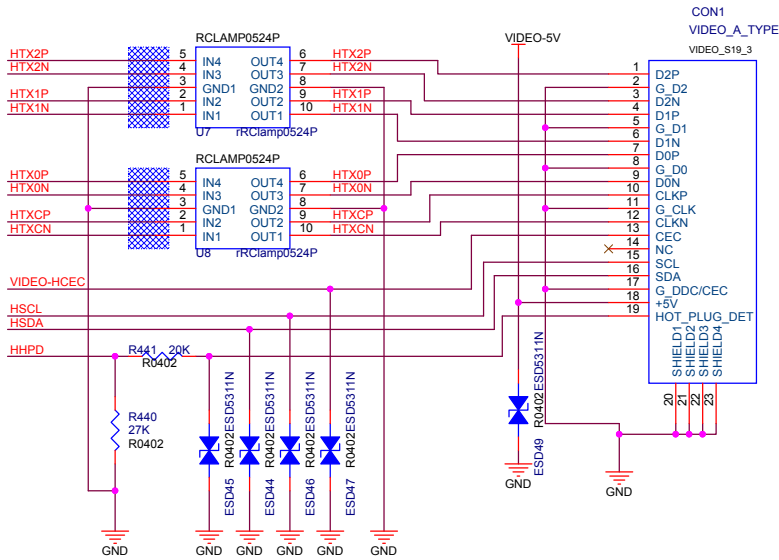
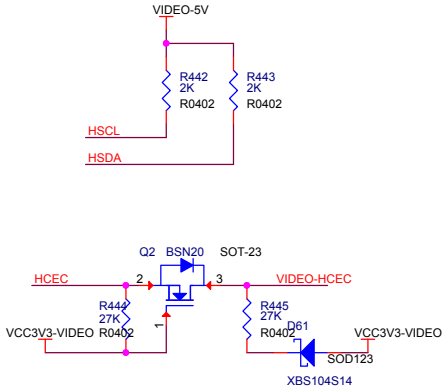
Euler bus



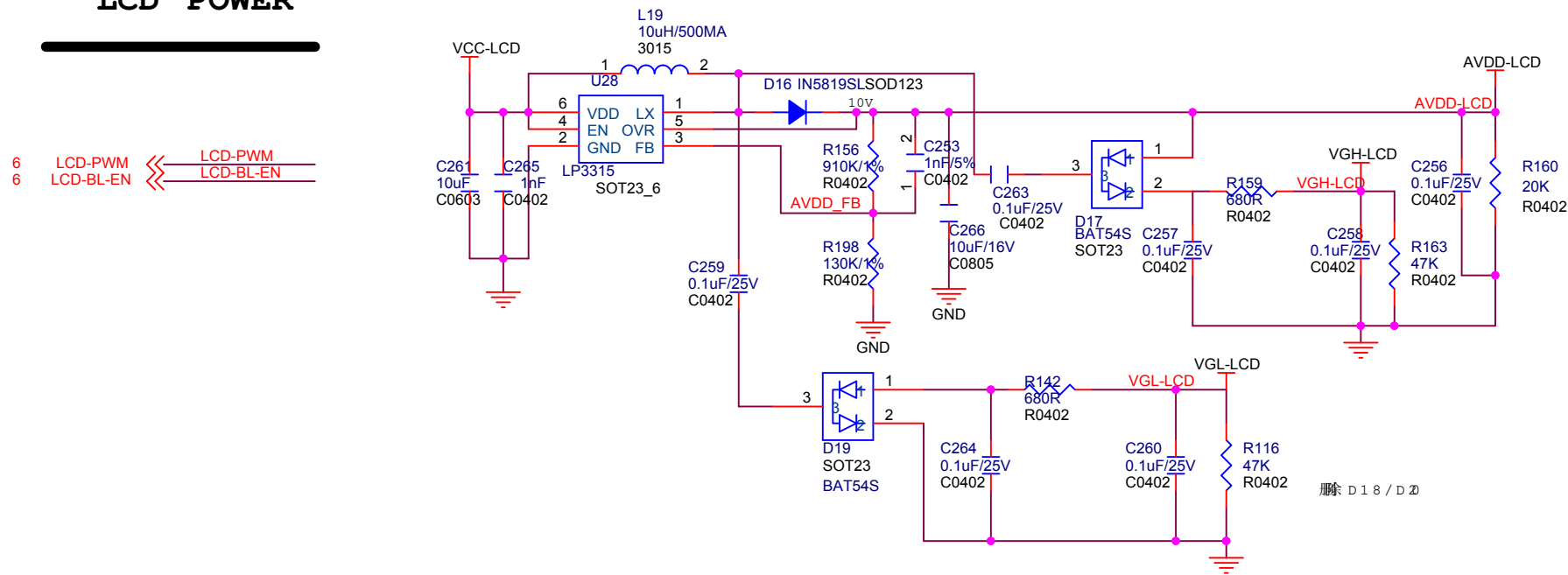
VIDEO



Differential pairs
Z0= 100 ohm

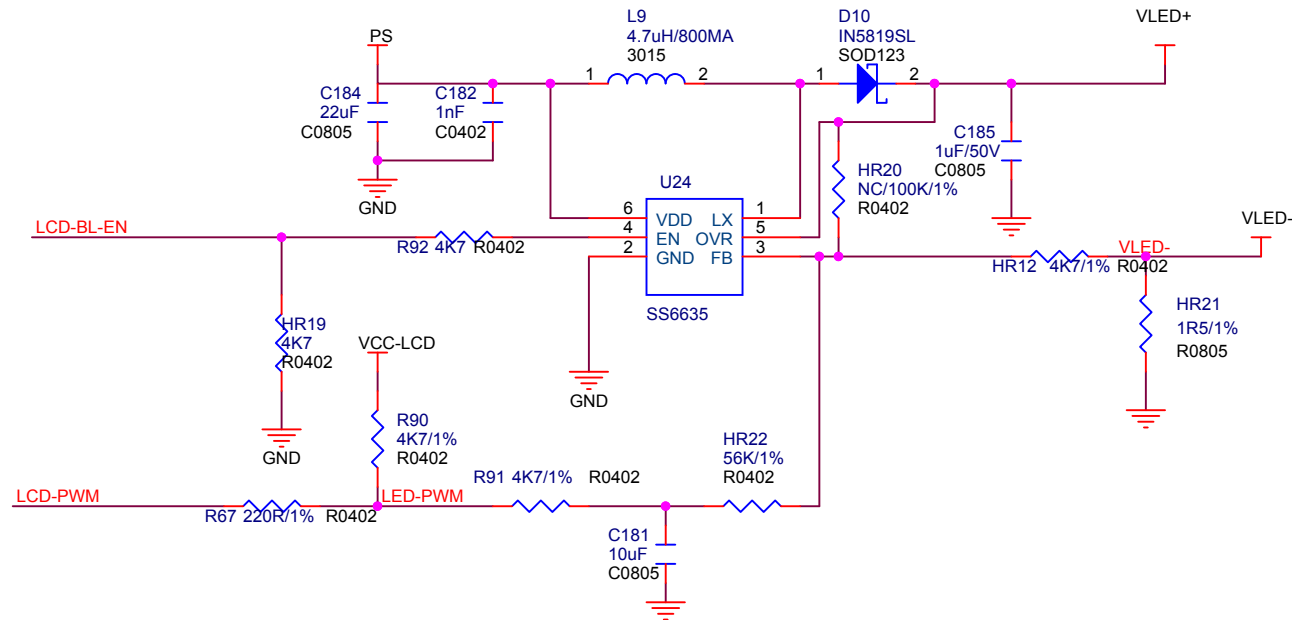


LCD POWER



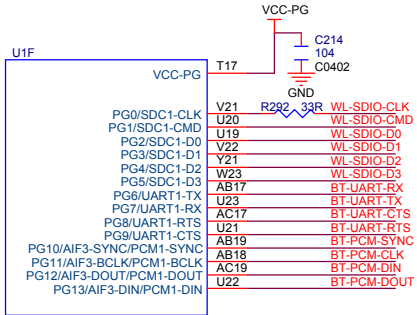
删除 D18 / D20

Backlight

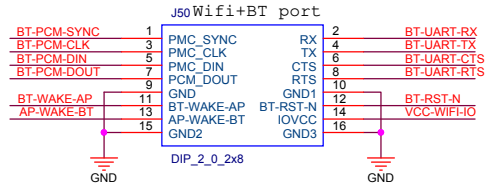
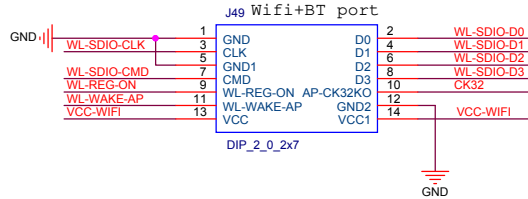
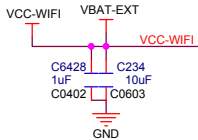
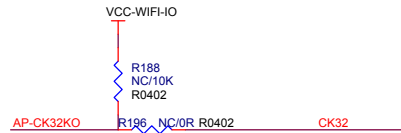
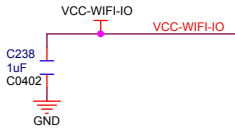
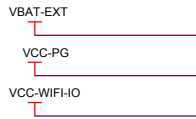
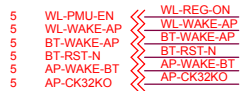


Pine A64			
Title		PINE A64+ 2GB	
Document Number		LCD POWER	
Size A4			Rev V1.3
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WIFI+BT

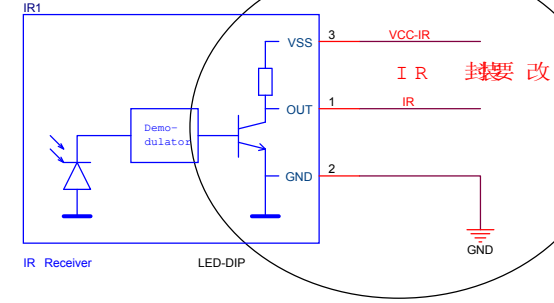
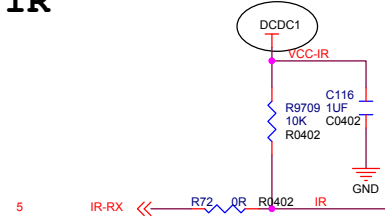


A64

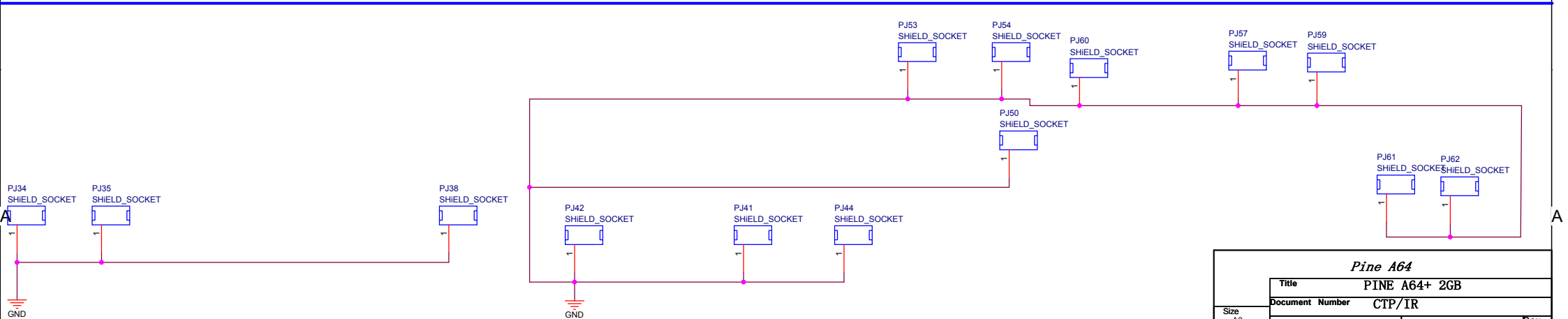
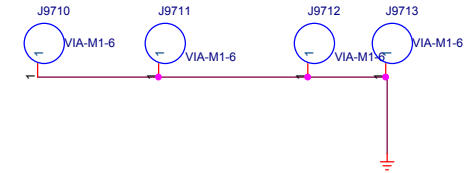
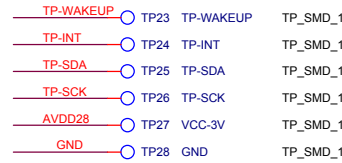
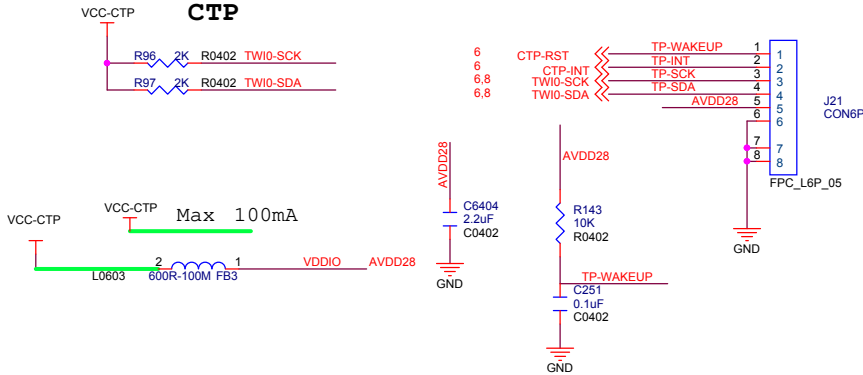


CTP

IR

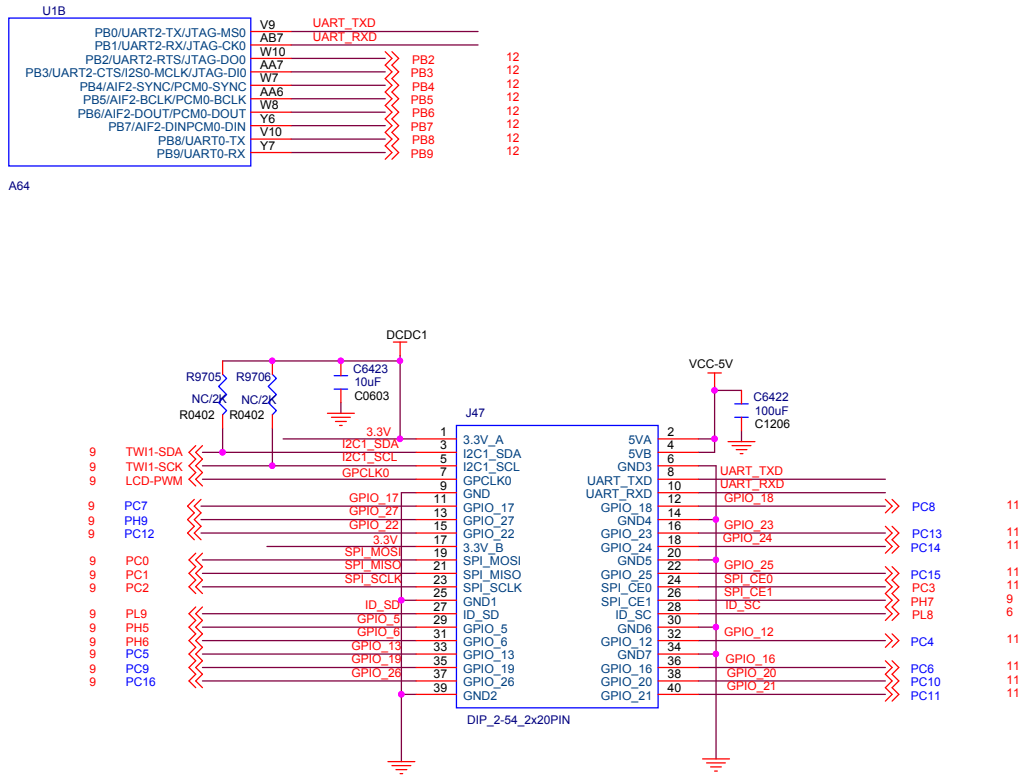


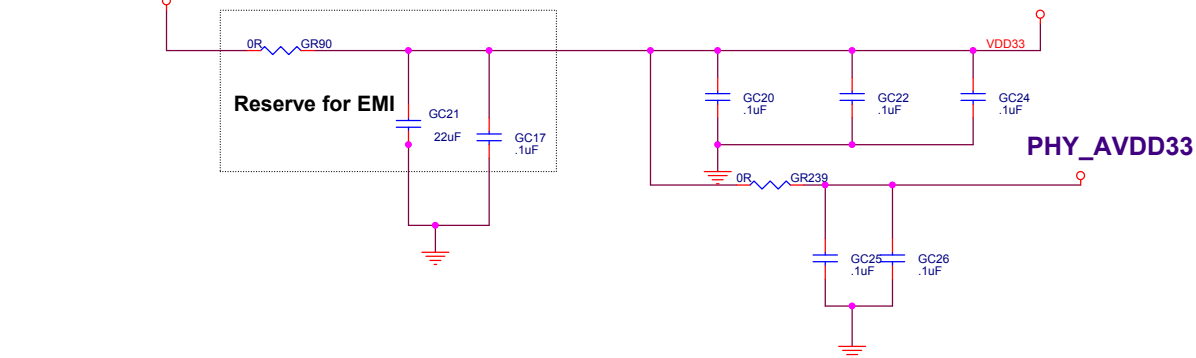
CTP



Pine A64			
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PI-2 bus





RTL8211CN/D/E	GL1	C56	U10	GR65	GR66	GR122	GC41/GC57
Enable switching regulator	○	○	✗	○	✗	✗	○
Disable switching regulator	✗	✗	○	✗	○	○	✗

Note 1: The Trace length between GL1 and Pin 48 must be within 0.5 cm. GC40 and GC41 to G L1 must be within 0.5cm.

RTL8211D/8211CN:GC40 22uF(X5R)
RTL8211E: GC40 4.7uF(X5R)

C40 close to L1



VDDREG

PHY_AVDD33

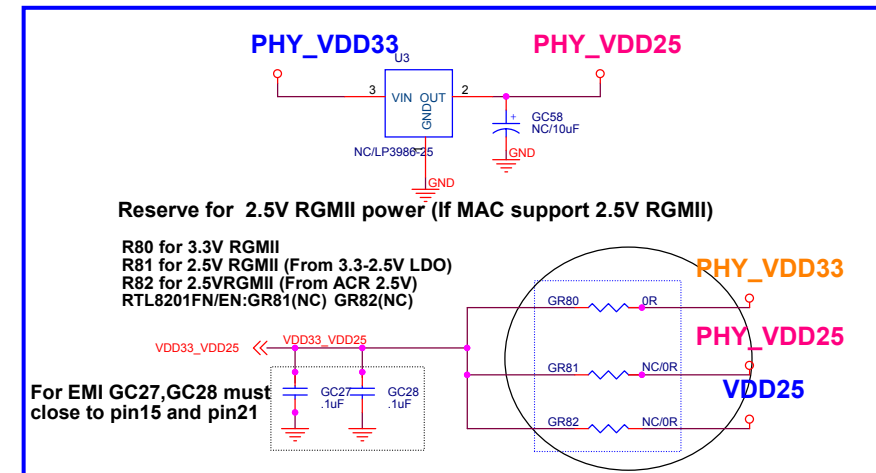
Note 2: The Trace length from C56, C57 to Pin 44,45 must be within 1 cm. The trace width from PHY_AVDD33 to Pin 44,45 should >40mils

RTL8201FN/EN:GC56(NC),GC57(NC),GR146(NC)
RTL8211CN/8211D: GC56 22uF(X5R)
RTL8211E: GC56 4.7uF(X5R)

External Power Source

U10,GC69,GC68, GR122,GR120 and GR121 are only used by 8211CN/8211D/8211E application when switching regulator is disabled. For other applications, please remove them.

RESERVE



Reserve for 2.5V RGMII power (If MAC support 2.5V RGMII)

R80 for 3.3V RGMII
R81 for 2.5V RGMII (From 3.3-2.5V LDO)
R82 for 2.5VRGMII (From ACR 2.5V)
RTL8201FN/EN:GR81(NC) GR82(NC)

For EMI GC27,GC28 must
close to pin15 and pin21

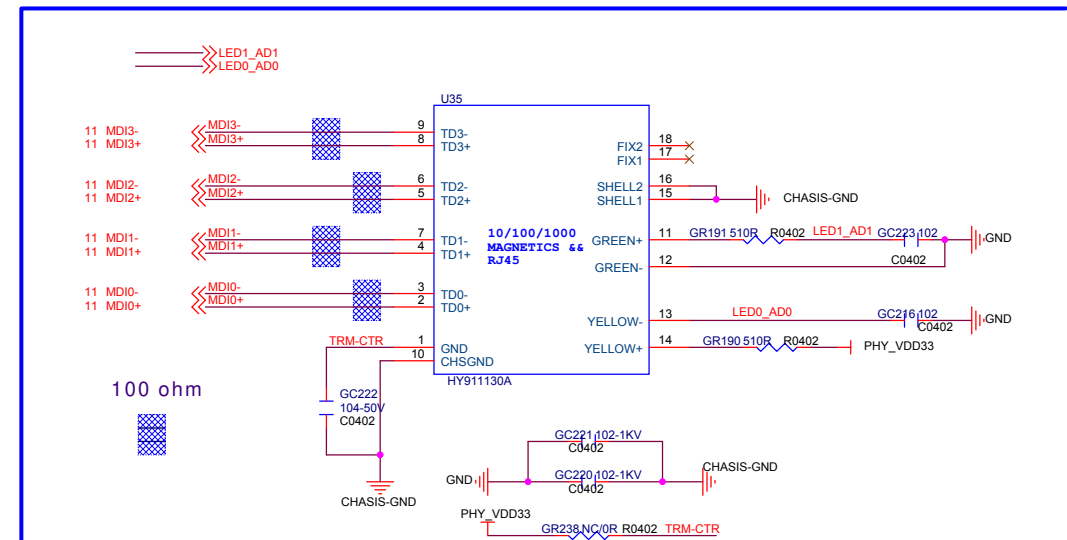
PHY_AVDD10

RTL8201FN/EN :
C40,C41,GL1 is NC
GC33,GC38,GC35,G

C44 close to pin40

PHY_VDD10

C39 close to pin28

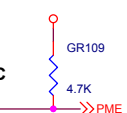


100 ohm

<i>Pine A64</i>			
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PHY_VDD33

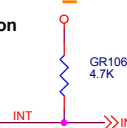
Note: PME Function
RTL8211D/8211E/ 8201FN only
RTL8201EN/8211CN Pin33 is NC



Interrupt

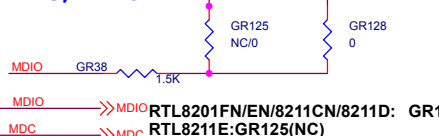
PHY_VDD33

GR127 for RTL8201EN INT function



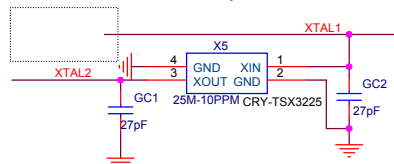
PHY_VDD33

MDC/MDIO



RTL8201FN/EN/8211CN/8211D: GR128(NC)
RTL8211E:GR125(NC)

External clock source from OSC or Chipset.



Use external clock:
RTL8201FN/RTL8201EN/8211CN/8211D/8211E: GR105(0 ohm)

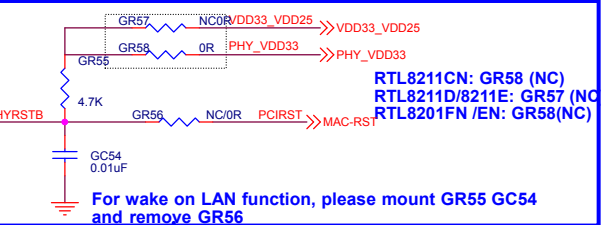
Enable/Disable SWREG

PHY_AVDD33

Connect ENSWREG to PHY_AVDD33
to enable Switching regulator or
connect ENSWREG to GND to
disable Switching regulator.

RTL8201FN /EN:
GR65 is Fiber Mode
GR66 is UTP Mode(default)

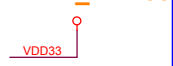
PHY Reset



RTL8211CN: GR58 (NC)
RTL8211D/8211E: GR57 (NC)
RTL8201FN /EN: GR58(NC)

For wake on LAN function, please mount GR55 GC54
and remove GR56

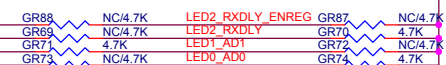
PHY_VDD33



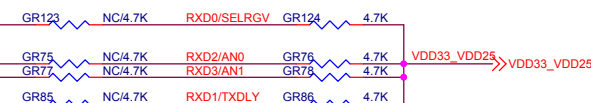
RTL8201FN: Pull High for LDO Enable
Pull Low for LDO disable

PHY_VDD33

PHY_VDD33



RTL8211D/E: If use 2.5V RGMII please pull down (GR123)RXD0/SELRGV
RTL8211CN/8201EN:GR123,GR124 NC

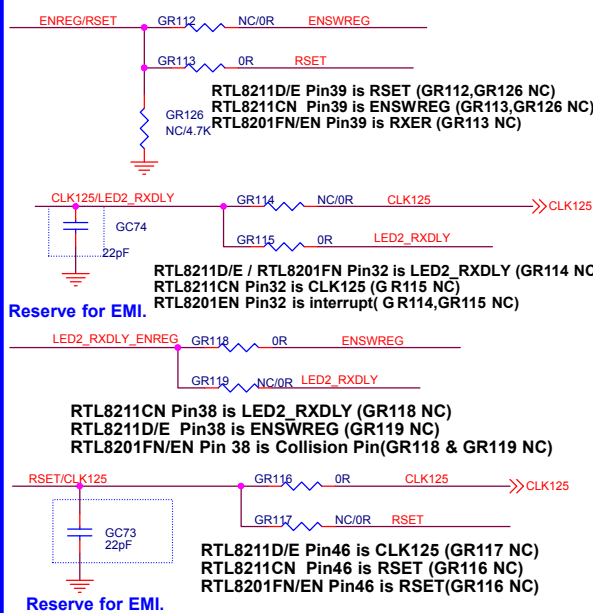


RTL8211CN/8211D/8211E:
GR76,GR78: Config for all capability
GR71,GR74: PHY Address=01 (8211D/8211CN)
GR46,GR71,R74: PHY Address=001 (8211E)
GR69,GR85: Without TX/RX Delay

RTL8201EN:
GR88:MII Interface
GR87:SNII Interface
GR71,GR74: PHY Address=001
Other resistors are NC

RTL8201FN:
R78 : REF CLK Input
R77: REF CLK Output
R69,R71,R74: PHY Address=001
Other resistors are NC

RSET/ENSWREG/CLK125 Co-layout



Reserve for EMI.

RTL8211D/E Pin39 is RSET (GR112,GR126 NC)
RTL8211CN Pin39 is ENSWREG (GR113,GR126 NC)
RTL8201FN/EN Pin39 is RXER (GR113 NC)

RTL8211D/E / RTL8201FN Pin32 is LED2_RXDLY (GR114 NC)
RTL8211CN Pin32 is CLK125 (G R115 NC)
RTL8201FN Pin32 is interrupt (GR114,GR115 NC)

RTL8211CN Pin38 is LED2_RXDLY (GR118 NC)
RTL8211D/E Pin38 is ENSWREG (GR119 NC)
RTL8201FN/EN Pin 38 is Collision Pin (GR118 & GR119 NC)

Reserve for EMI.

RTL8211D/E:GC45(NC)
RTL8211CN:GC45(NC)

