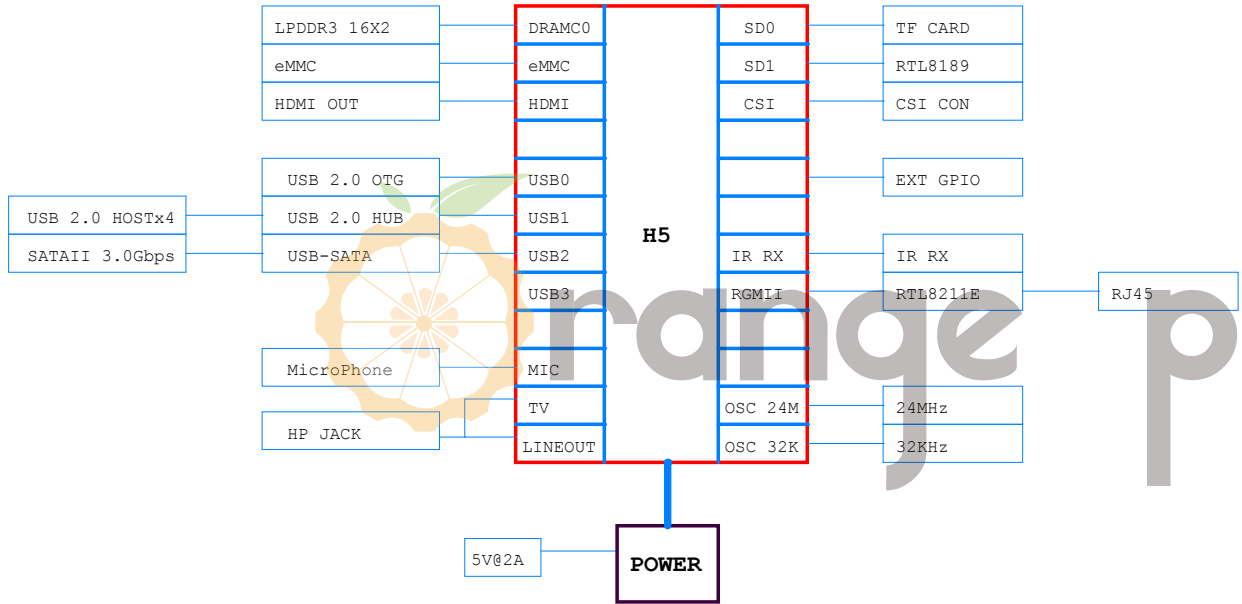


REVISION HISTORY

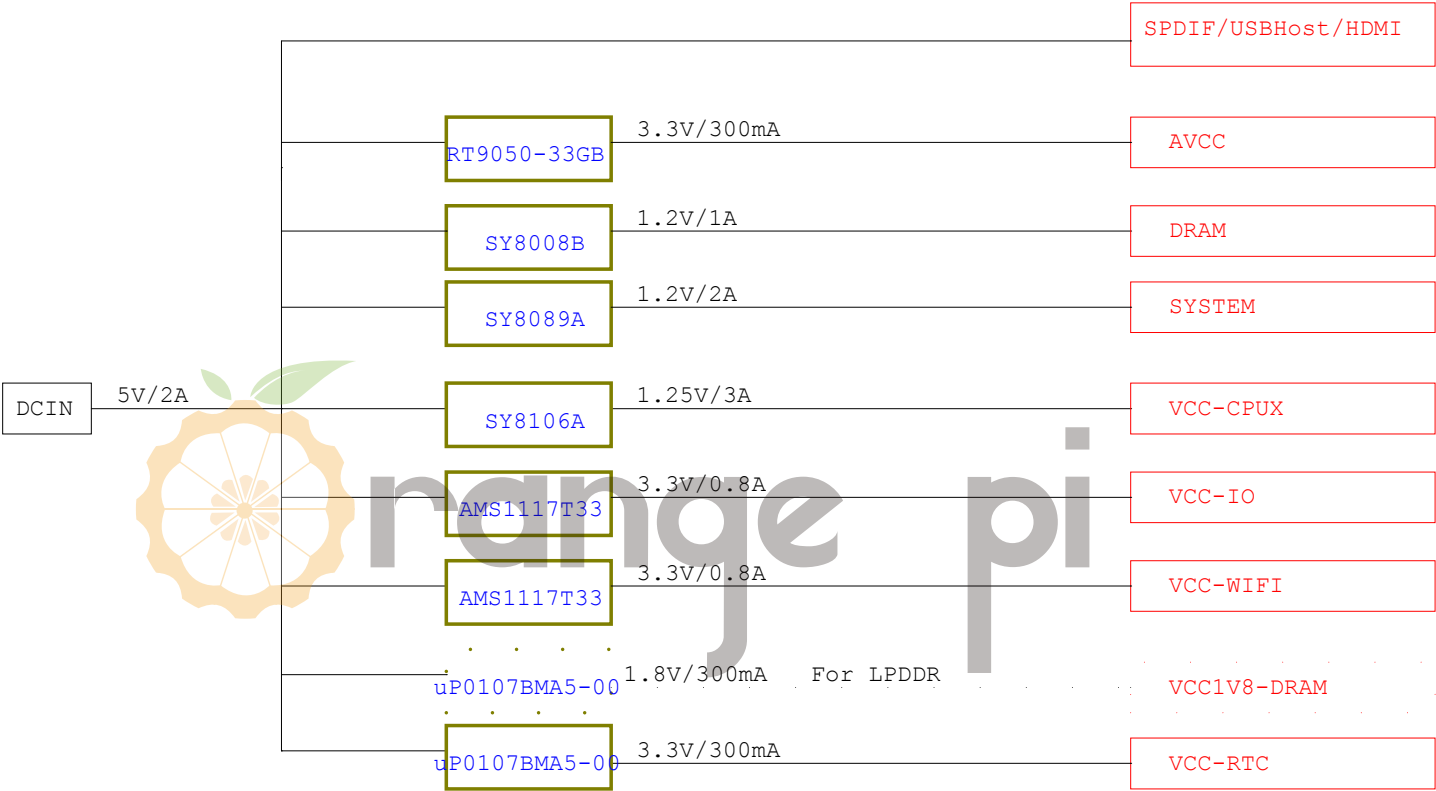
Schematics Index:

Revision	Description	Date	Drawn	Checked
Ver 1.0	Initial	2016-07-21		
Ver 1.1	增加CPU核电压电容 (10uf, 104)	2016-09-09		





POWER TREE



GPIO ASSIGNMENT

PIN	Define	CFG	Function
PA0	EMS/DRVVBUS0	3/1	JTAG /USB
PA1	CK/DRVVBUS1	3/1	
PA2	TDO/WPS	3/1	
PA3	FDI	3	UART
PA4	JART-TX	3	
PA5	JART-RX	3	
PA6	NC	7	
PA7	NC	7	
PA8	NC	7	
PA9	NC	7	
PA10	NC	7	
PA11	NC	7	
PA12	NC	7	
PA13	NC	7	
PA14	NC	7	
PA15	STATUS-LED	1	LED
PA16	MUTE	1	AV
PA17	SPDIF-OUT	2	SPDIF
PA18	NC	7	
PA19	NC	7	
PA20	NC	7	
PA21	NC	7	

PIN	Define	CFG	Function
PC0	NWE	2/3	
PC1	NALE	2/3	
PC2	NCLE	2/3	
PC3	NCE1	2/3	
PC4	NCE0	2	
PC5	NRE	2/3	
PC6	NRB0	2/3	NAND /eMMC /NOR
PC7	NRB1	2	
PC8	NDQ0	2/3	
PC9	NDQ1	2/3	
PC10	NDQ2	2/3	
PC11	NDQ3	2/3	
PC12	NDQ4	2/3	
PC13	NDQ5	2/3	
PC14	NDQ6	2/3	
PC15	NDQ7	2/3	
PC16	NDQS	2/3	

PIN	Define	CFG	Function
PD0	NC	7	
PD1	NC	7	
PD2	NC	7	
PD3	NC	7	
PD4	NC	7	
PD5	NC	7	
PD6	NC	7	
PD7	NC	7	
PD8	NC	7	
PD9	NC	7	
PD10	NC	7	
PD11	NC	7	
PD12	NC	7	
PD13	NC	7	
PD14	NC	7	
PD15	NC	7	
PD16	NC	7	
PD17	NC	7	

PIN	Define	CFG	Function
PE0	NC	7	
PE1	NC	7	
PE2	NC	7	
PE3	NC	7	
PE4	NC	7	
PE5	NC	7	
PE6	NC	7	
PE7	NC	7	
PE8	NC	7	
PE9	NC	7	
PE10	NC	7	
PE11	NC	7	
PE12	NC	7	
PE13	NC	7	
PE14	NC	7	
PE15	NC	7	

PIN	Define	CFG	Function
PF0	D1	2	CARD0
PF1	D0	2	
PF2	CLK	2	
PF3	CMD	2	
PF4	D3	2	
PF5	D2	2	
PF6	DET	0	

PIN	Define	CFG	Function
PG0	NC	7	
PG1	NC	7	
PG2	NC	7	
PG3	NC	7	
PG4	NC	7	
PG5	NC	7	
PG6	NC	7	
PG7	NC	7	
PG8	NC	7	
PG9	NC	7	
PG10	NC	7	
PG11	NC	7	
PG12	NC	7	
PG13	NC	7	

PIN	Define	CFG	Function
PL0	TWI	2	TWI
PL1	TWI	2	
PL2	USB0-DRVVBUS	1	USB
PL3	USB1-DRVVBUS	1	
PL4	RECOVERY	0	KEY
PL5	VCC-IO-EN	1	IO-EN
PL6	NC	7	
PL7	WIFI-EN	7	
PL8	PWR-STB	1	
PL9	PWR-DRAW	1	
PL10	PWR-LED	1	
PL11	IR-RX	2	

4

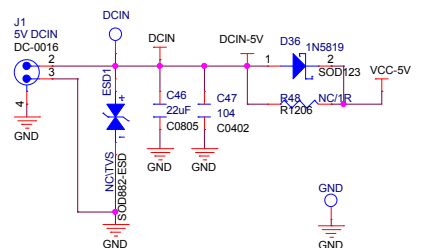


5 4 3 2 1



	PWRON/WORK	STANDBY	PWROFF
PWR-STB	1	0	0
PWR-DRAM	1	1	0

DCIN

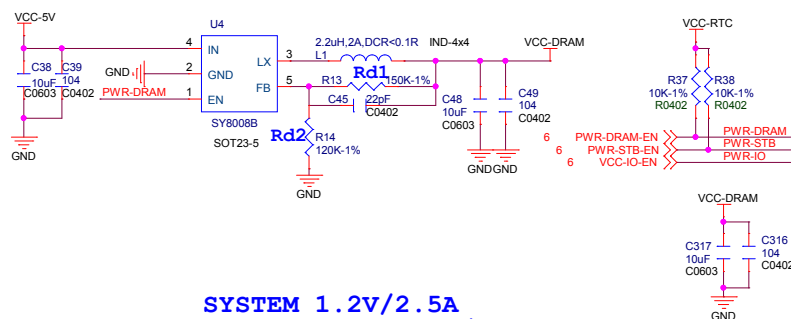


POWER

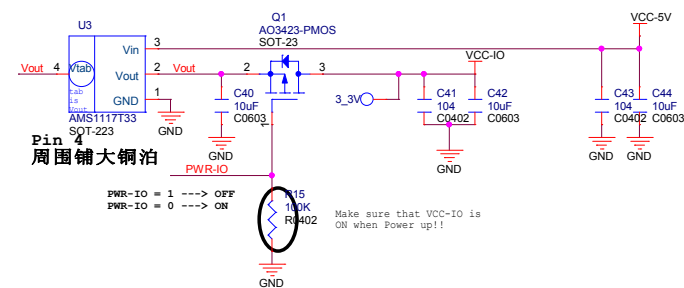
$$V_{out} = 0.6 * (1 + R_{d1}/R_{d2})$$

$$V_{DRAM} = 1.5V/1A, R_2 = 100K-1\%$$

$$V_{DRAM} = 1.35V/1A, R_2 = 120K-1\%$$

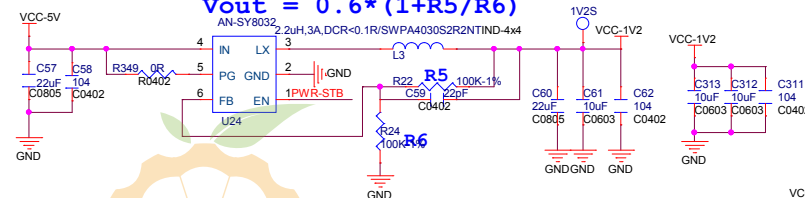


VCCIO 3.3V/1A

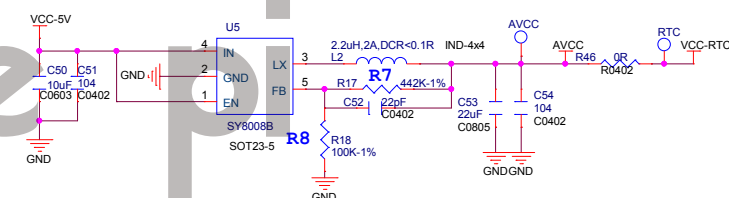


SYSTEM 1.2V/2.5A

$$V_{out} = 0.6 * (1 + R_5/R_6)$$

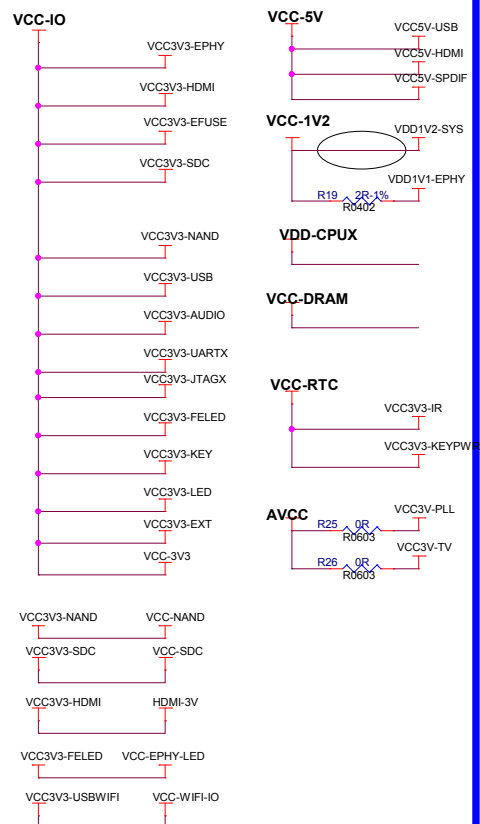
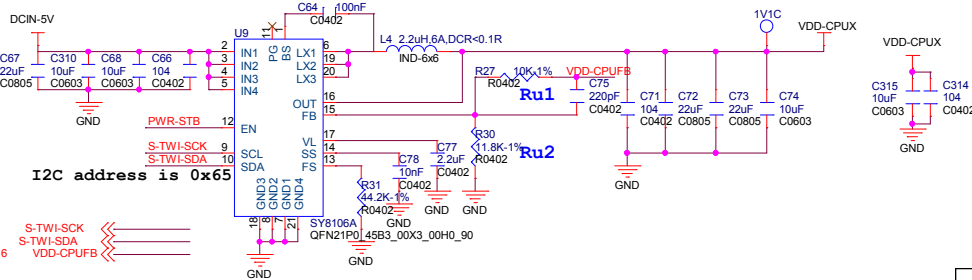


AVCC 3.3V/1A



CPUX 1.2V/6A

$$V_{out} = 0.6 * (1 + R_{u1}/R_{u2})$$



HS, 此处电压调整为1.1V (调整电阻R01、R02)

Xunlong Software

Design Name
ORANGE_PI_PC2

Size
A3

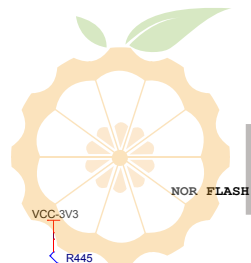
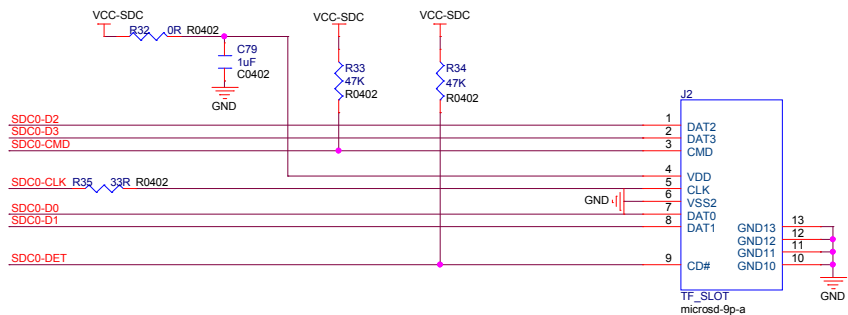
Page Name
POWER

Rev

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TF-eMMC

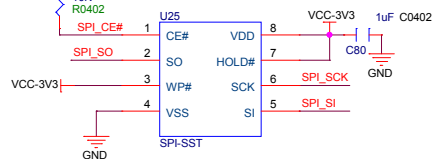
6 SDC0-D1
6 SDC0-D0
6 SDC0-CLK
6 SDC0-CMD
6 SDC0-D3
6 SDC0-D2
6 SDC0-DET



range pi

6 SPI0_MOSI
6 SPI0_MISO
6 SPI0_CLK
6 SPI0_CS0

SPI_SI
SPI_SO
SPI_SCK
SPI_CE#



Xunlong Software

Design Name

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Page Name
eMMC-NOR FLASH

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USB

5

4

3

2

1

D

D

C

C

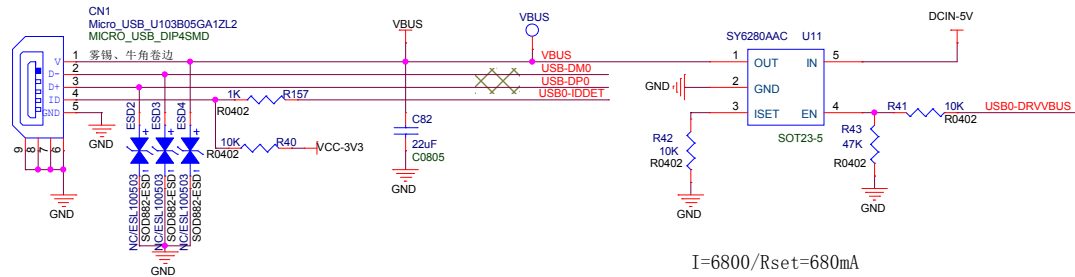
B

B

A

A

- 6 USB-DM0
- 6 USB-DP0
- 6 USB0-IDDET
- 6 USB0-DRVVBUS



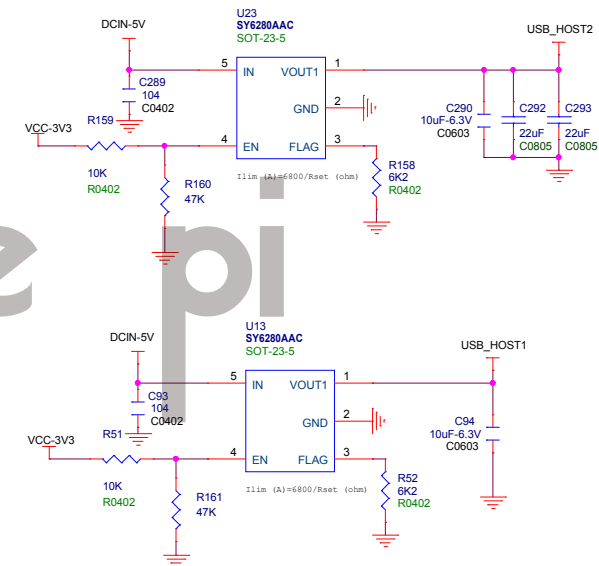
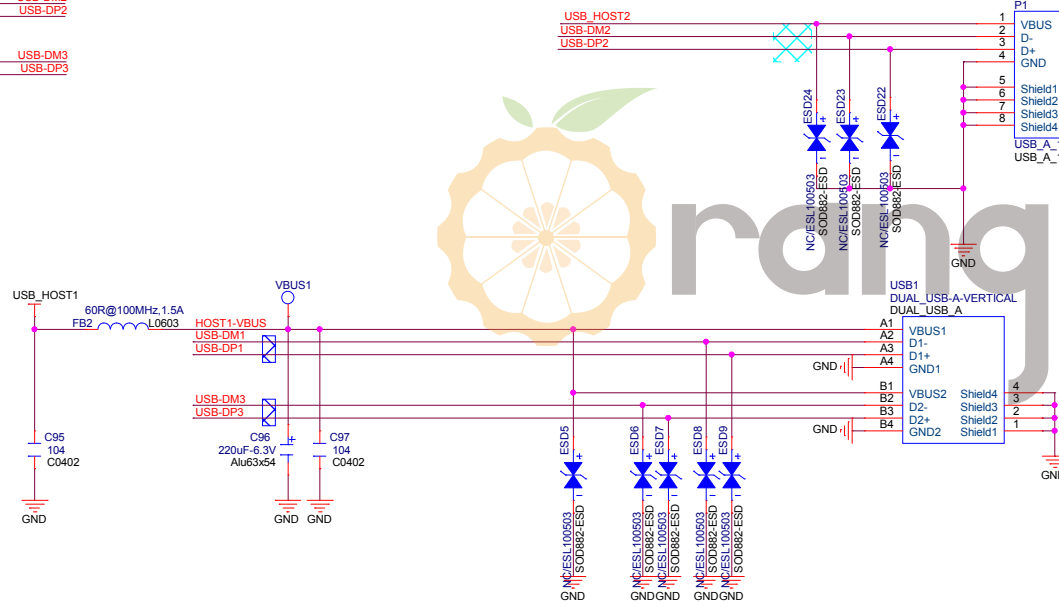
I=6800/Rset=680mA

- 6 USB-DM1
- 6 USB-DP1
- 6 USB1-DRVVBUS

- 6 USB-DM2
- 6 USB-DP2

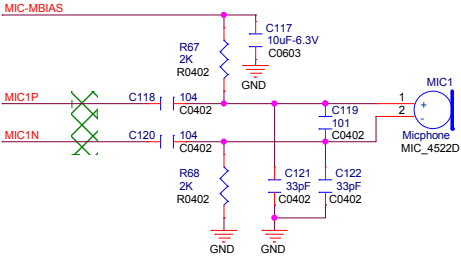
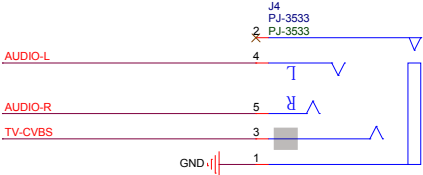
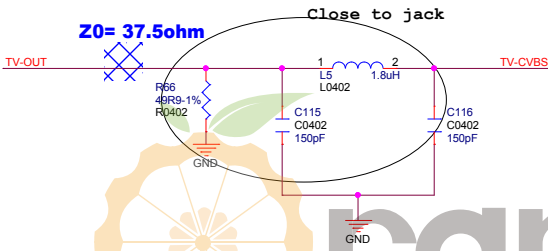
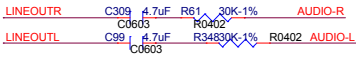
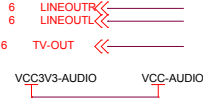
- 6 USB-DM3
- 6 USB-DP3

note: Make sure the routing between the ESD and the USB connectors should be on the same PCB side



Xunlong Software			
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A3	USB		
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AV-MIC

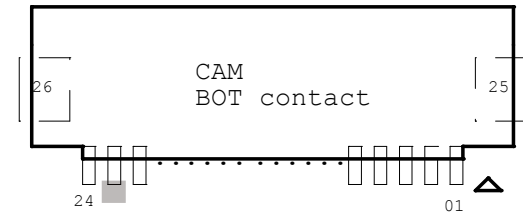
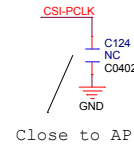
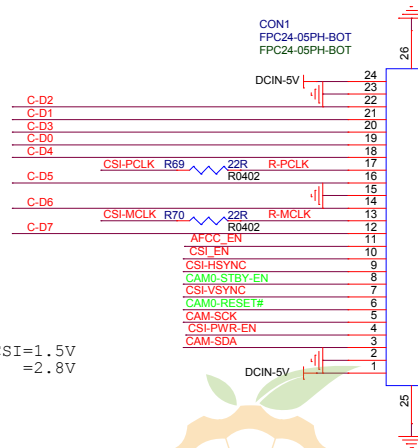


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Design Name			
ORANGE_PI_PC2			
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A3	AV-MIC		
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Camera

6	CSI-RESET#	CAM0-RESET#
6	CSI-STBY-EN	CAM0-STBY-EN
6	CSI-PWR-EN	CSI-PWR-EN
6	CSI-SCK	CAM-SCK
6	CSI-SDA	CAM-SDA
6	CSI-PCLK	CSI-PCLK
6	CSI-MCLK	CSI-MCLK
6	CSI-HSYNC	CSI-HSYNC
6	CSI-VSYNC	CSI-VSYNC
6	CSI-D0	C-D0
6	CSI-D1	C-D1
6	CSI-D2	C-D2
6	CSI-D3	C-D3
6	CSI-D4	C-D4
6	CSI-D5	C-D5
6	CSI-D6	C-D6
6	CSI-D7	C-D7
6	AFCC_EN	AFCC_EN

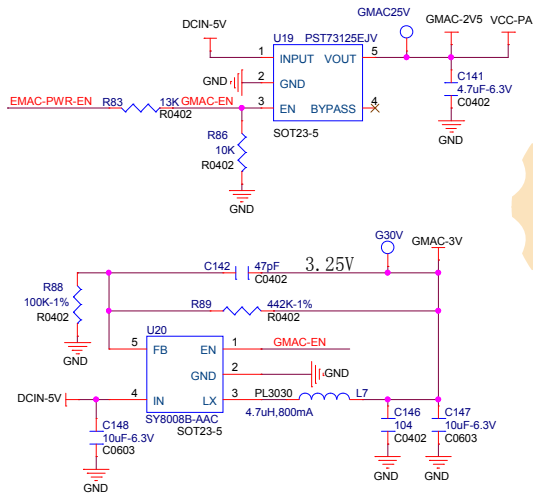
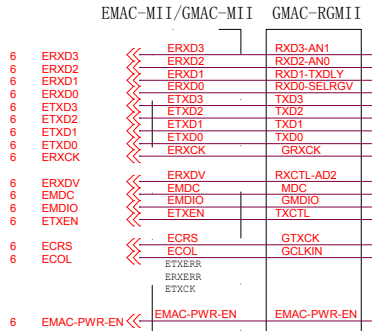
VDD1V5-CSI=1.5V
VCC-CSI =2.8V



Xunlong Software			
Design Name		ORANGE_PI_PC2	
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A3	CSI		
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GMAC

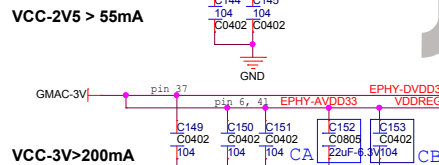
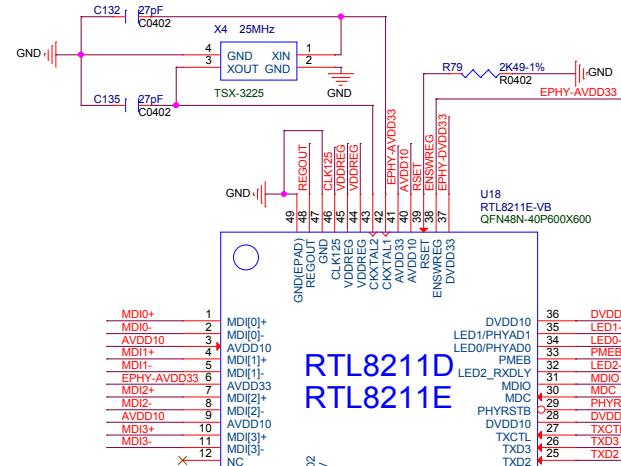
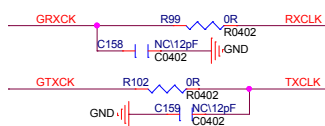
10/100/1000 RGMII Ethernet PHY



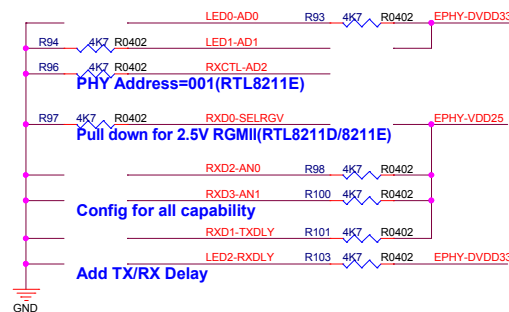
Place filter network close to CLK125.
Reserved for EMI



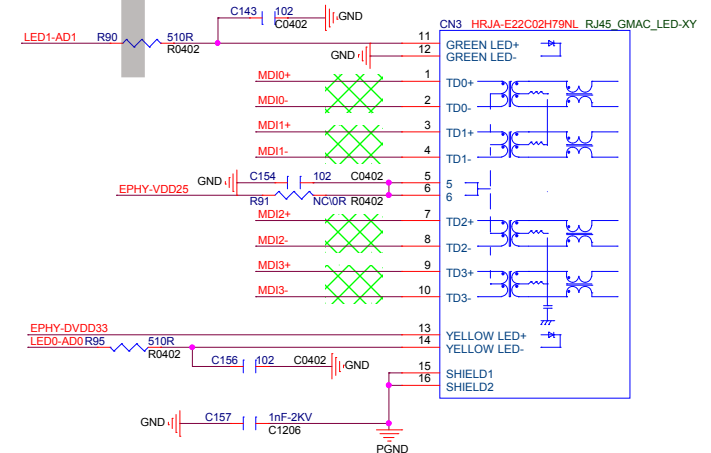
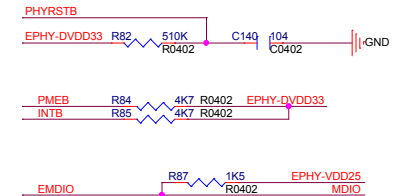
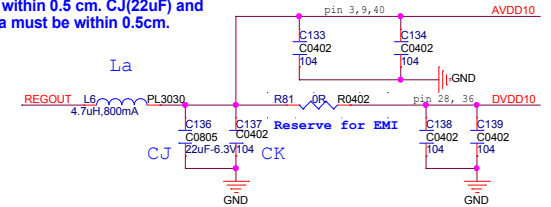
Place filter network close to RX_CLK.
Reserved for EMI



Note 2: The Trace length from CA(22uF),CB(0.1uF) to Pin 44,45(VDDREG) must be within 0.5 cm. The trace width from AVDD33 to Pin 44,45 should be >40mils.



Note 1: The Trace length between La and PHY's Pin48 must be within 0.5 cm. CJ(22uF) and CK(0.1uF) to La must be within 0.5cm.

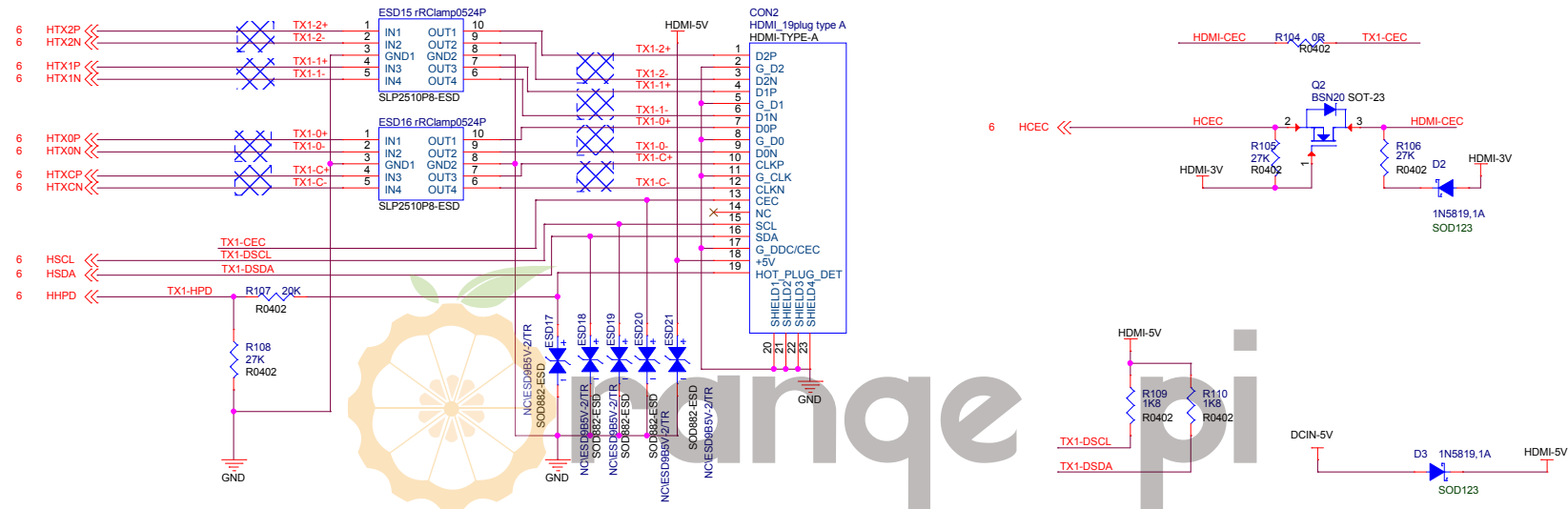


LED0:Blinking=Transmitting or Receiving.
LED1:Link Up/Down

Xunlong Software

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HDMI



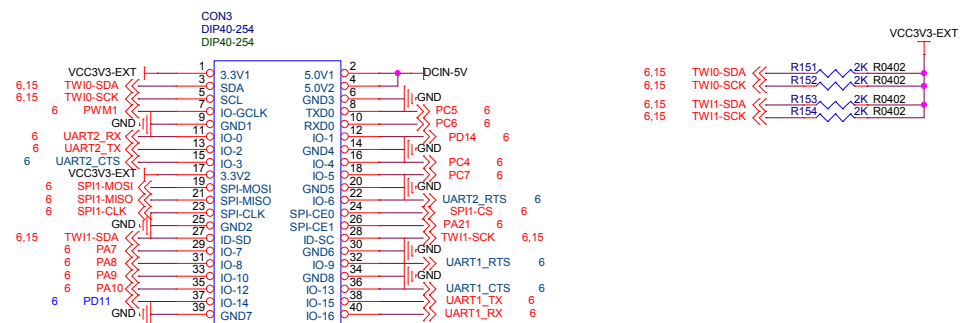
WIFI



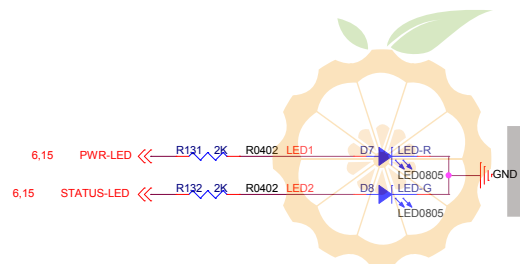
Xunlong Software			
Design Name		ORANGE_PI_PC2	
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A3	WIFI		
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Ext Port

Ext



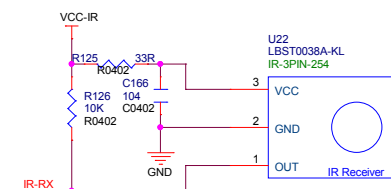
LED



KEY



IR



DEBUG

