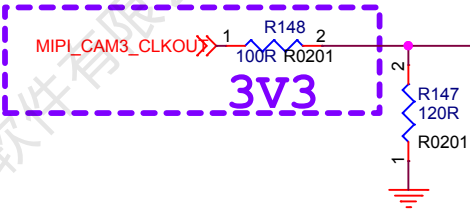
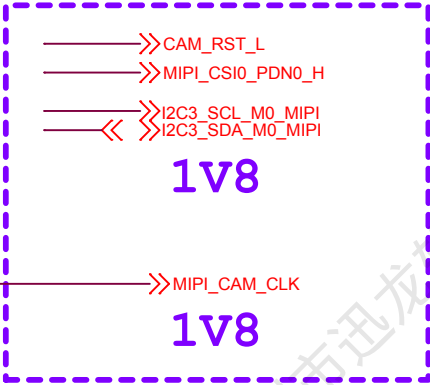
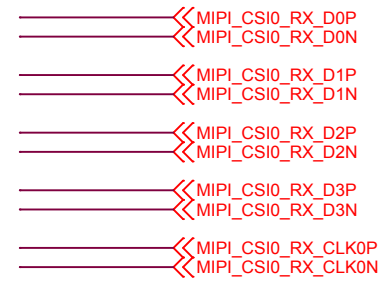
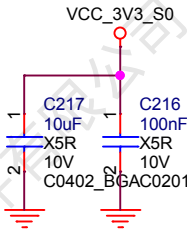
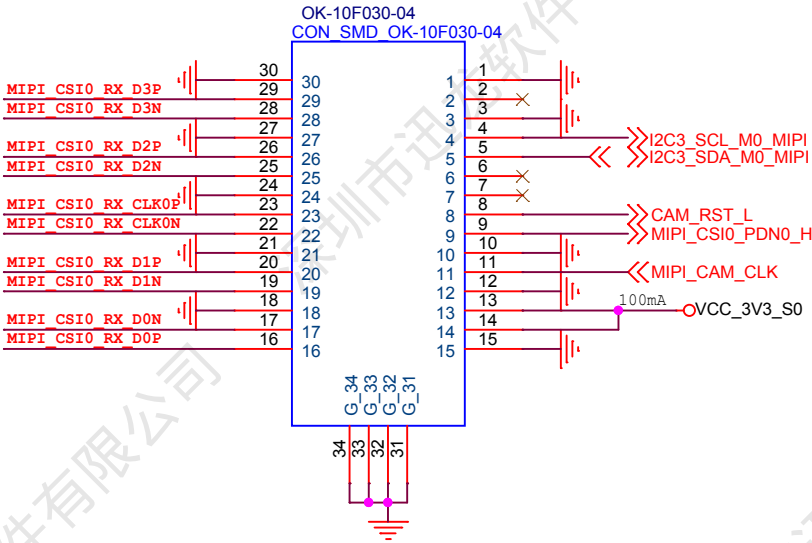


MIPI-CSIO_RX

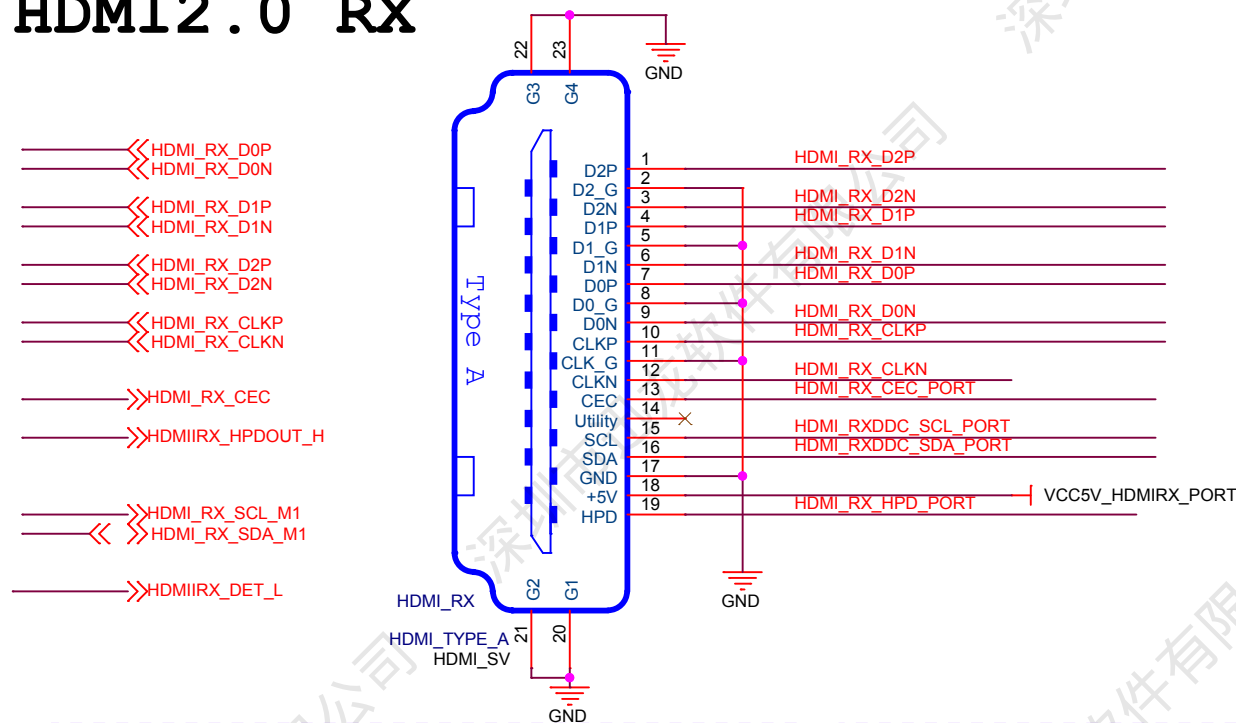


CAM



Shenzhen Xunlong Software Co., Ltd				
Project:	OPI 5 PLUS			
File:	01.VI-Camera_MIPI_CSI-RX			
Date:	Friday, July 25, 2025			Rev: V1.3.1
Size:	A3	Sheet:	1	Of: 33

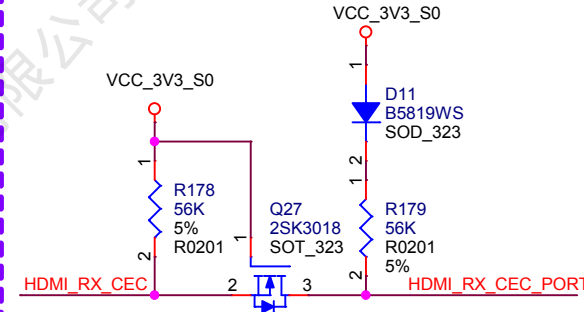
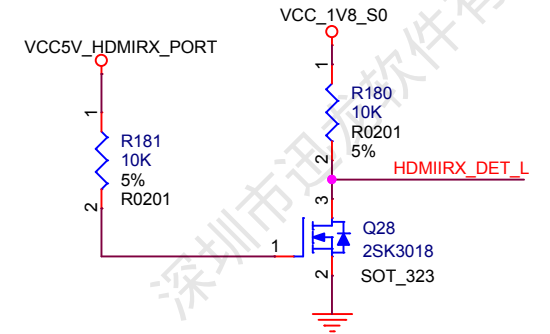
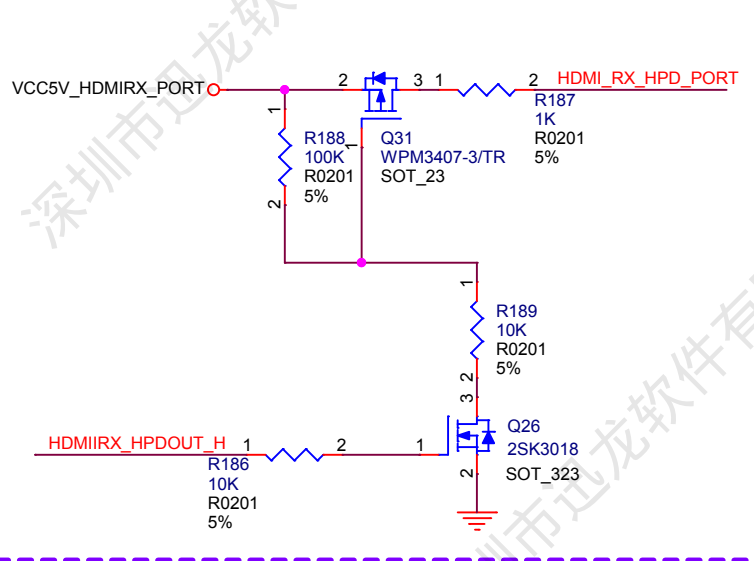
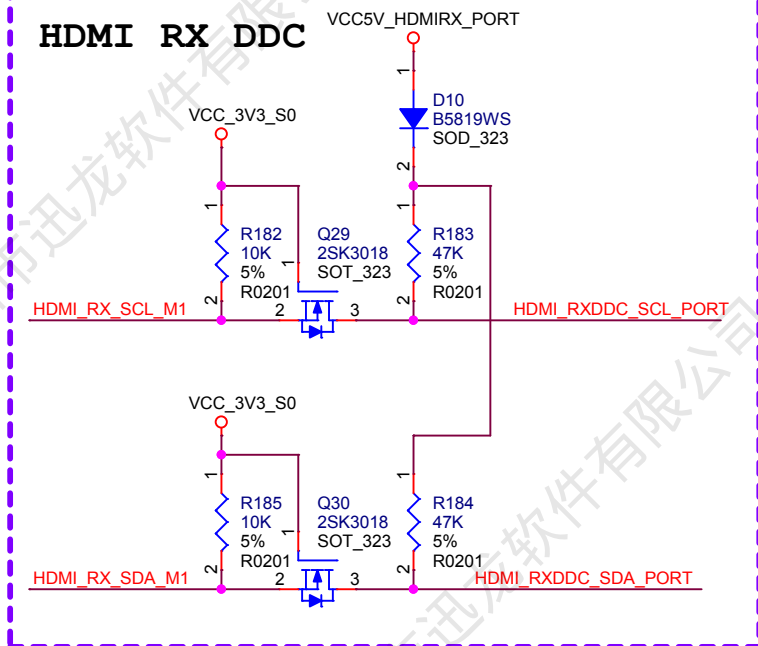
HDMI2.0 RX



Note:

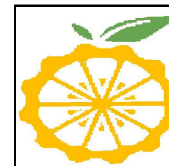
(This HDMI2.0 RX interface has low probability anomalies, such as splash screen and restart, in scenarios such as frequent plug and pull, high and low resolution switching, etc. The probability is between 0.1% and 1%. We are still trying to debug and solve these problems. If the user will frequently use various peripherals to insert this HDMI2.0 RX interface, it is recommended to use external bridges connecting chips to improve compatibility to avoid affecting product production.)

HDMI RX DDC



HPD:

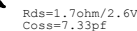
Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side: Require input and Detection.
Min 2.0V, Max: 5.3V



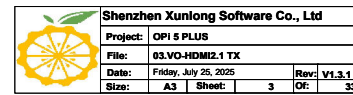
Shenzhen Xunlong Software Co., Ltd

Project:	OPI 5 PLUS		
File:	02.VI-HDMI2.0 RX		
Date:	Friday, July 25, 2025	Rev:	V1.3.1
Size:	A3	Sheet:	2

HDMI TX0

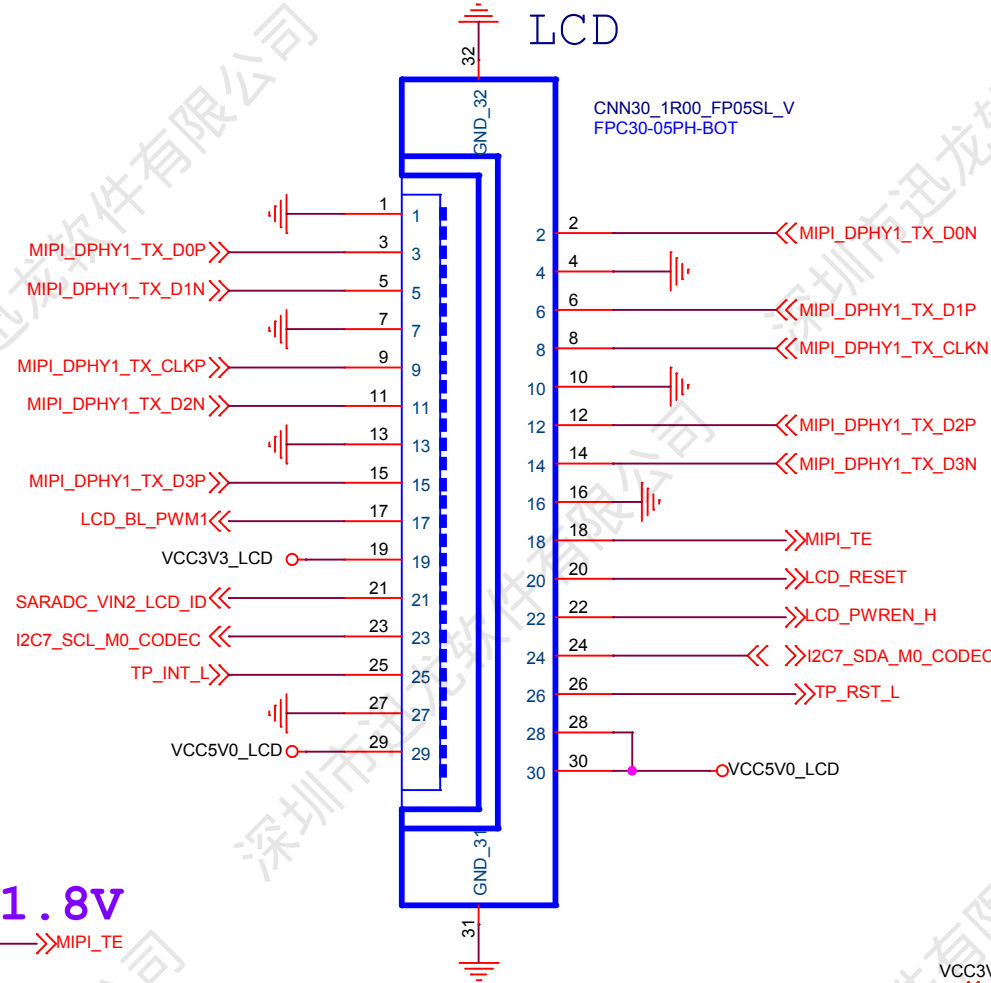
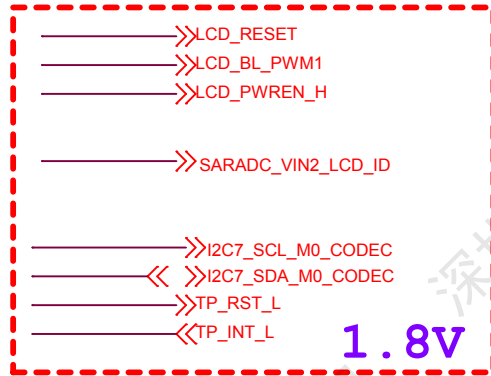


HDMI TX1



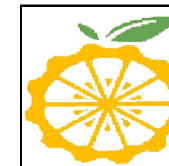
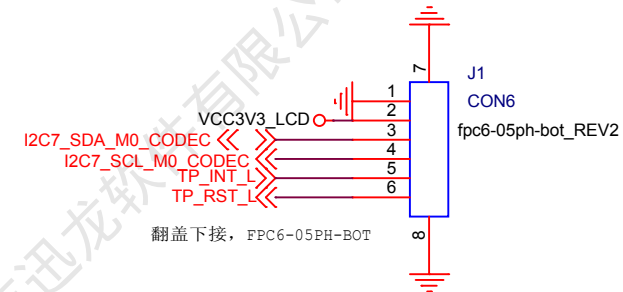
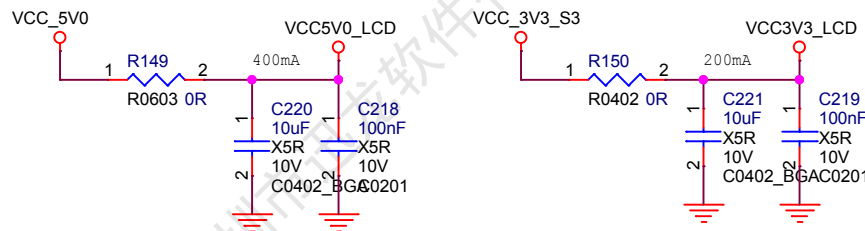
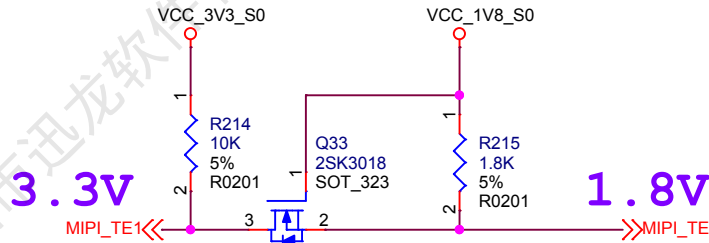
MIPI DPHY1 TX

MIPI DPHY1 TX



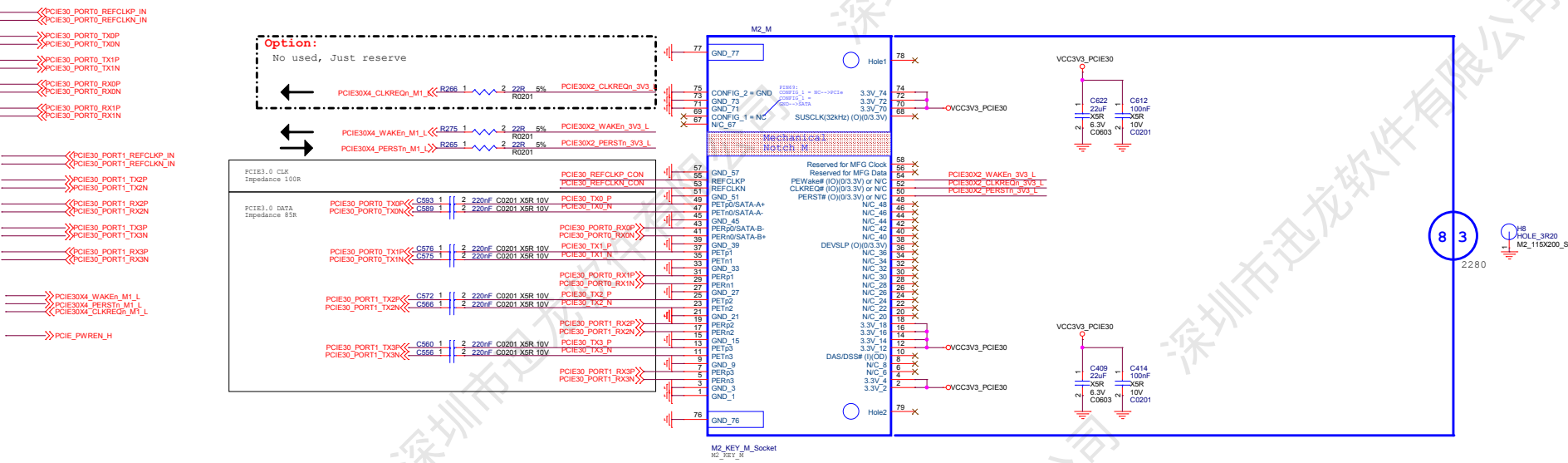
FPC Pin List

Pin1 :GND
Pin2 :D0N
Pin3 :D0P
Pin4 :GND
Pin5 :D1N
Pin6 :D1P
Pin7 :GND
Pin8 :CLKN/AUXN
Pin9 :CLKP/AUXP
Pin10:GND
Pin11:D2N
Pin12:D2P
Pin13:GND
Pin14:D3N
Pin15:D3P
Pin16:GND
Pin17:LCD_PWM_BL
Pin18:LCD_TE
Pin19:VCC3V3_LCD
Pin20:LCD_RST
Pin21:LCD_ID
Pin22:LCD_PWREN
Pin23:TP_I2C_SCL
Pin24:TP_I2C_SDA
Pin25:TP_INT
Pin26:TP_RST
Pin27:GND
Pin28:5V0
Pin29:5V0
Pin30:5V0

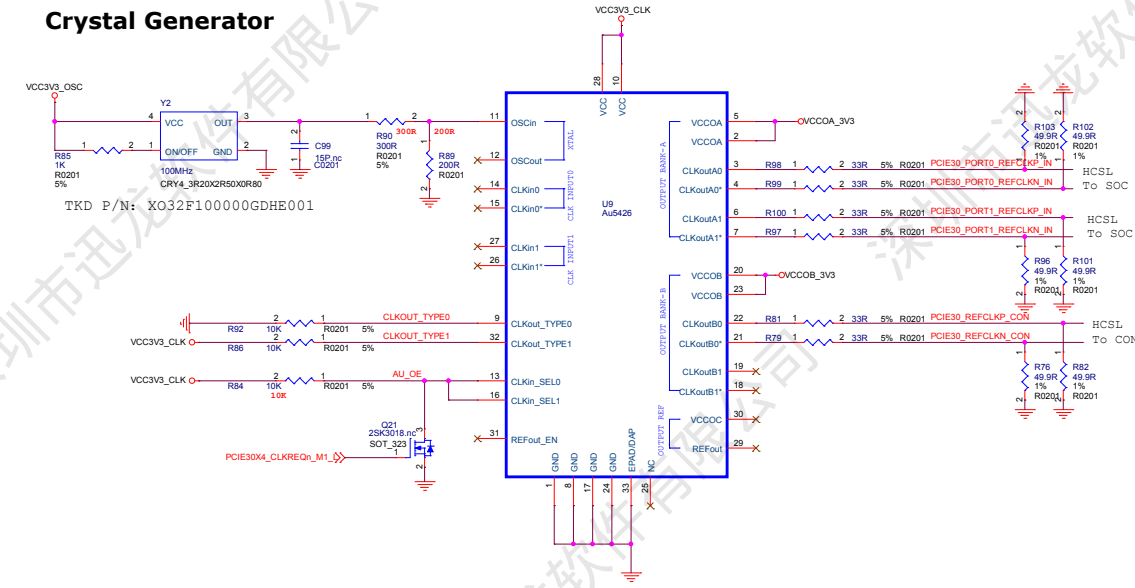


Shenzhen Xunlong Software Co., Ltd				
Project:	OPI 5 PLUS			
File:	04.VO-LCM_MIPI			
Date:	Friday, July 25, 2025	Rev:	V1.3.1	
Size:	A3	Sheet:	4	Of: 33

M.2_PCIe3.0 x 2Lanes

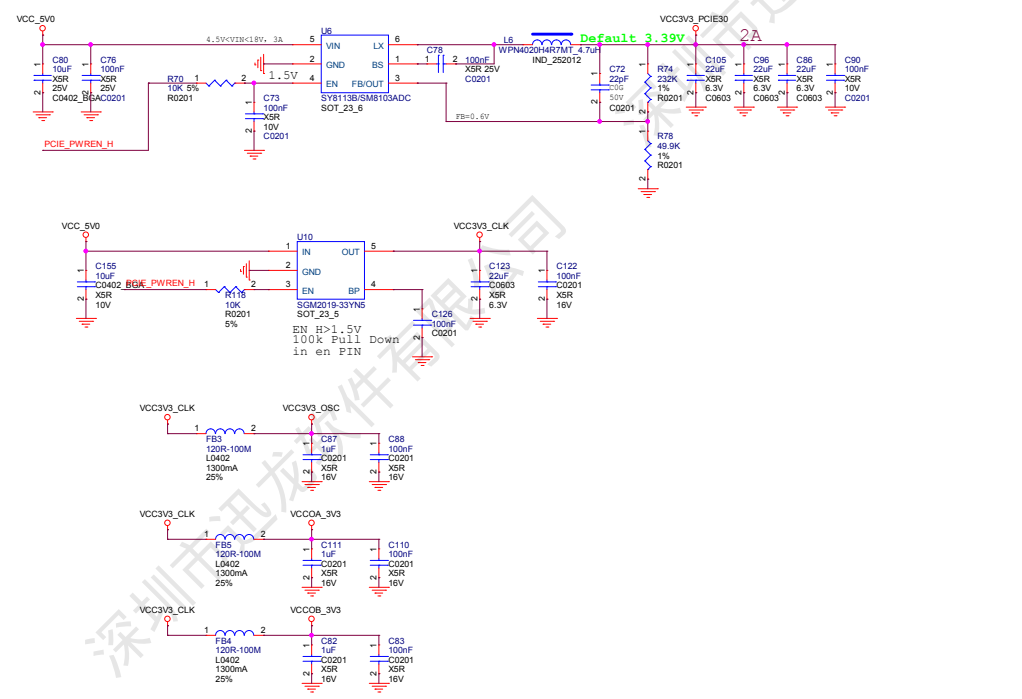


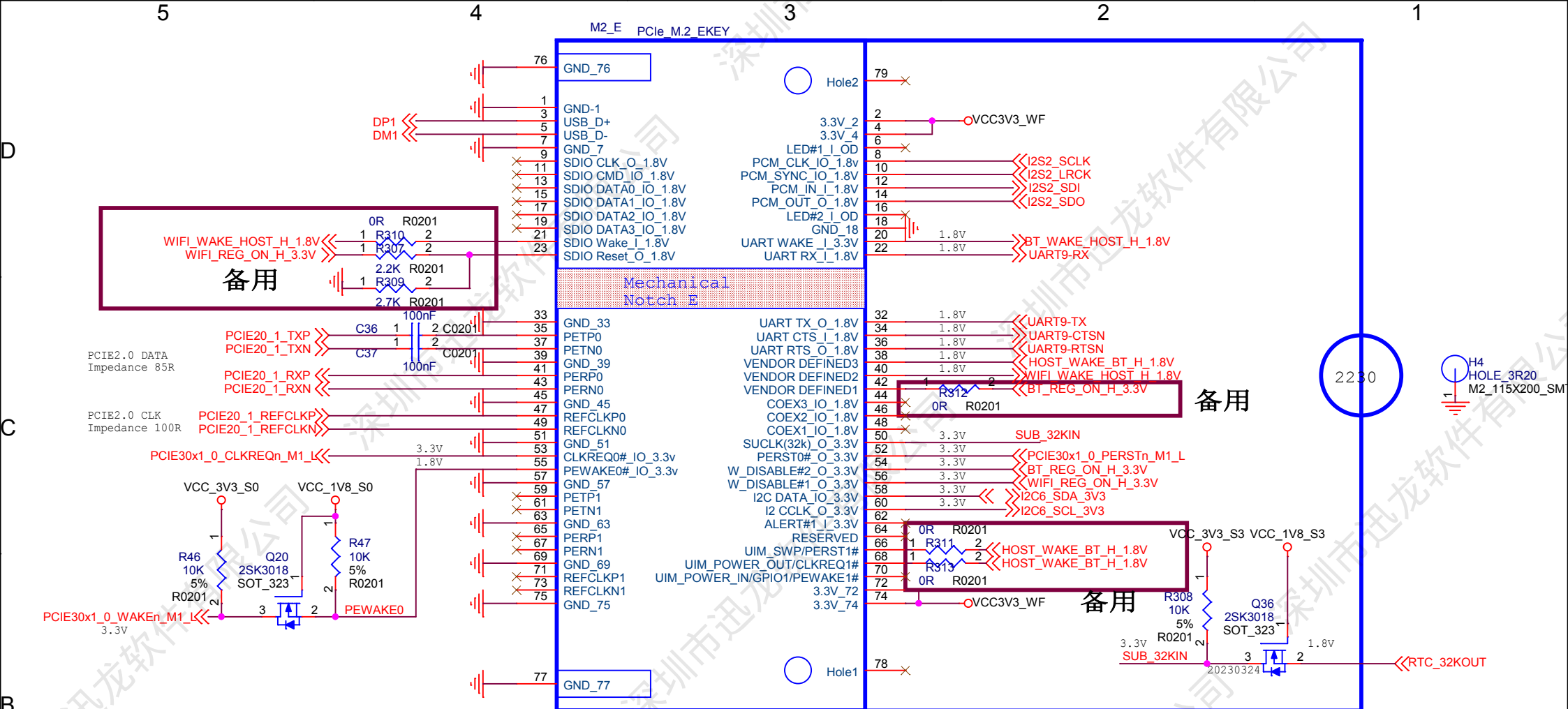
Crystal Generator



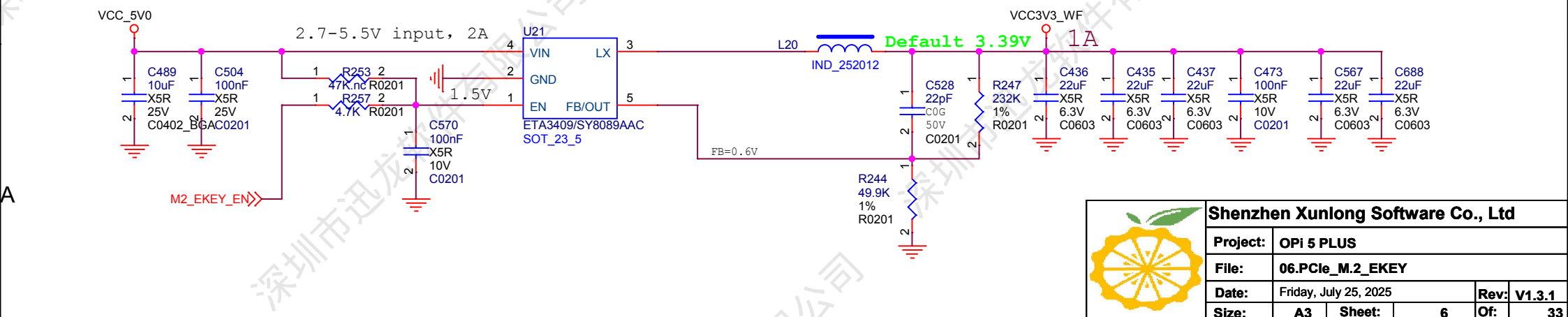
CLKIN SELECT			CLKOUT TYPE SELECT		
CLKIN_SEL1	CLKIN_SEL0	CLK Buffer Type	CLKOUT_TYPE1	CLKOUT_TYPE0	CLK Buffer Type
0	0	CLKIN0	0	0	CLKOUT0
0	1	CLKIN1	0	1	CLKOUT1
1	0	CLKIN2	1	0	CLKOUT2
1	1	CLKIN3	1	1	CLKOUT3

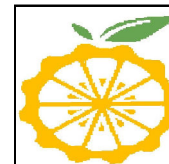
M.2 Power





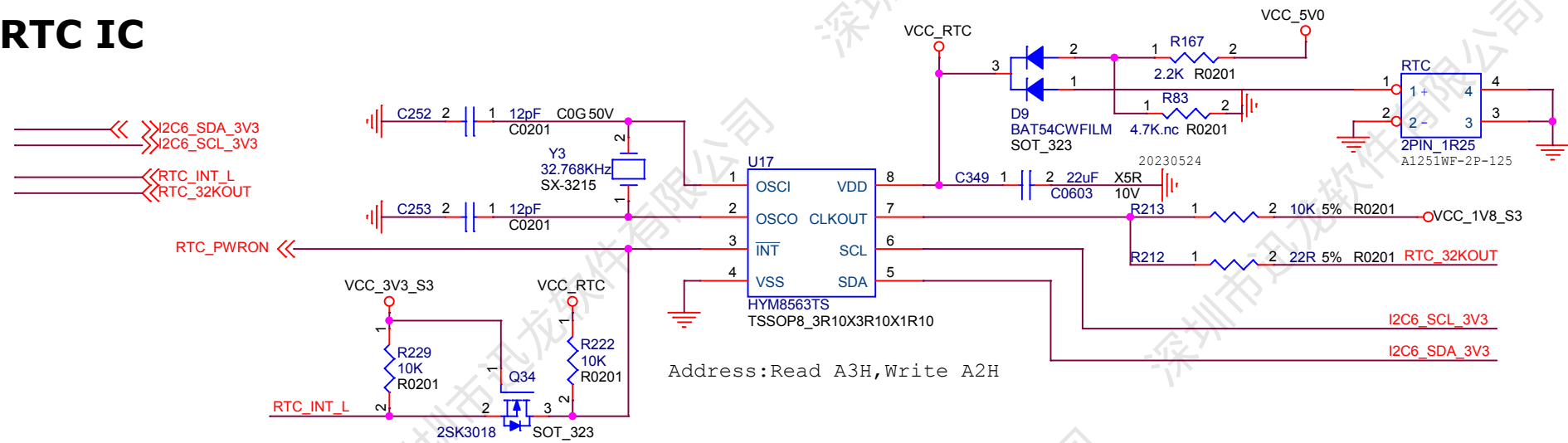
AW-XB533NF-PUR
AP12275_M2P



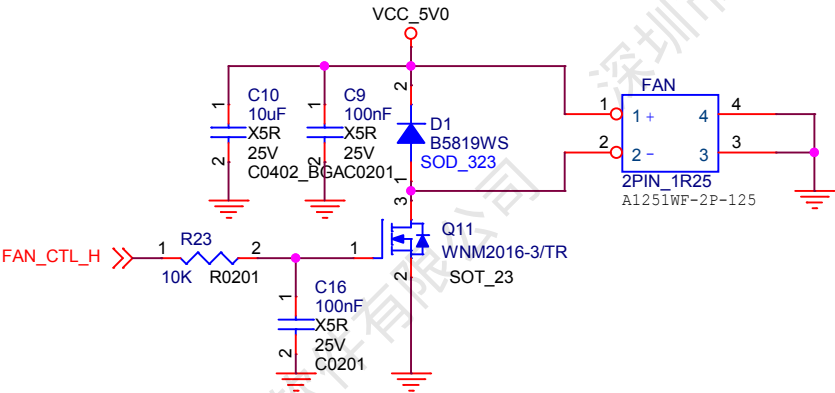


Size:	A3	Sheet:	7	Of:	33
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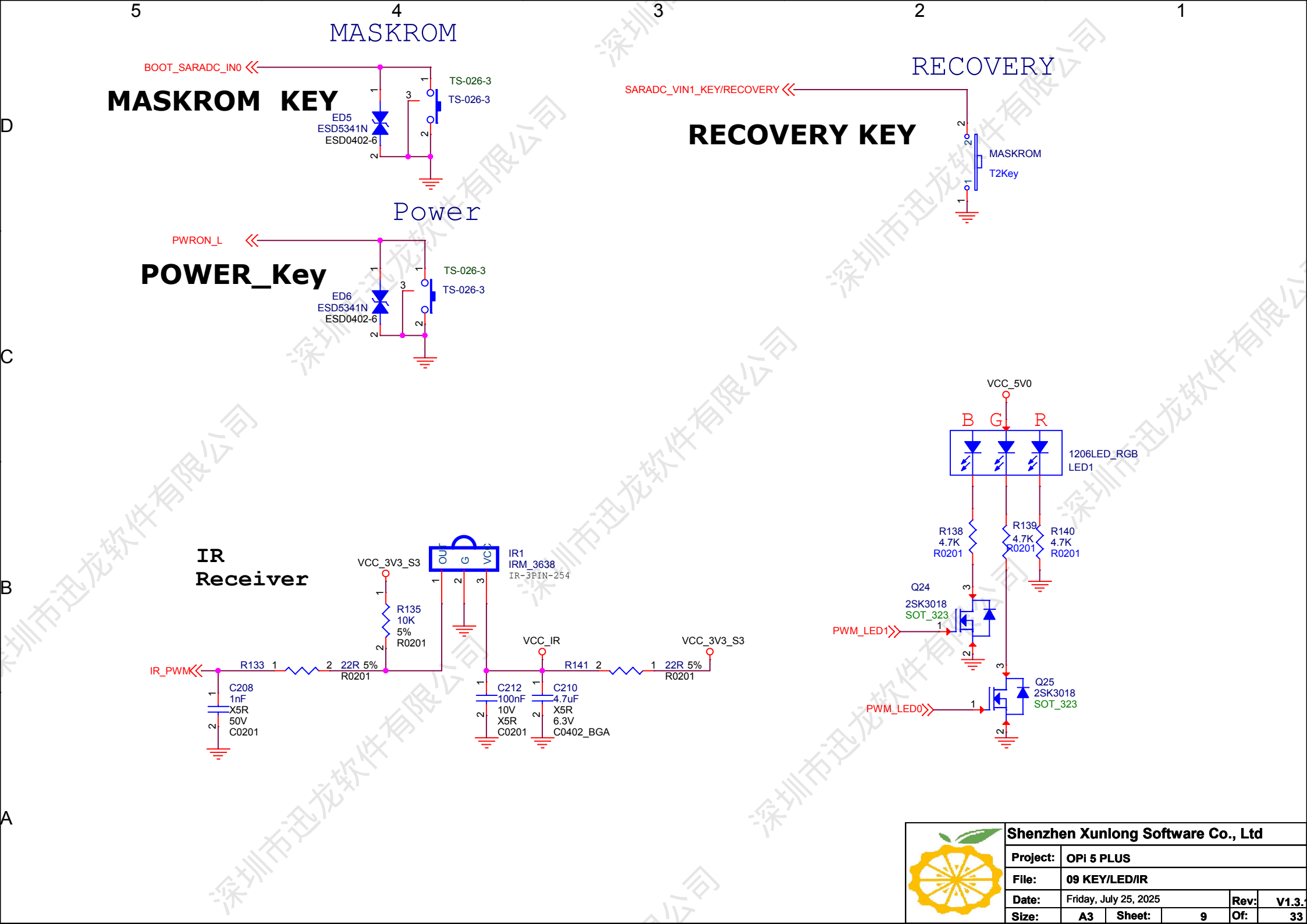
RTC IC

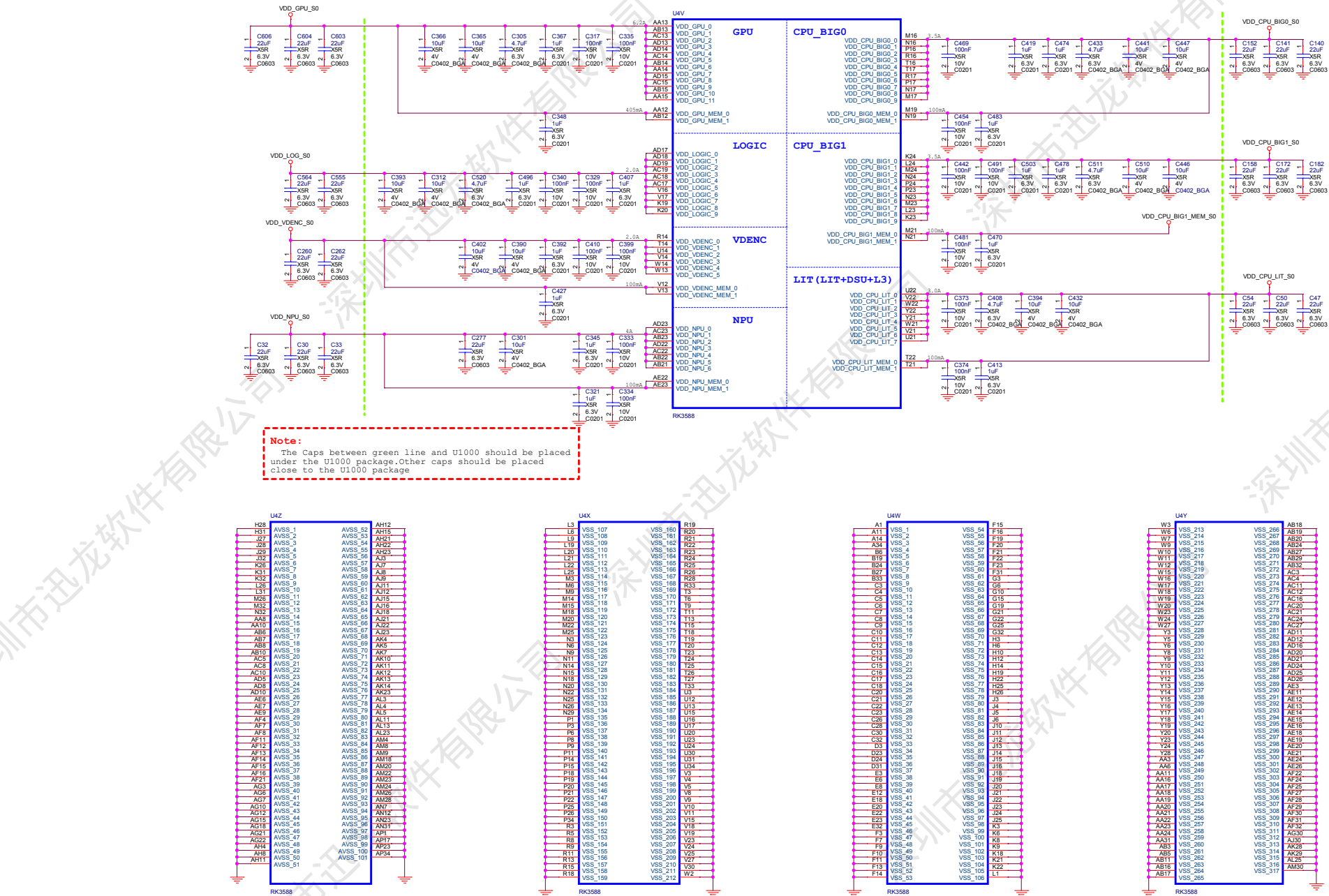


FAN_POWER



Shenzhen Xunlong Software Co., Ltd				
Project:	OPI 5 PLUS			
File:	08.RTC/FAN			
Date:	Friday, July 25, 2025			Rev: V1.3.1
Size:	A3	Sheet:	8	Of: 33





RK3588_E (OSC/PLL/PMUIO1/2)

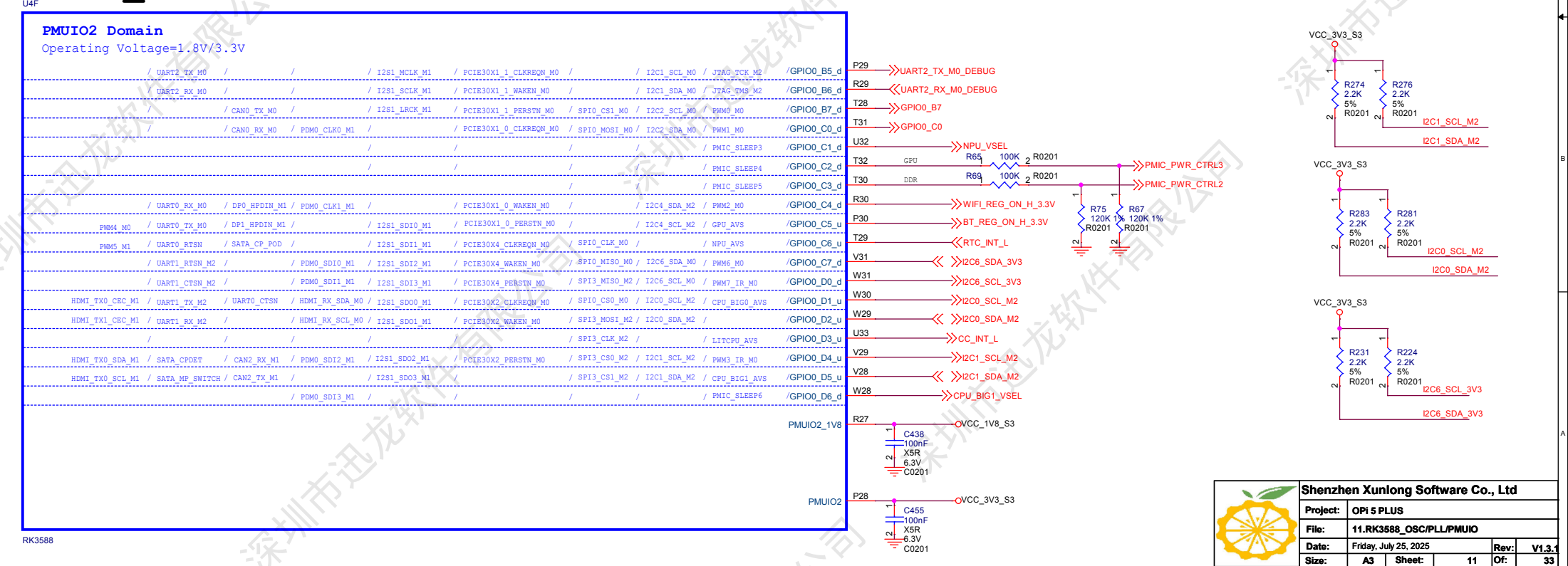
Note:
Adjusted the load capacitance according to the crystal specification

The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

$CL = \{CL1 * CL2 / (CL1 + CL2)\} + PCB \text{ strays}$
Total CL<=12pF

Note:
The Caps between green line and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3588_F (PMUIO2)

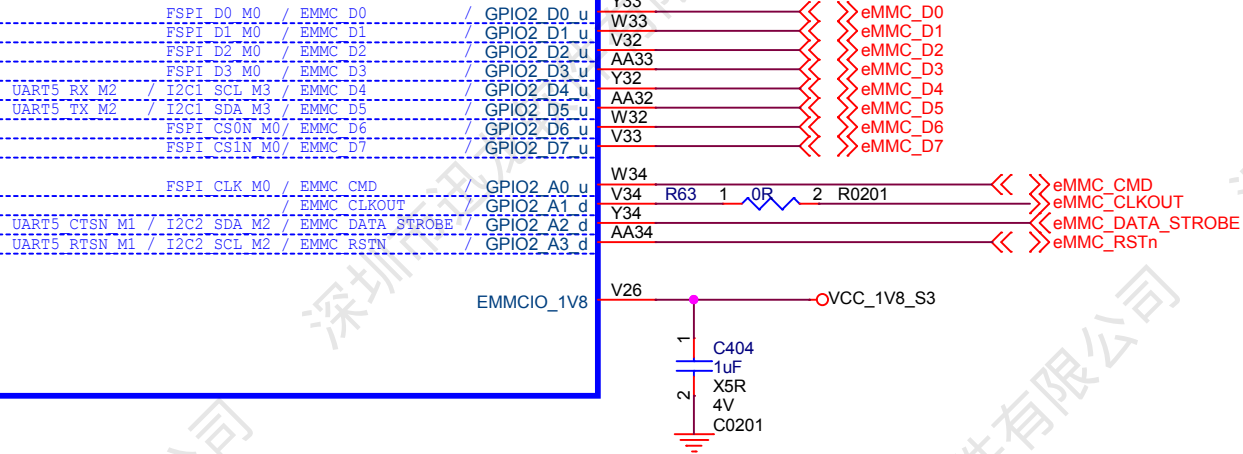


RK3588_C (EMMCIO Domain)

U4C

EMMCIO Domain

Operating Voltage=1.8V



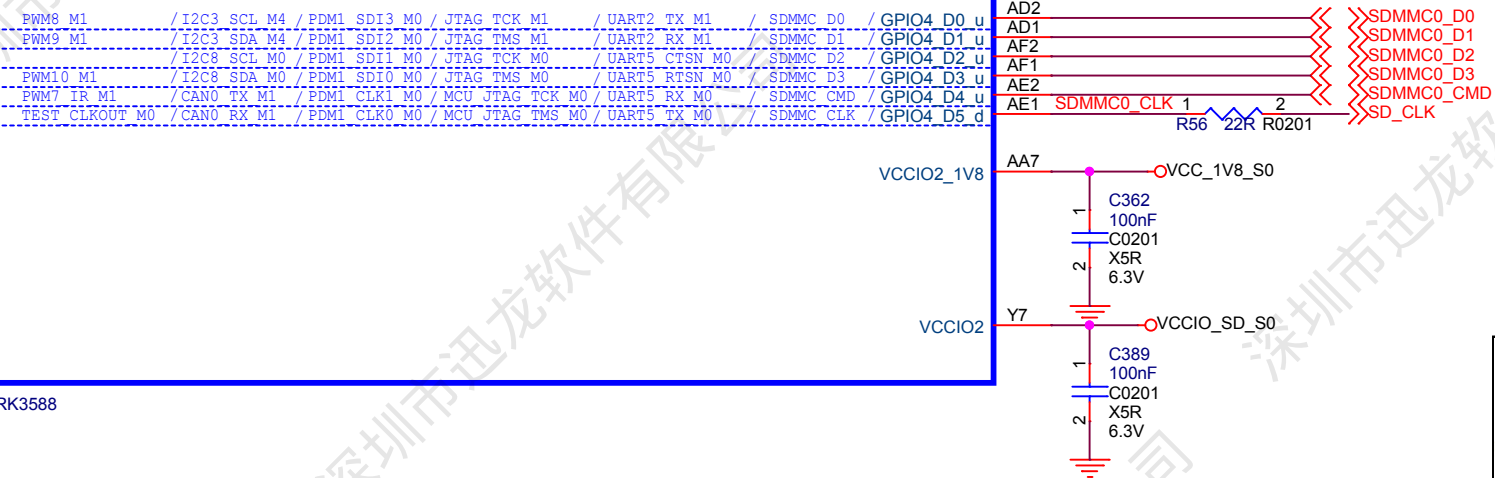
RK3588

RK3588 D (VCCIO2 Domain)

U4D

VCCI02 Domain

Operating Voltage=1.8V/3.3V



RK3588



Shenzhen Xunlong Software Co., Ltd

Project:	OPI 5 PLUS
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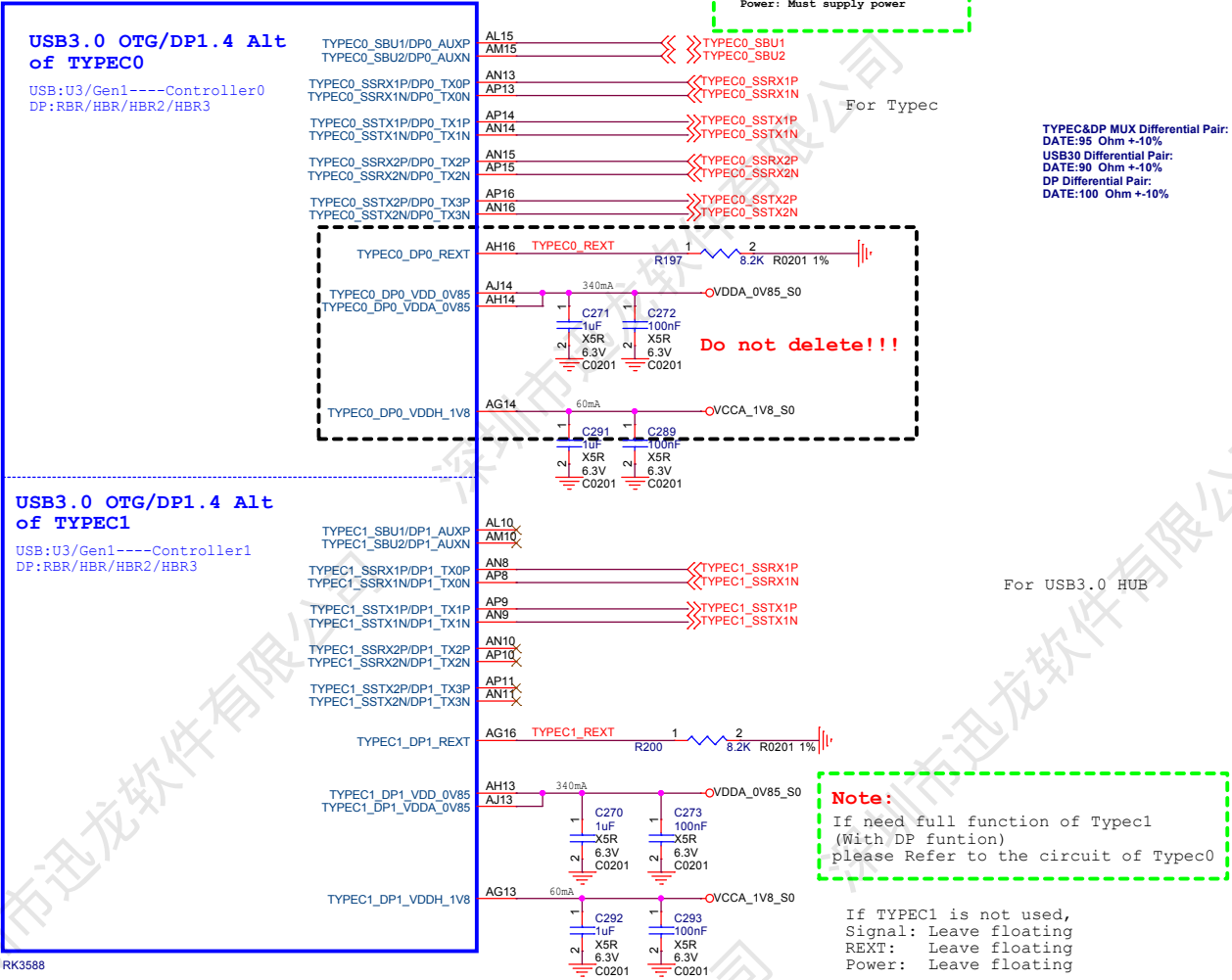
File: 13.RK3588_Flash/SD Controller

Date:	Friday, July 25, 2025	Rev:	V1.3.1
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Size:	A3	Sheet:	13	Of:	33
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RK3588_M(TYPEC/DP)

U4M



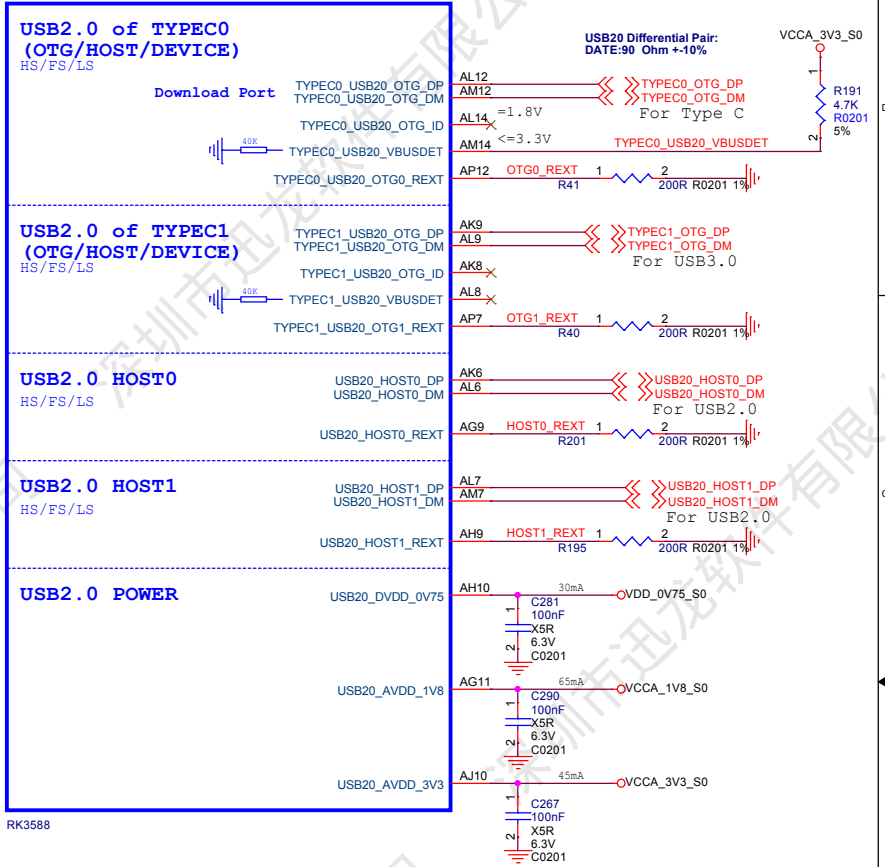
RK3588

USB30/DP1.4 Alt Mode Configuration

Option1	DP x4Lane	DP_TX_Lane0-3
Option2	USB30 x4Lane	TYPEC_SSTX1P/1N&TYPEC_SSRX1P/1N or TYPEC_SSTX2P/2N&TYPEC_SSRX2P/2N
Option3	USB30X2Lane+DPX2Lane	USB30: Lane0 Lane1 DP: Lane2 Lane3
Option4	USB30X2Lane+DPX2Lane	USB30: Lane2 Lane3 DP: Lane0 Lane1

RK3588_L(USB2.0 HOST/OTG)

U4L



RK3588



Shenzhen Xunlong Software Co., Ltd			
Project:	OPI 5 PLUS		
File:	14.RK3588_USB30/USB20_Ctrl		
Date:	Friday, July 25, 2025	Rev:	V1.3.1
Size:	A3	Sheet:	14 Of: 33

U4G



U4U



RK3588

TABLE 1

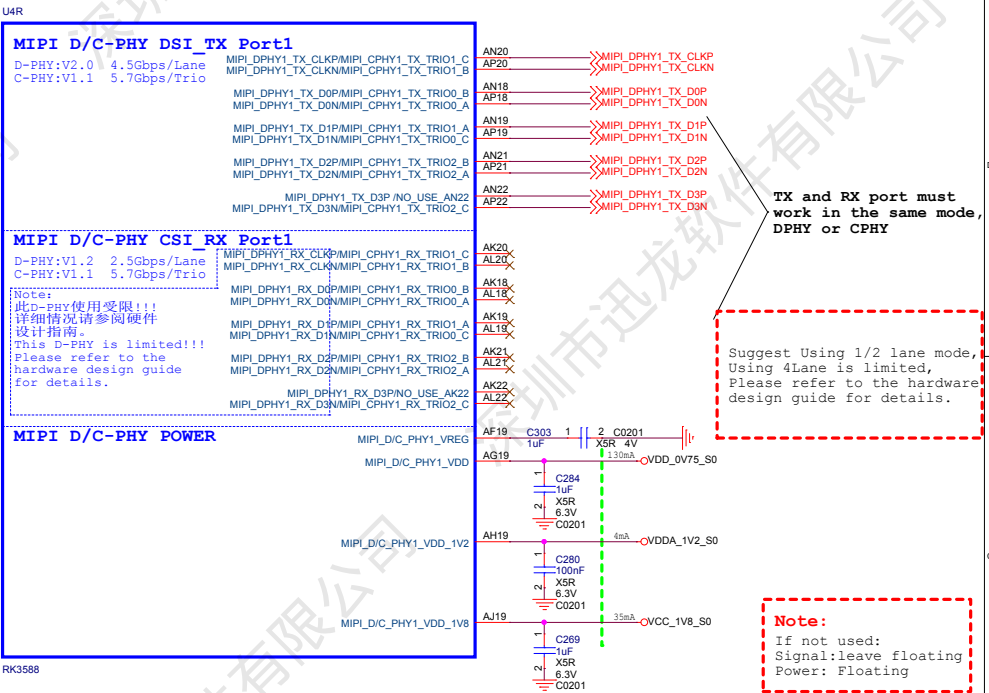
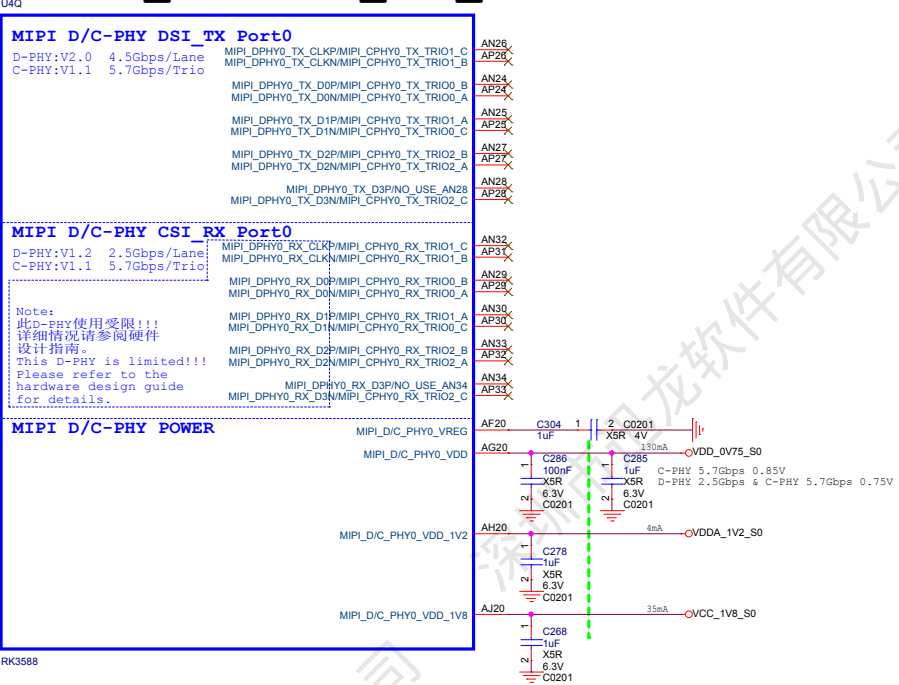
1

U

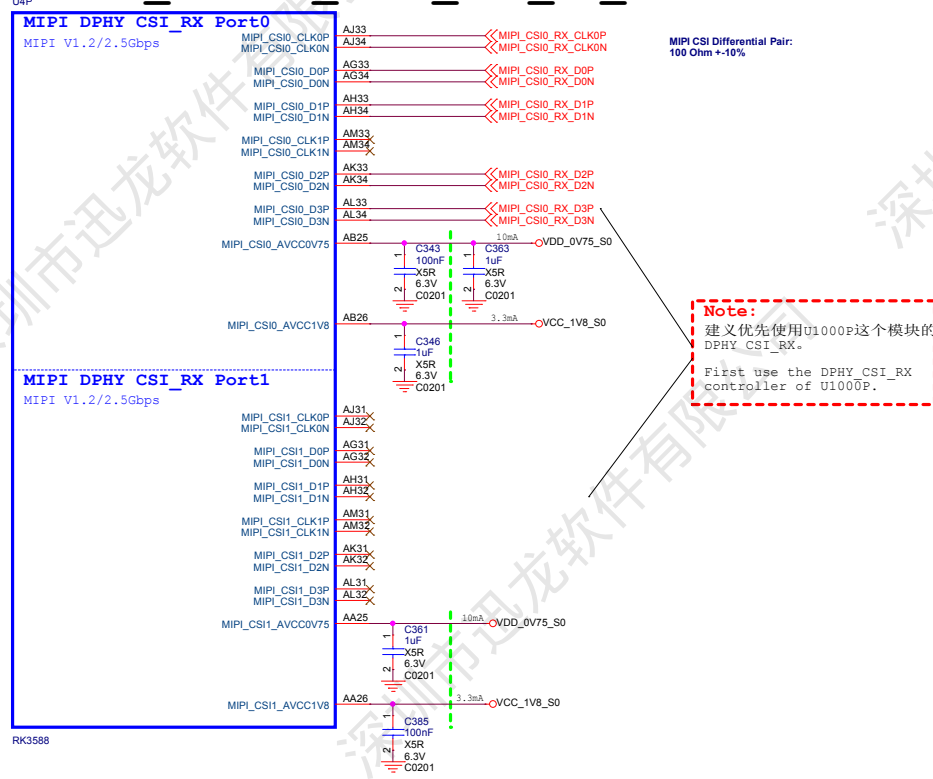


Project:	OPI 5 PLUS				
File:	15.RK3588_SARADC/1.8V Only GPIO				
Date:	Friday, July 25, 2025			Rev:	V1.3.4
Size:	A3	Sheet:	15	Of:	33

RK3588_Q/R(MIPI_D/C_PHY0/1)



RK3588_P(MIPI_DPHY_CSI_RX_PHY)



MIPI_CSI_RX Configuration

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3, but clock lane1 is invalid; In dual clock lanes mode, CLK0P/0N is the clock lane of Data lane0 and Data lane1, while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
The Caps to the left of green line should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588_S (HDMI2.1 TX)

RK3588_T (HDMI20 RX)

Note:

The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

U4S

HDMI TX/eDP MUX Port0

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps

HDMI_TX0_SBDP/EDP_TX0_AUXP
HDMI_TX0_SBDN/EDP_TX0_AUXN

HDMI_TX0_D0P/EDP_TX0_D0P
HDMI_TX0_D0N/EDP_TX0_D0N

HDMI_TX0_D1P/EDP_TX0_D1P
HDMI_TX0_D1N/EDP_TX0_D1N

HDMI_TX0_D2P/EDP_TX0_D2P
HDMI_TX0_D2N/EDP_TX0_D2N

HDMI_TX0_D3P/EDP_TX0_D3P
HDMI_TX0_D3N/EDP_TX0_D3N

HDMI/EDP_TX0_REXT

HDMI/EDP_TX0_VDD_0V75

HDMI/EDP_TX0_AVDD_0V75

HDMI/EDP_TX0_VDD_IO_1V8
HDMI/EDP_TX0_VDD_CMN_1V8

HDMI TX/eDP MUX Port1

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps

HDMI_TX1_SBDP/EDP_TX1_AUXP
HDMI_TX1_SBDN/EDP_TX1_AUXN

HDMI_TX1_D0P/EDP_TX1_D0P
HDMI_TX1_D0N/EDP_TX1_D0N

HDMI_TX1_D1P/EDP_TX1_D1P
HDMI_TX1_D1N/EDP_TX1_D1N

HDMI_TX1_D2P/EDP_TX1_D2P
HDMI_TX1_D2N/EDP_TX1_D2N

HDMI_TX1_D3P/EDP_TX1_D3P
HDMI_TX1_D3N/EDP_TX1_D3N

HDMI/EDP_TX1_REXT

HDMI/EDP_TX1_VDD_0V75

HDMI/EDP_TX1_AVDD_0V75

HDMI/EDP_TX1_VDD_IO_1V8
HDMI/EDP_TX1_VDD_CMN_1V8

AG2 >>> HDMI0_TX_SBDP/eDP0_TX_AUXP
AG1 >>> HDMI0_TX_SBDN/eDP0_TX_AUXN

AJ2 >>> HDMI0_TX0P_PORT/eDP0_TX_D0P
AJ1 >>> HDMI0_TX0N_PORT/eDP0_TX_D0N

AK3 >>> HDMI0_TX1P_PORT/eDP0_TX_D1P
AK2 >>> HDMI0_TX1N_PORT/eDP0_TX_D1N

AL2 >>> HDMI0_TX2P_PORT/eDP0_TX_D2P
AL1 >>> HDMI0_TX2N_PORT/eDP0_TX_D2N

AH3 >>> HDMI0_TX3P_PORT/eDP0_TX_D3P
AH2 >>> HDMI0_TX3N_PORT/eDP0_TX_D3N

AM2 >>> HDMI_TX0_REXT R51 1 2 8.2K R0201 1%

AA9 <260mA 440mA >>> HDMI_VDDA0V85_S0

C375 4.7uF X5R VDD_IO<77mA VDD_CMN<71mA Actual Setting 0.8375V

AB9 <1mA C0402_BGA

C330 1uF X5R 6.3V C0201

AC7 >>> VCC_1V8_S0

AC6 C319 1uF X5R 6.3V C0201

C310 100nF X5R 10V C0402_BGA

C282 4.7uF X5R 10V C0402_BGA

AN2 >>> HDMI1_TX_SBDP/eDP1_TX_AUXP
AP2 >>> HDMI1_TX_SBDN/eDP1_TX_AUXN

AN4 >>> HDMI1_TX0P_PORT/eDP1_TX_D0P
AP4 >>> HDMI1_TX0N_PORT/eDP1_TX_D0N

AM5 >>> HDMI1_TX1P_PORT/eDP1_TX_D1P
AN5 >>> HDMI1_TX1N_PORT/eDP1_TX_D1N

AN6 >>> HDMI1_TX2P_PORT/eDP1_TX_D2P
AP6 >>> HDMI1_TX2N_PORT/eDP1_TX_D2N

AM3 >>> HDMI1_TX3P_PORT/eDP1_TX_D3P
AN3 >>> HDMI1_TX3N_PORT/eDP1_TX_D3N

AN1 >>> HDMI_TX1_REXT R49 1 2 8.2K 1% R0201

AD9 <260mA 440mA >>> HDMI_VDDA0V85_S0

C311 1uF X5R 6.3V C0201

C342 100nF X5R 10V C0402_BGA

AC9 <1mA C0201

C341 1uF X5R 6.3V C0201

AD7 >>> VCC_1V8_S0

AD6 C323 1uF X5R 6.3V C0201

C332 100nF X5R 10V C0402_BGA

C336 4.7uF X5R 10V C0402_BGA

HDMI2.1_TX
100 Ohm +10%

U4T

HDMI RX

HDMI:V2.0

HDMI_RX_D0P

HDMI_RX_D0N

HDMI_RX_D1P

HDMI_RX_D1N

HDMI_RX_D2P

HDMI_RX_D2N

HDMI_RX_CLKP

HDMI_RX_CLKN

HDMI_RX_REXT

HDMI_RX_AVDD0V75

HDMI_RX_VPH3V3

HDMI_RX_DVDD3V3

AG5 >>> HDMI_RX_D0P

AG4 >>> HDMI_RX_D0N

AH6 >>> HDMI_RX_D1P

AH5 >>> HDMI_RX_D1N

AJ5 >>> HDMI_RX_D2P

AJ4 >>> HDMI_RX_D2N

AF6 >>> HDMI_RX_CLKP

AF5 >>> HDMI_RX_CLKN

AF3 >>> HDMI_RX_REXT

AE8 >>> VDD_0V75_S0

C299 1uF X5R 6.3V C0201

AE4 >>> VCCA_3V3_S0

AE5 C302 100nF X5R 6.3V C0201

C316 1uF X5R 6.3V C0201

Note:

If not used:
Signal:leave floating
Power: Floating

HDMI20_RX
100 Ohm +10%

Note:

The Caps to the left of green line should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

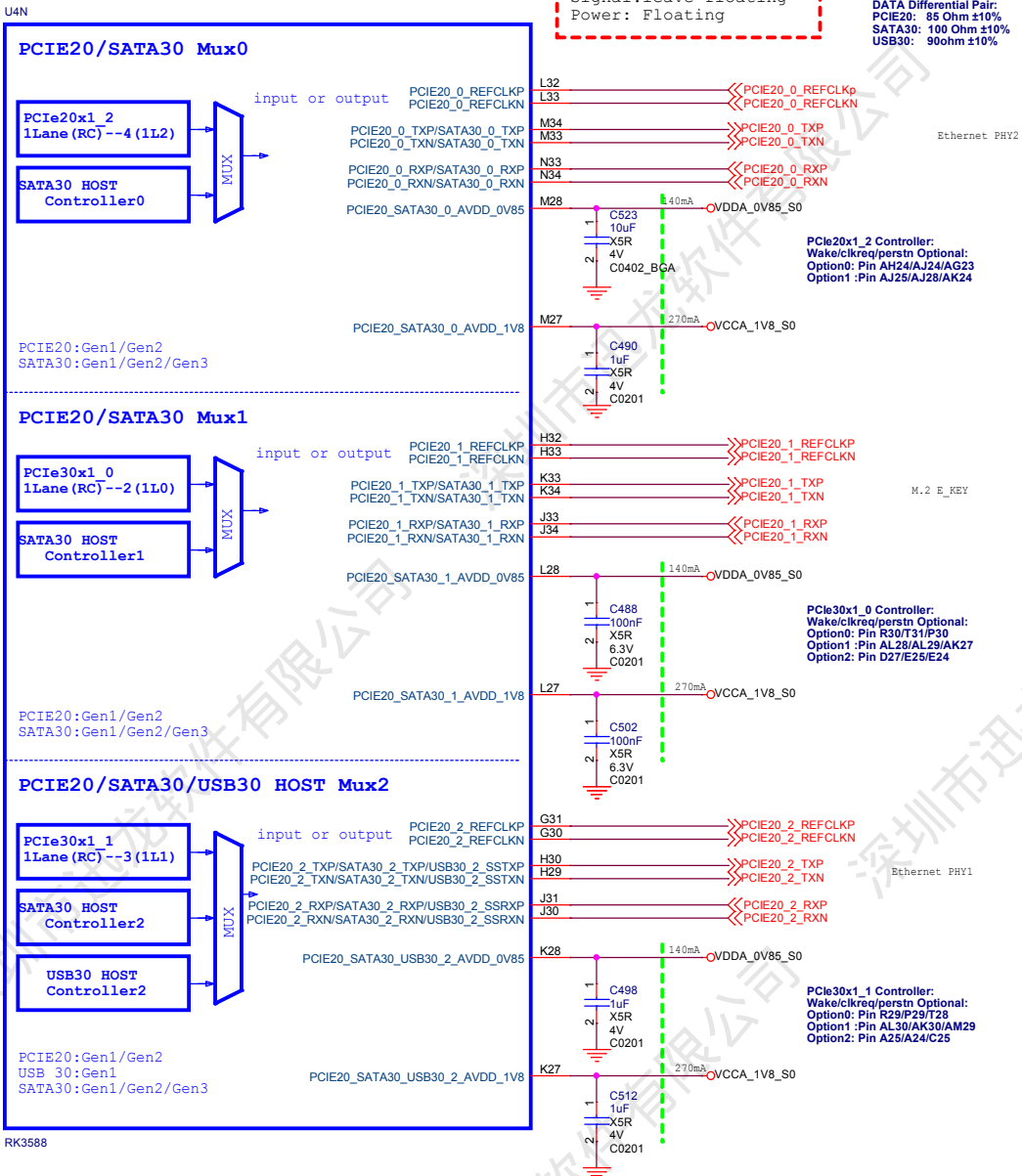
Note:

If not used:
Signal:leave floating
Power: Floating or tie to VSS



Shenzhen Xunlong Software Co., Ltd			
Project:	OPI 5 PLUS		
File:	17.RK3588_HDMI/eDP Interface		
Date:	Friday, July 25, 2025	Rev:	V1.3.1
Size:	A3	Sheet:	17
		Of:	33

RK3588_N (PCIE20)



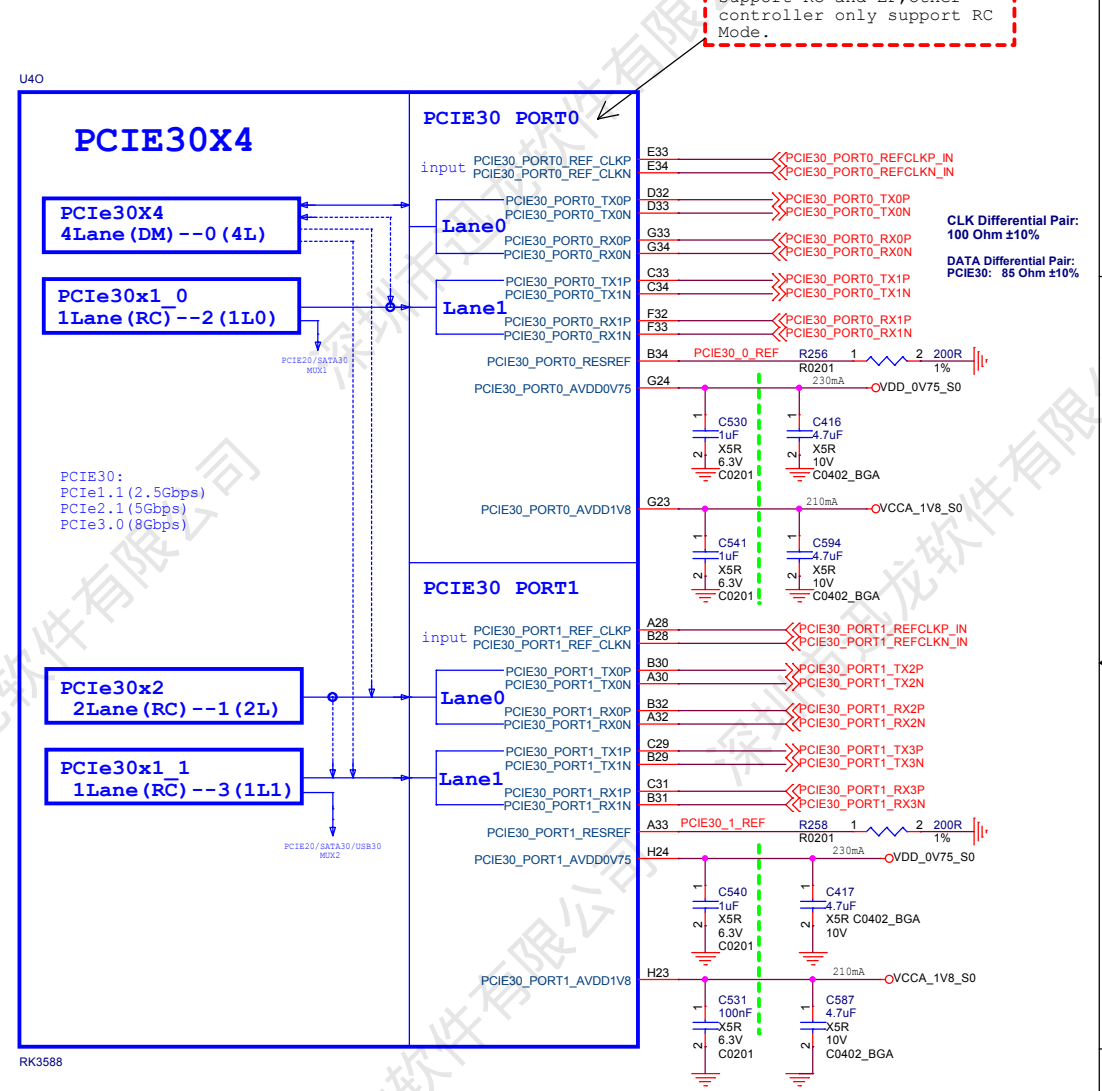
Note:

The SATA differential trace impedance is 100 OHM
The SATA trace length is less than 5 inch

Note:

每个SATA PORT最多只能扩展5个SATA，
不支持二级扩展。
Each sata port can only expand 5 sata
port at most, No support level-2 expand.

RK3588_O (PCIE30)



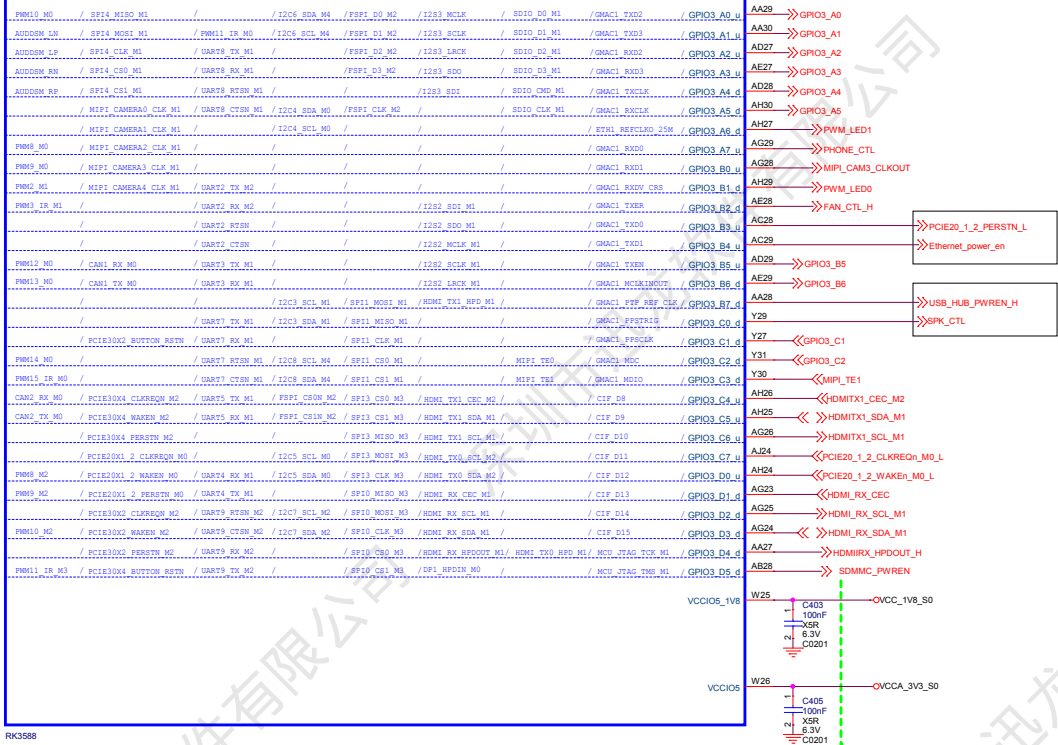
Shenzhen Xunlong Software Co., Ltd					
Project:	OPI 5 PLUS				
File:	18.RK3588_PCIE30/PCIE20/SATA30				
Date:	Friday, July 25, 2025	Rev:	V1.3.1		
Size:	A3	Sheet:	18	Of:	33

RK3588_J (VCCIO5 Domain)

U4J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V



RK3588_K (VCCIO6 Domain)

U4K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

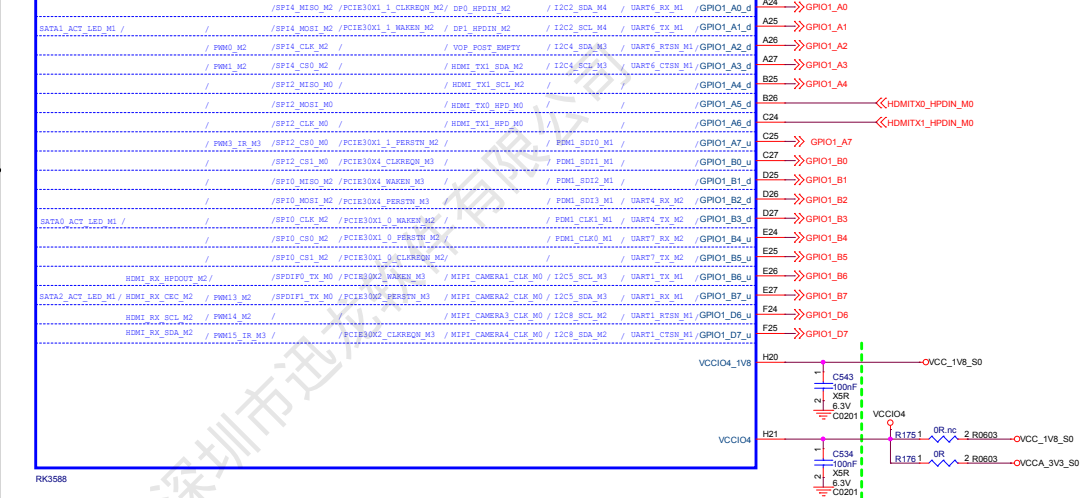


RK3588_I (VCCIO4 Domain)

U4I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V



D

C

B

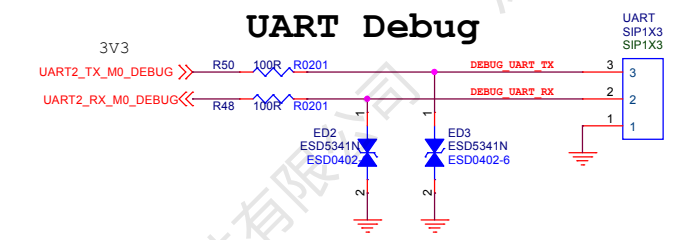
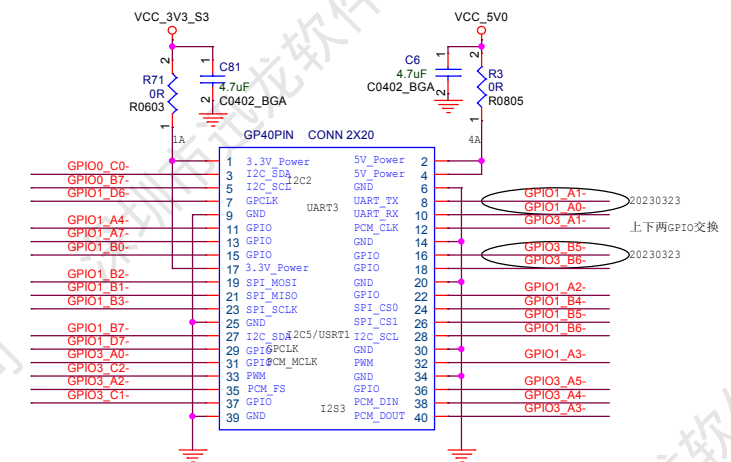
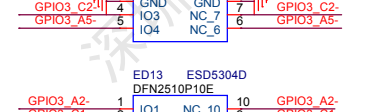
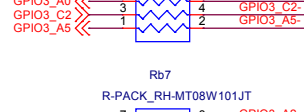
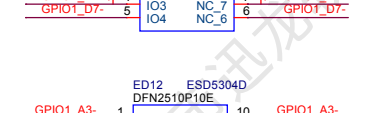
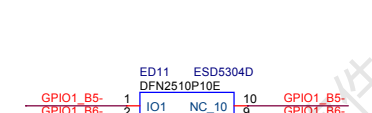
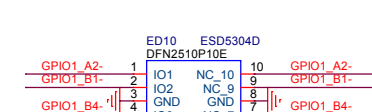
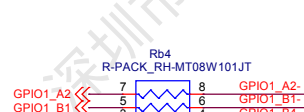
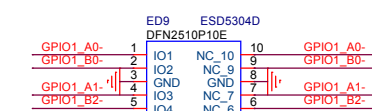
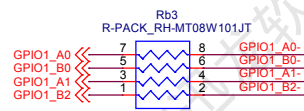
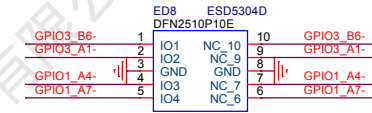
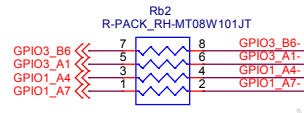
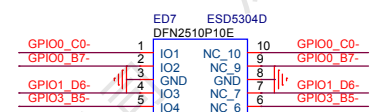
A

D

C

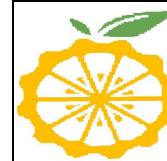
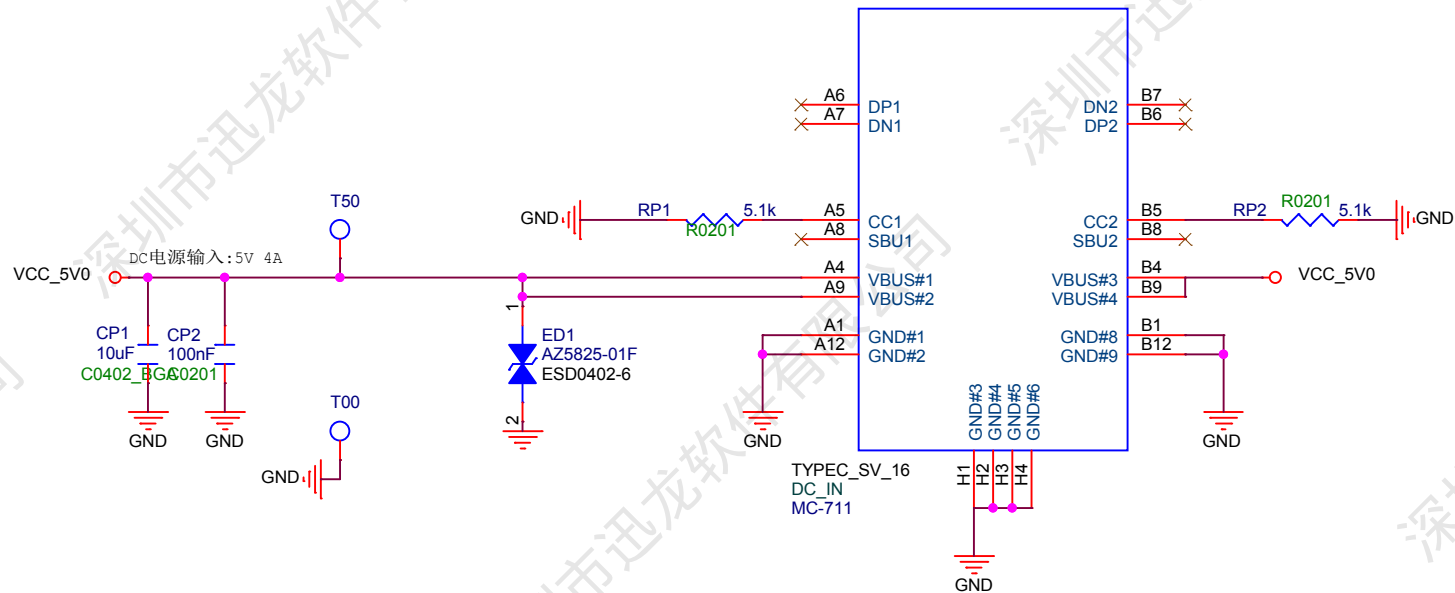
B

A



DCIN-5V/4A

TPYE-C POWER IN



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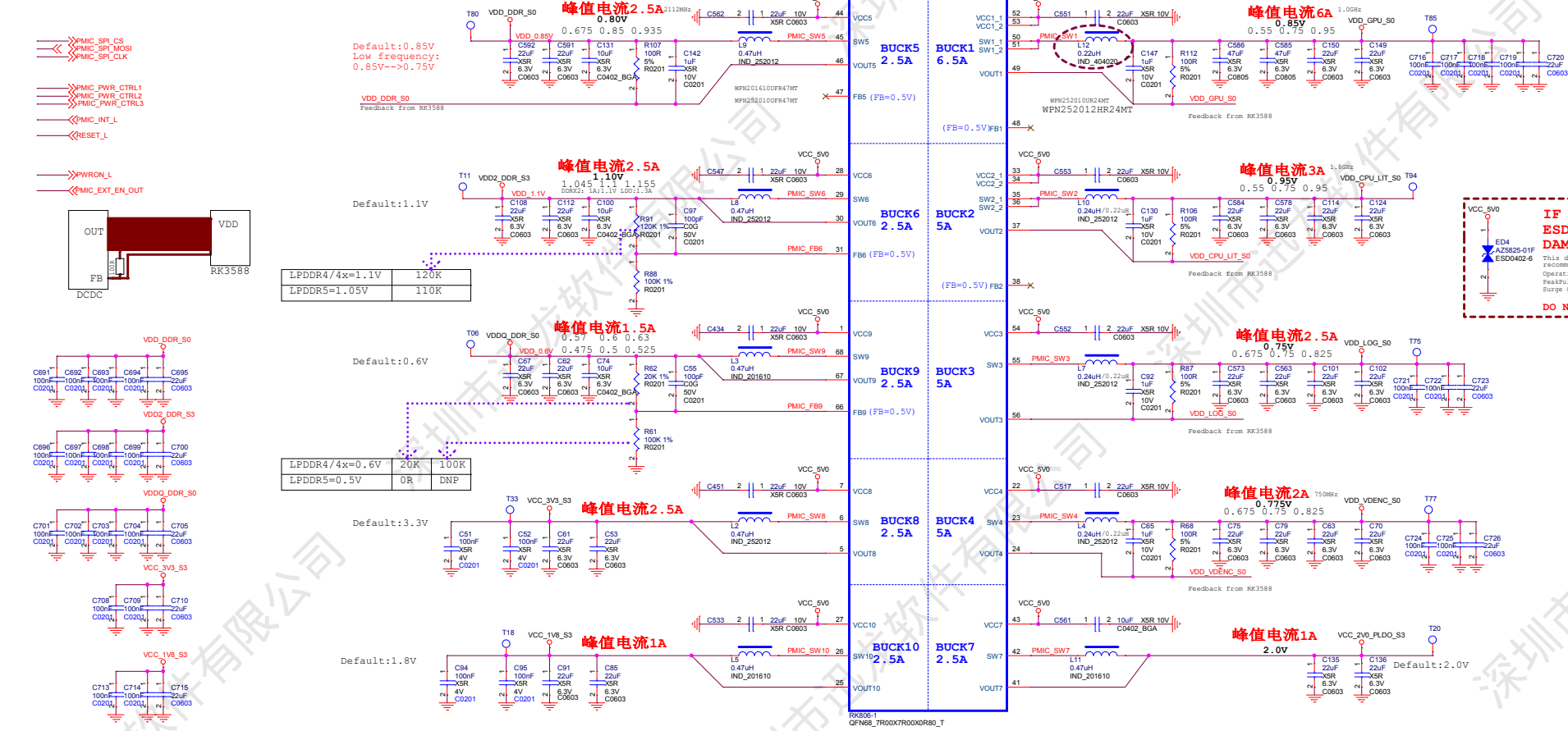
Project:	OPI 5 PLUS
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File:	21.Power_IN TYPE_C DC5V_4A
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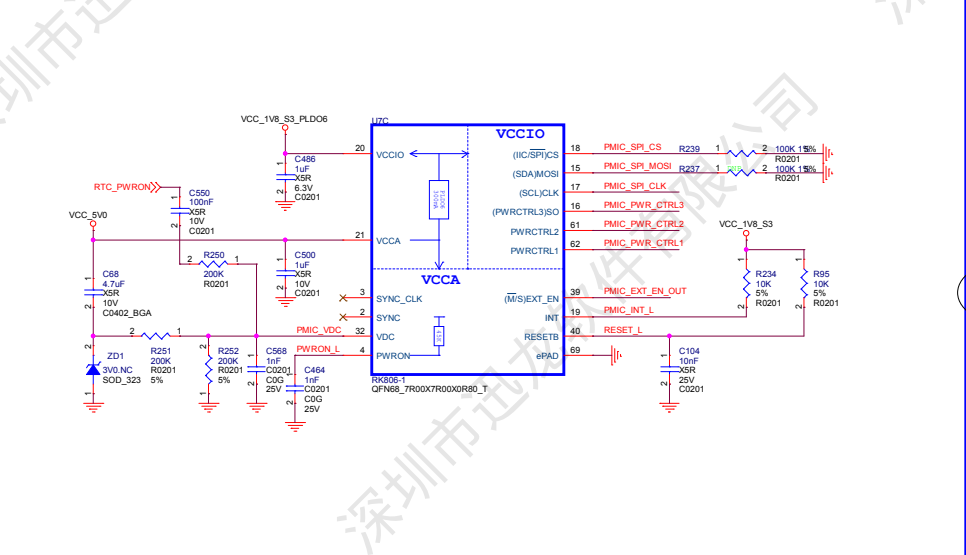
Date:	Friday, July 25, 2025	Rev:	V1.3.1
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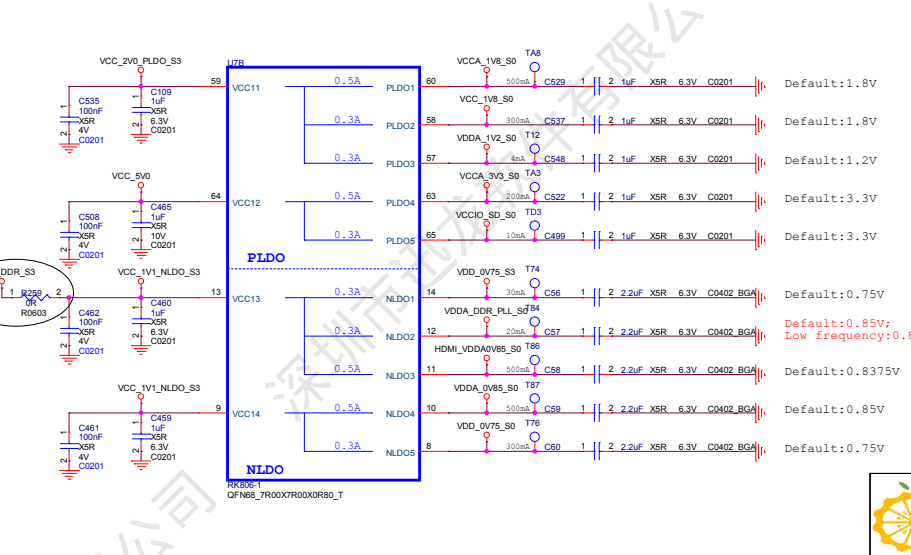
PMIC RK806-1 BUCK



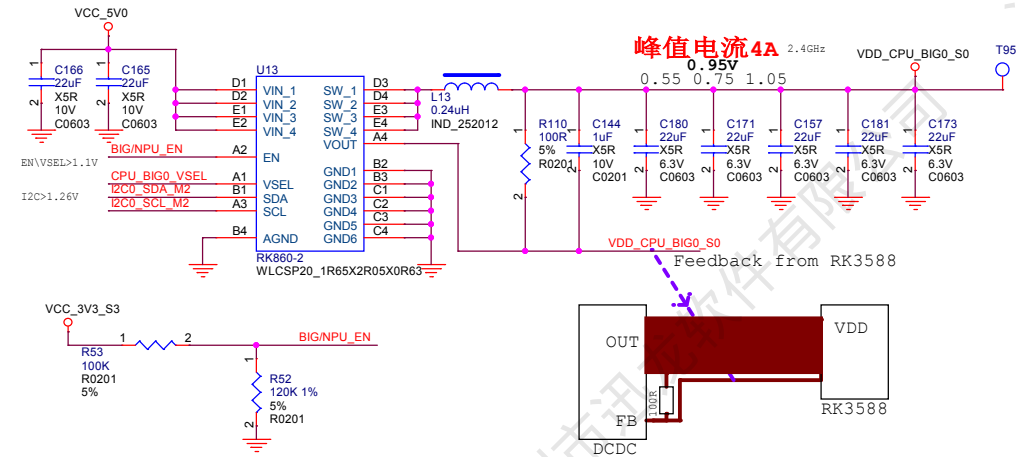
PMIC RK806-1 Managerment



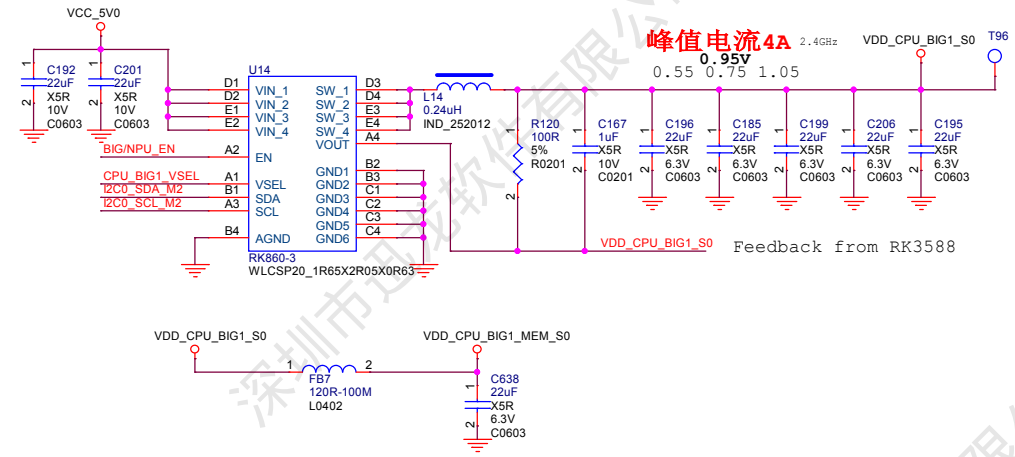
PMIC RK806-1 LDO



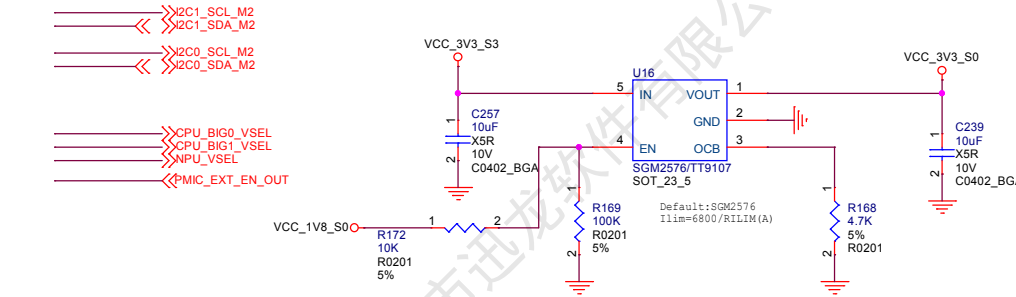
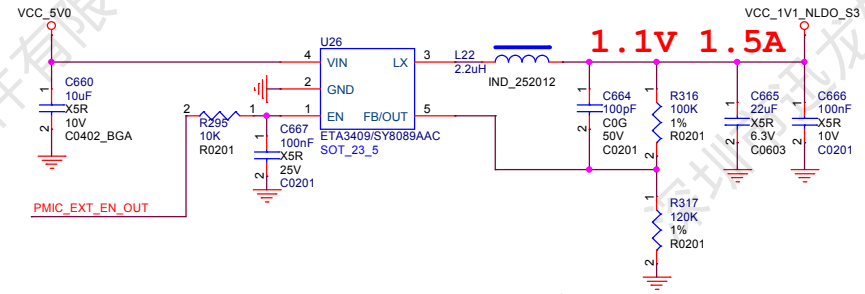
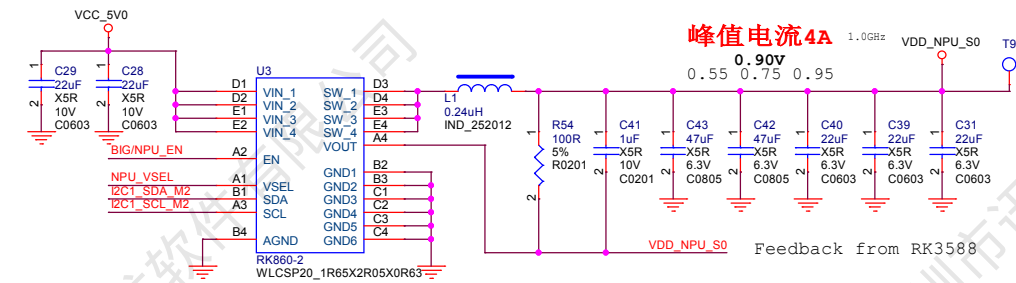
VDD_CPU_BIG0



VDD_CPU_BIG1

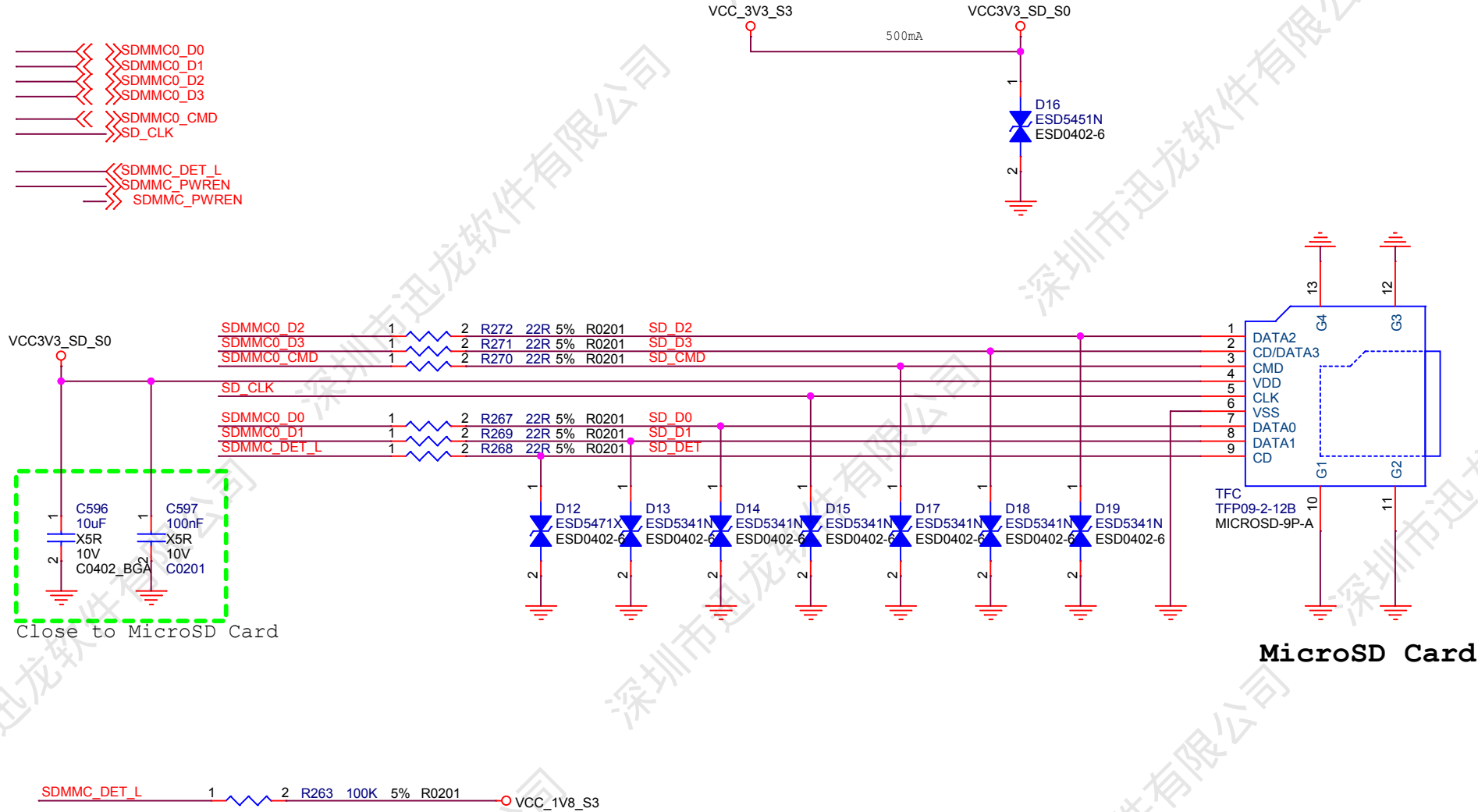


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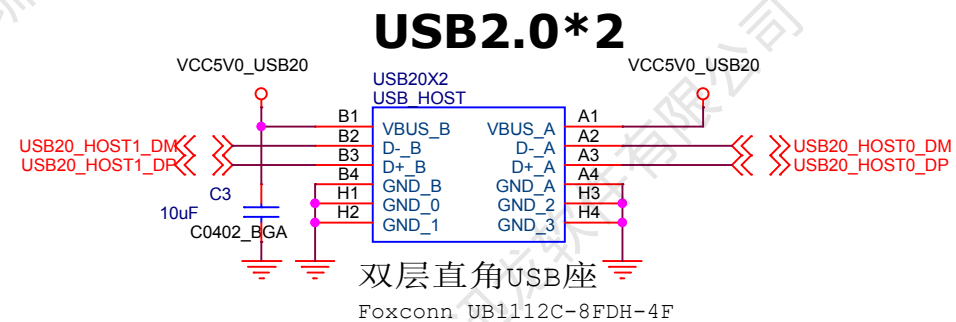
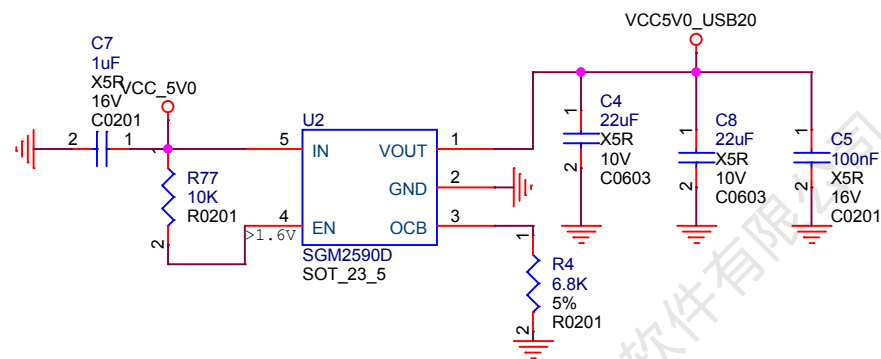


Shenzhen Xunlong Software Co., Ltd					
Project:	OPI 5 PLUS				
File:	23.Power_Ext Discrete				
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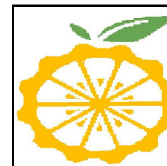
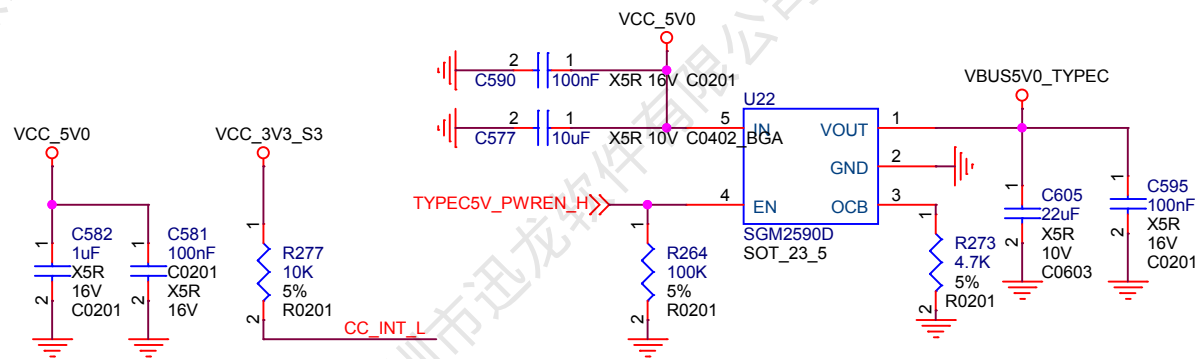
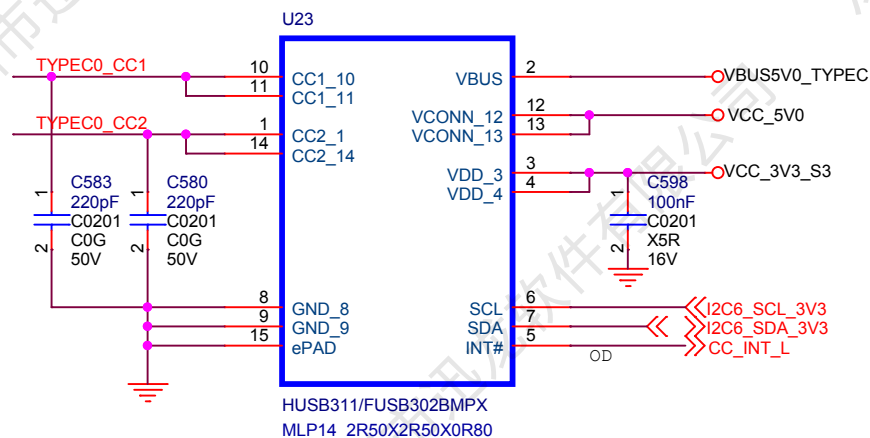
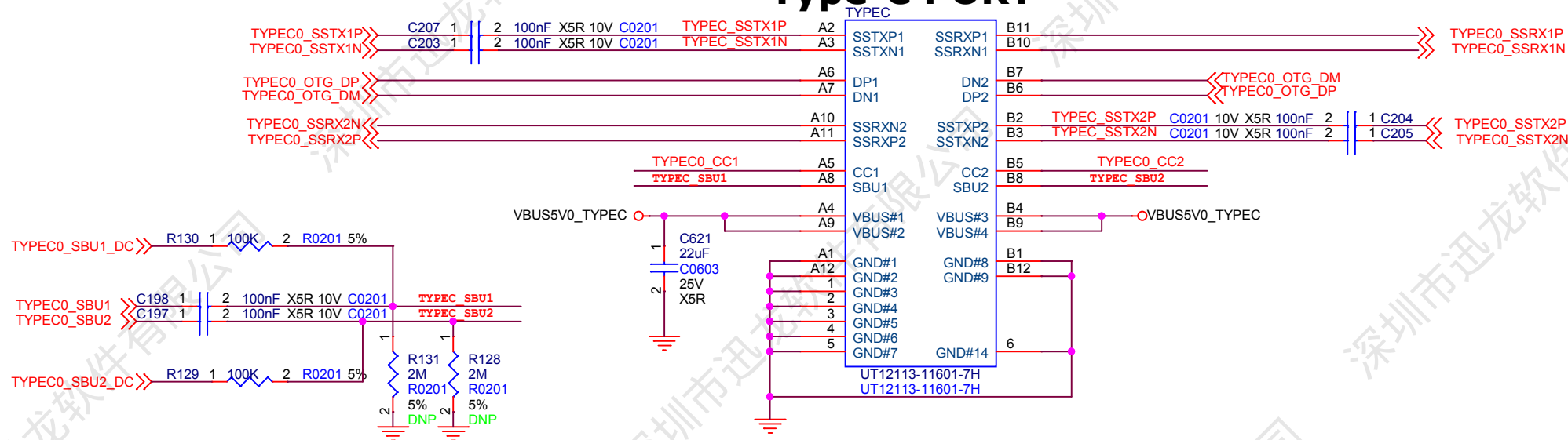
TF CARD



Shenzhen Xunlong Software Co., Ltd				
Project:	OPI 5 PLUS			
File:	24.Flash-TF Card			
Date:	Friday, July 25, 2025	Rev:	V1.3.1	
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Type-C PORT



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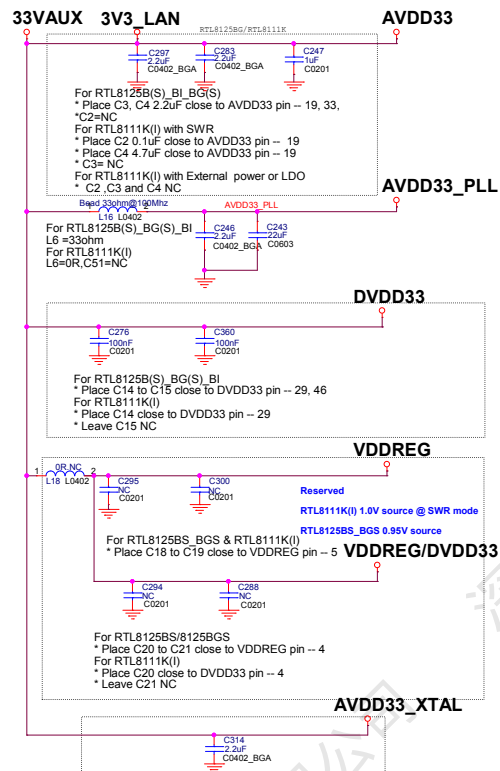
Project: OPI 5 PLUS

File: 26.Type C/USB2.0

Date: Friday, July 25, 2025

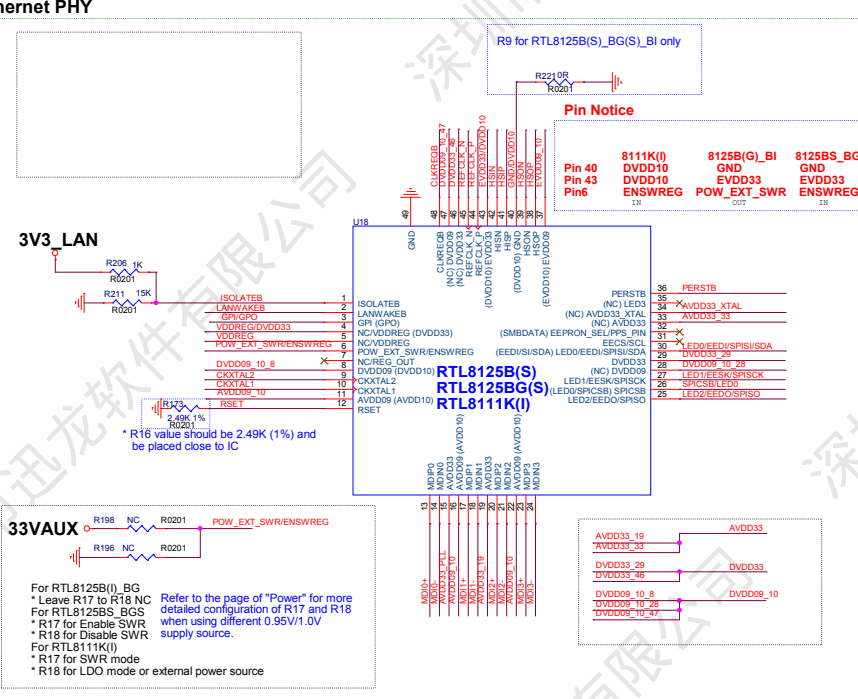
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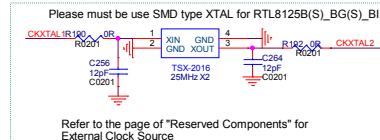


RTL	Core Source	C3	C15	C18	C19	C20	C21	C25
8111K(I)	SWR	X	X	O	O	O	X	X
	LDO	X	X	X	X	O	X	X
	EXTERNAL	X	X	X	X	O	X	X
8125BS	SWR	O	O	O	O	O	O	O
	EXTERNAL	O	O	X	X	X	X	O
8125BG	EXTERNAL	O	O	X	X	X	X	O

**RTL8125B(S)_BI_BG(S) 0.95V
RTL8111K(I) 1.0V**



Clock Source

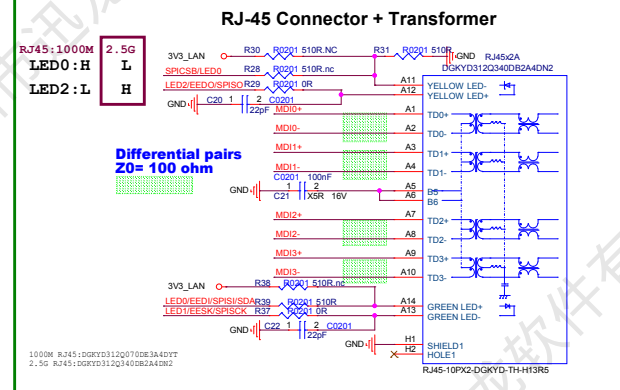
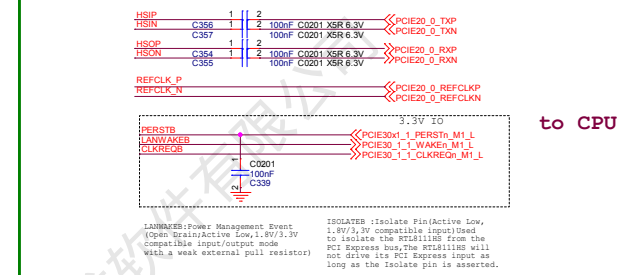


External Resistor

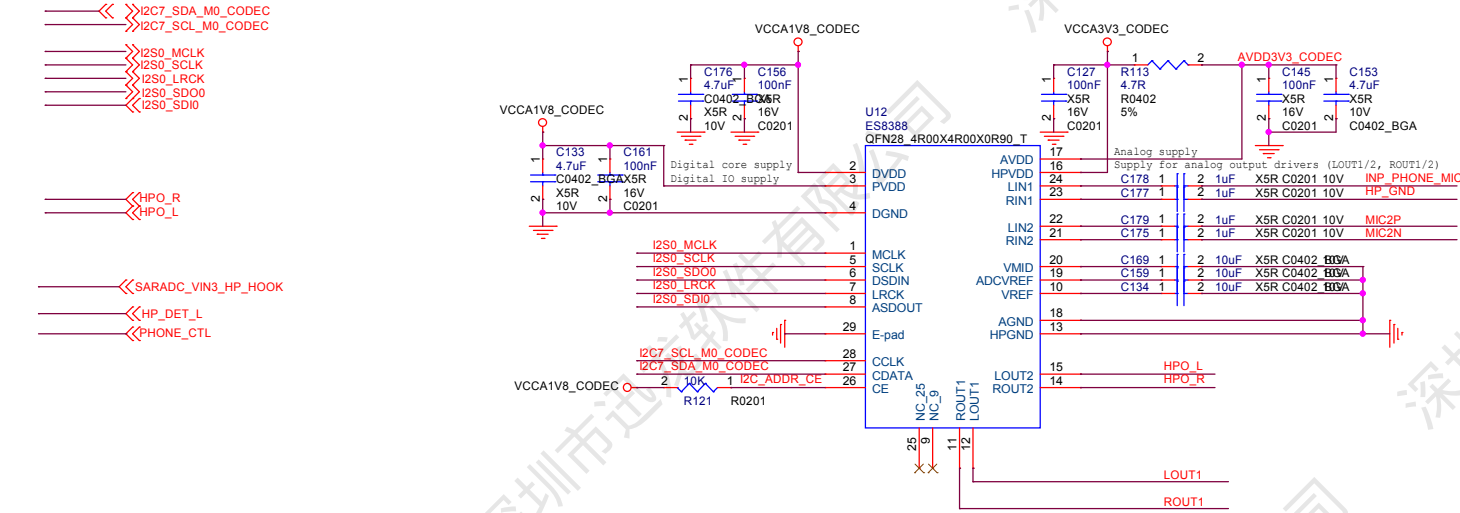


Core Source Option

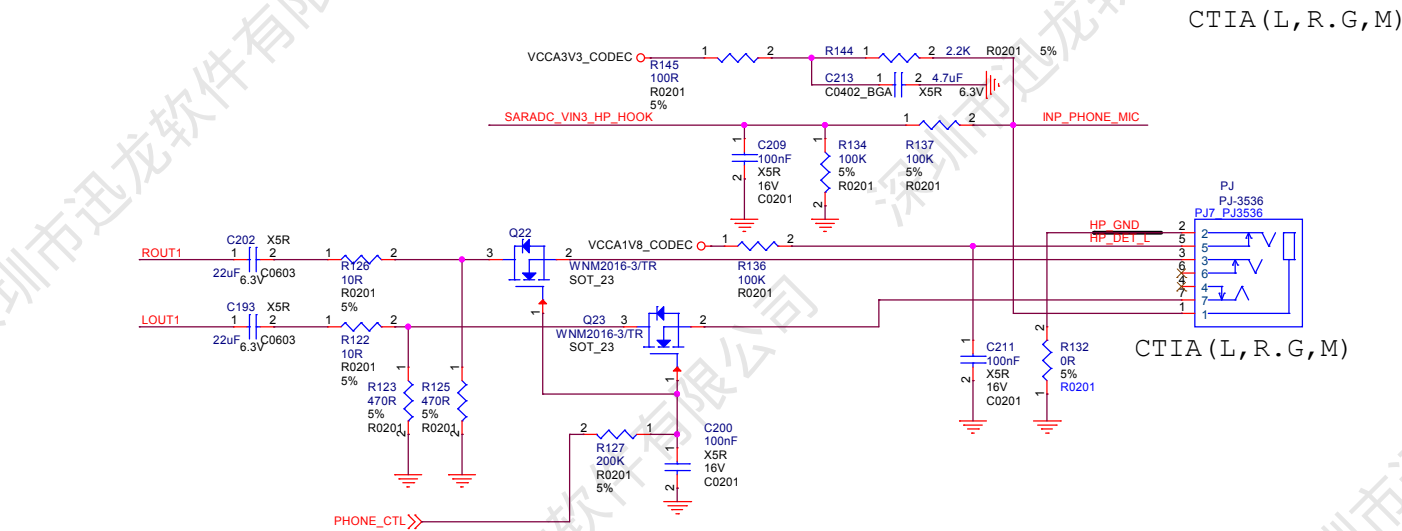
RTL	Core Source	C22	C23	C24	L1	R4	R5	R7	R17	R18	R34	R35
8111K(I)	SWR	X	O	O	O	X	O	X	O	X	X	X
	LDO	O	X	X	X	O	X	X	X	O	X	X
	EXTERNAL	X	X	X	X	X	X	O	X	O	O	X
8125BS	SWR	X	O	O	O	X	O	X	O	X	X	X
	EXTERNAL	X	X	X	X	X	X	O	X	O	O	X
8125BG	EXTERNAL	X	X	X	X	X	X	O	X	X	X	O



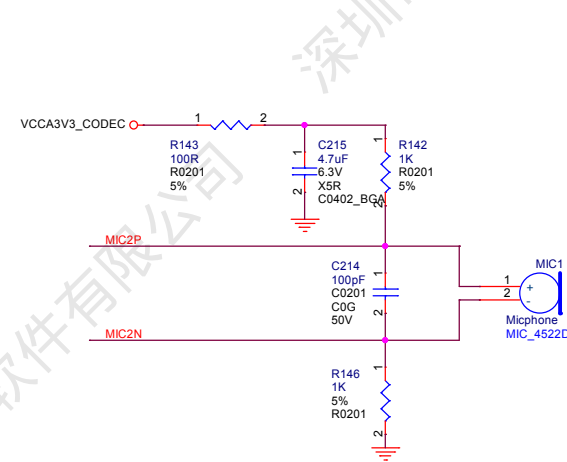
CODEC ES8388



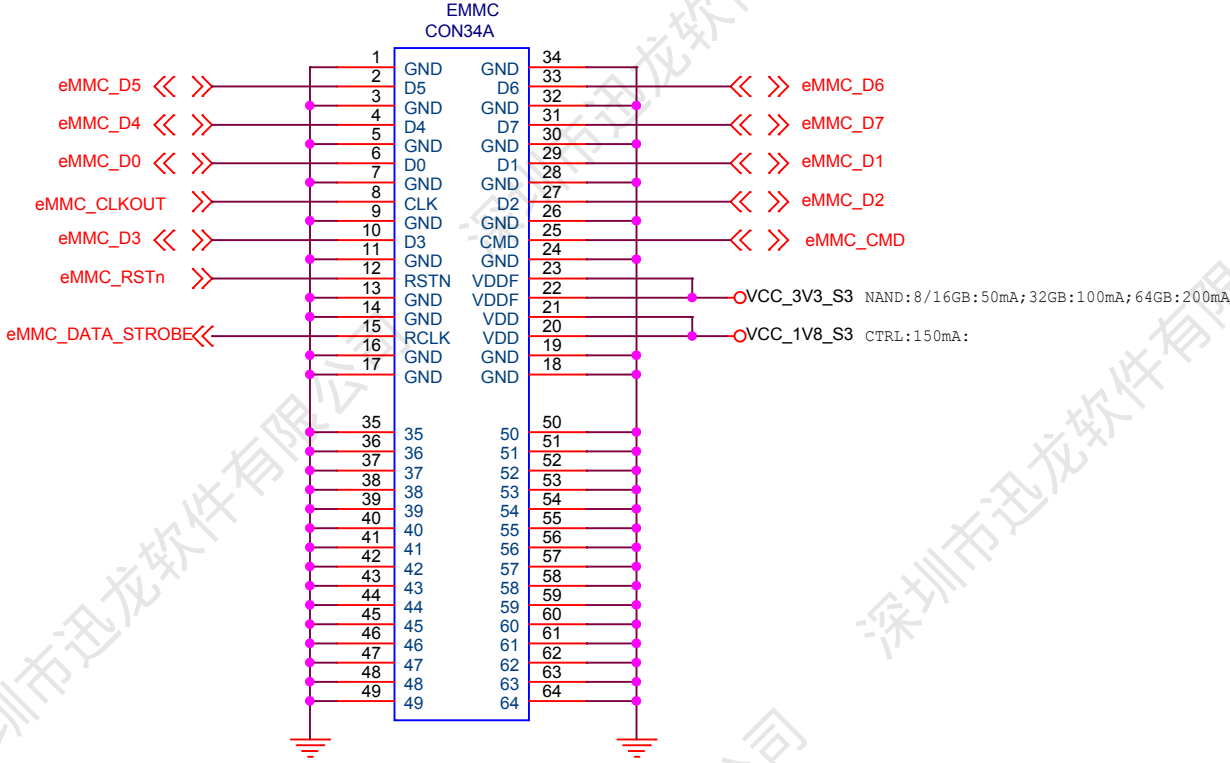
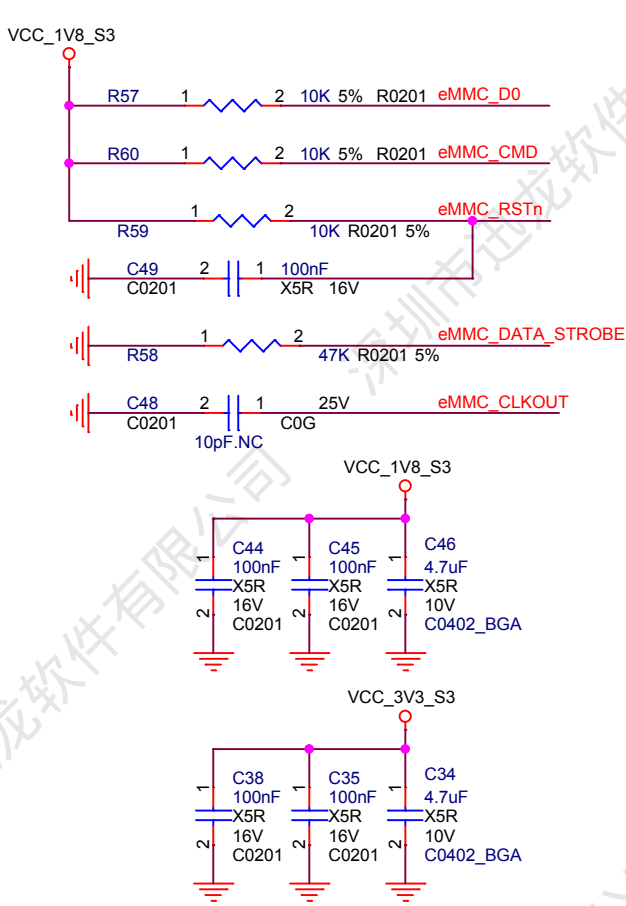
EARPHONE



Analog MIC



eMMC FLASH



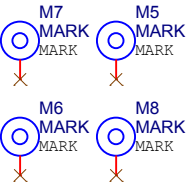
Shenzhen Xunlong Software Co., Ltd				
Project:	OPI 5 PLUS			
File:	31.Flash-eMMC Flash			
Date:	Friday, July 25, 2025	Rev:	V1.3.1	
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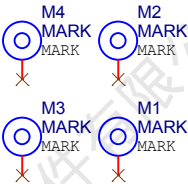


Mark

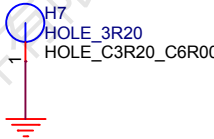
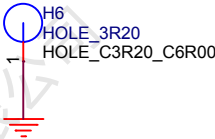
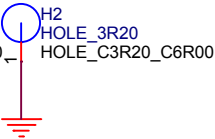
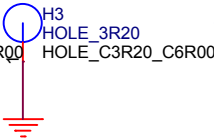
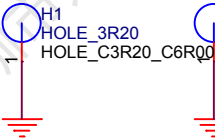
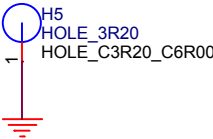
TOP Mark



BOTTOM Mark



HOLE



HEATSINK



Shenzhen Xunlong Software Co., Ltd				
Project:	OPI 5 PLUS			
File:	33.Mark/Hole/Heatsink			
Date:	Friday, July 25, 2025			Rev: V1.3.1
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