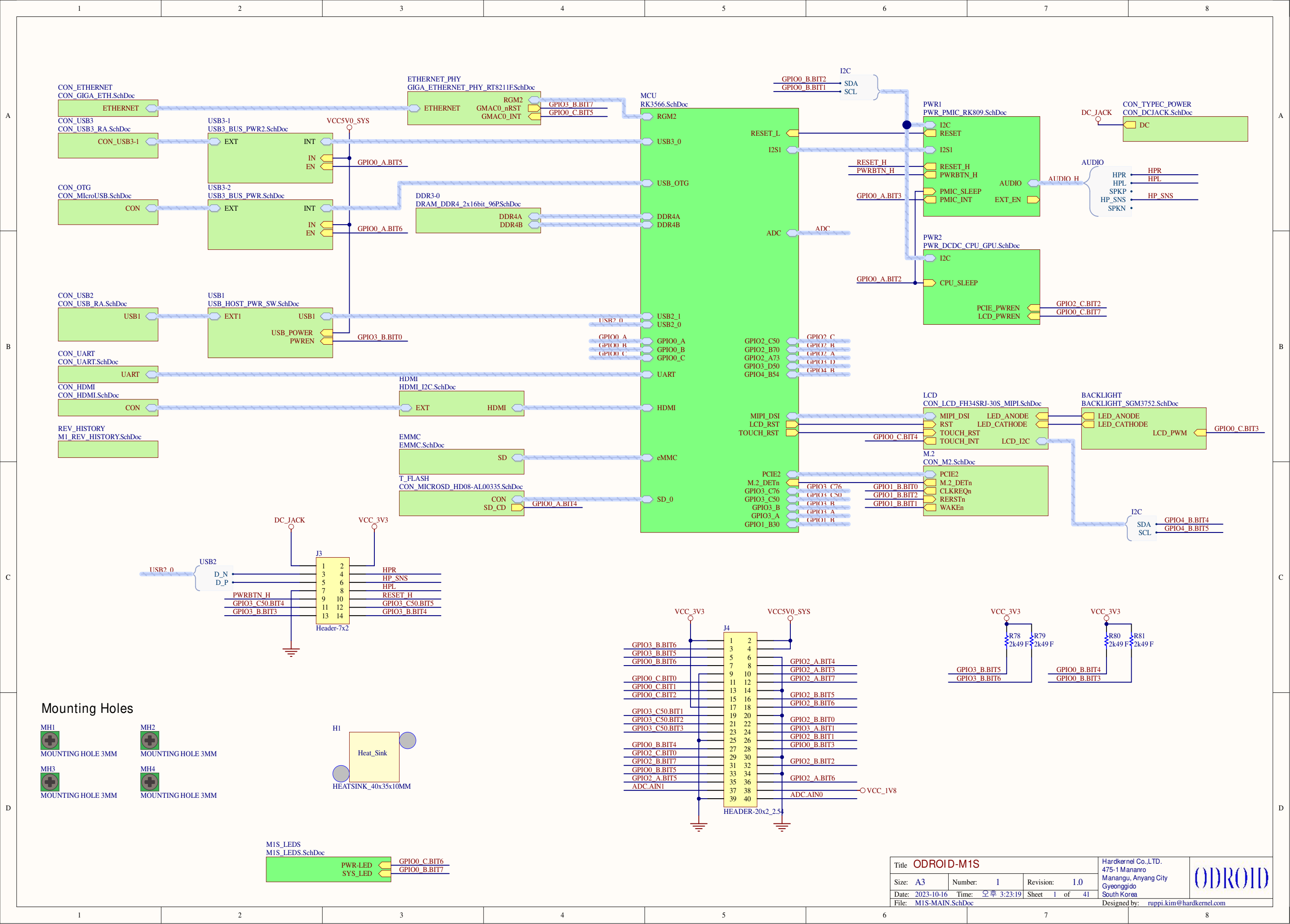
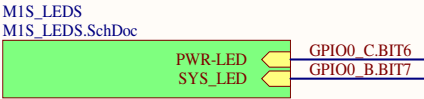
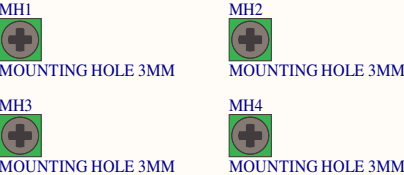




Mounting Holes



Title ODROID-M1S			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		
Size: A3	Number: 1	Revision: 1.0	Designed by: ruppi.kim@hardkernel.com		
Date: 2023-10-16	Time: 오후 3:23:19	Sheet 1 of 41			
File: M1S-MAIN.SchDoc					



A

B

C

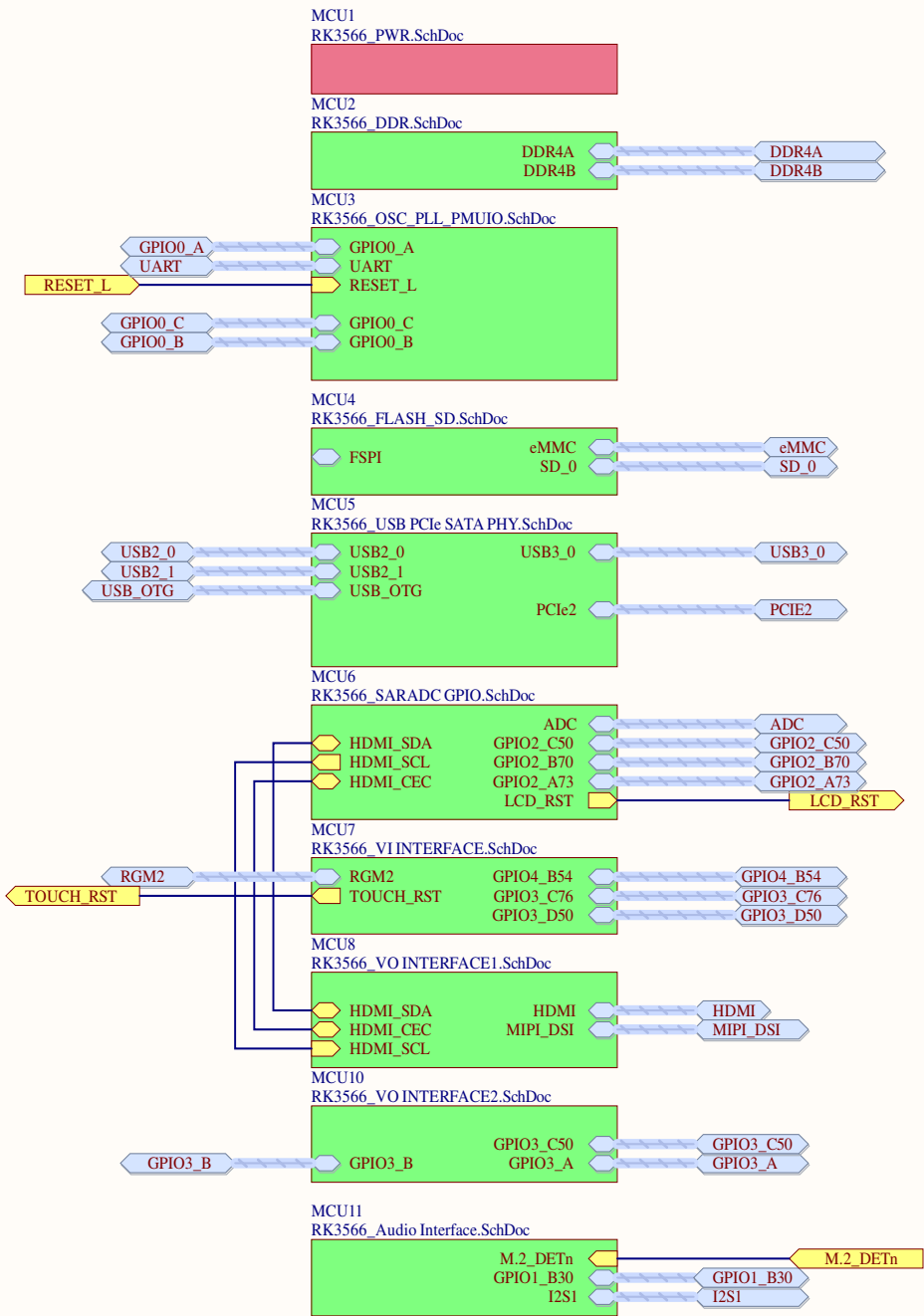
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A

B

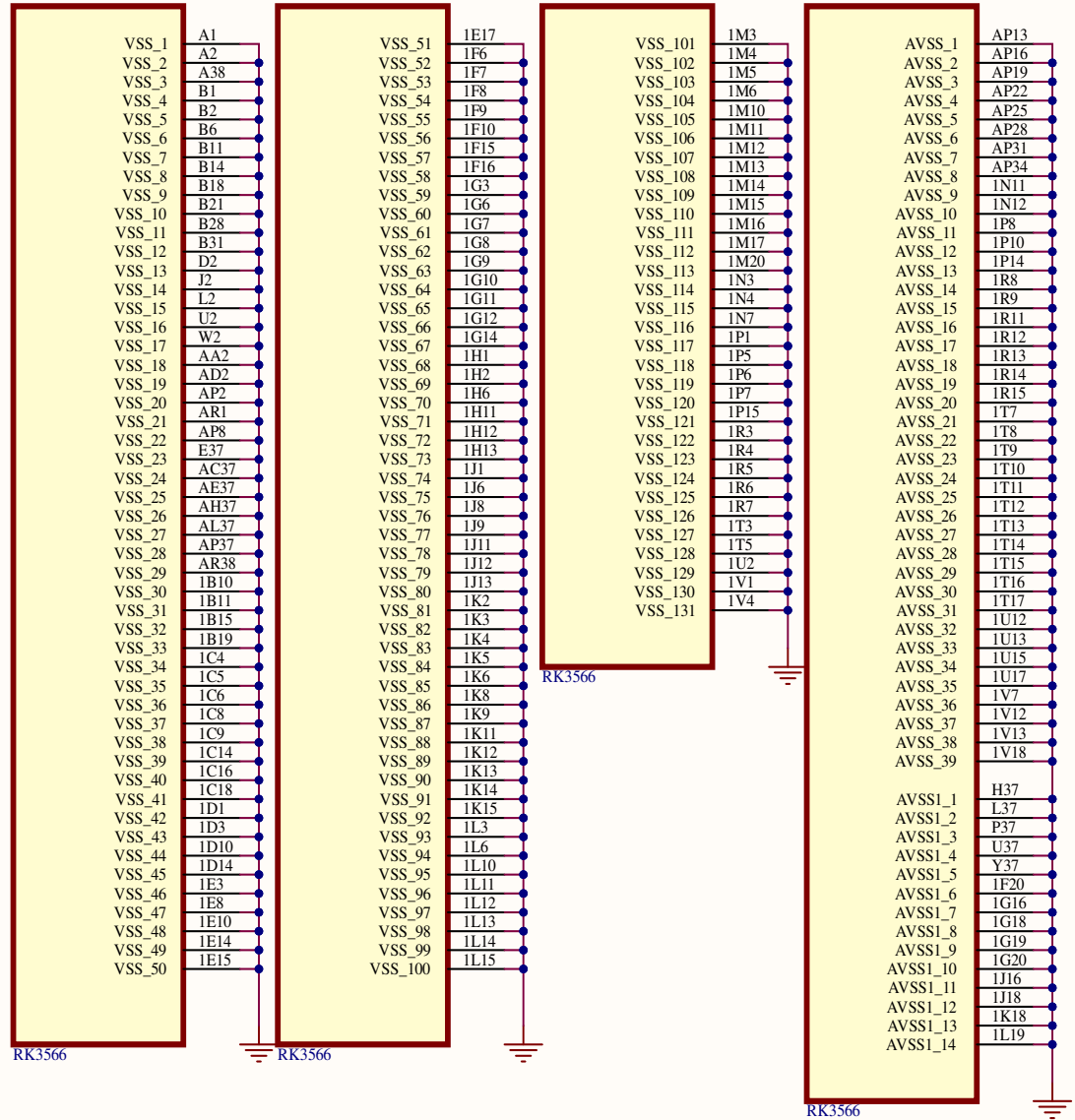
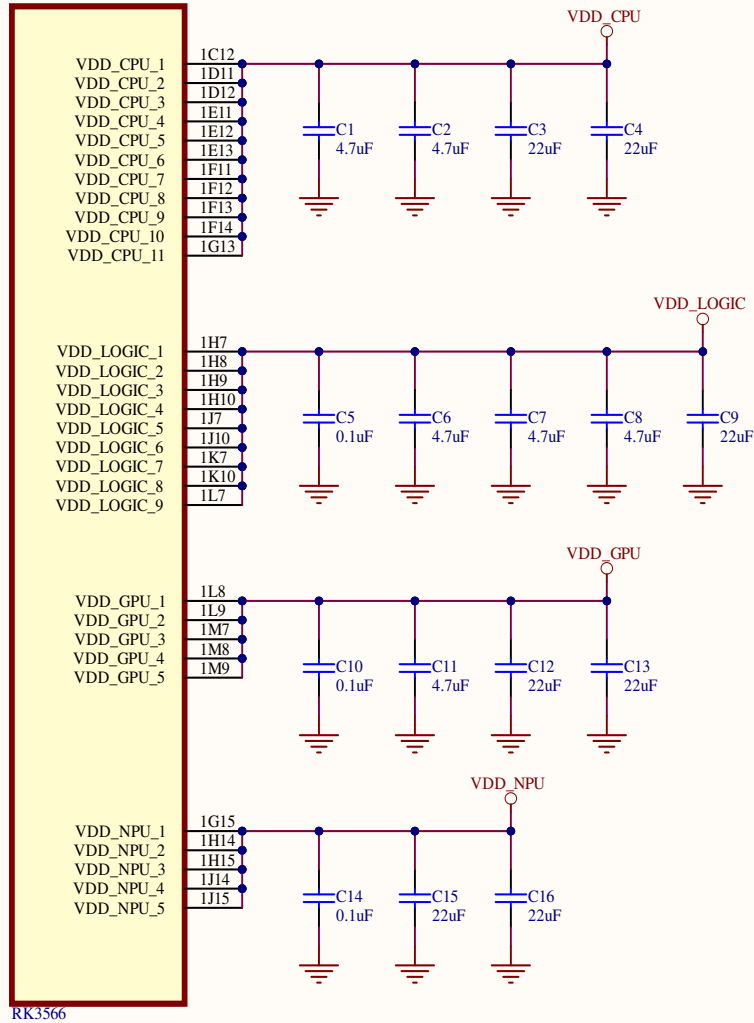
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D



Title			MCU RK3568		Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		
Size: A4		Number: 2	Revision: 0.1				
Date: 2023-10-16		Time: 오후 3:23:19	Sheet 2 of 41				
File: RK3566.SchDoc					Designed by: ruppi.kim@hardkernel.com		

RK3566_ABCDE (Power &Gnd)



Title **RK3566 POWER/GND**

Size: **A4**

Number: **3**

Revision: **1.0**

Date: **2023-10-16**

Time: **오후 3:23:19**

Sheet **3** of **41**

File: **RK3566_PWR.SchDoc**

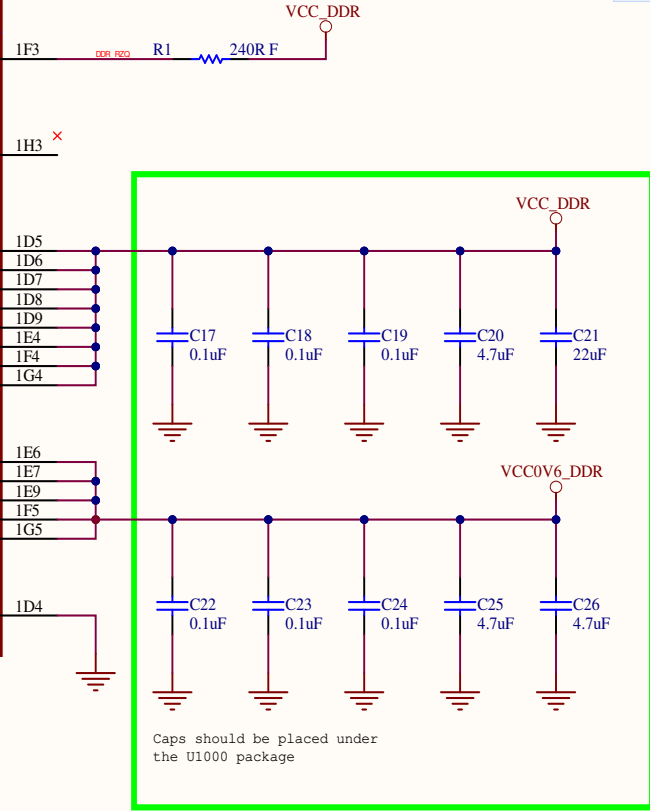
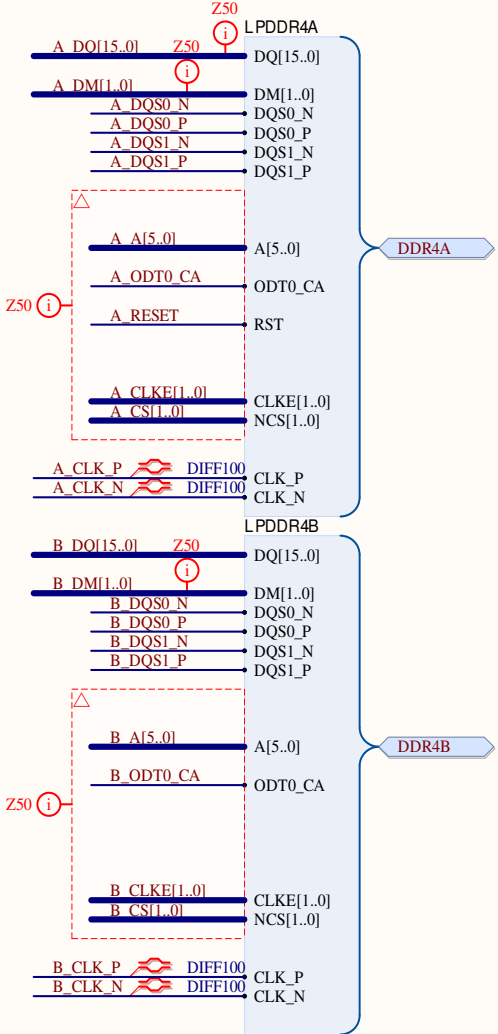
Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: **ruppi.kim@hardkernel.com**

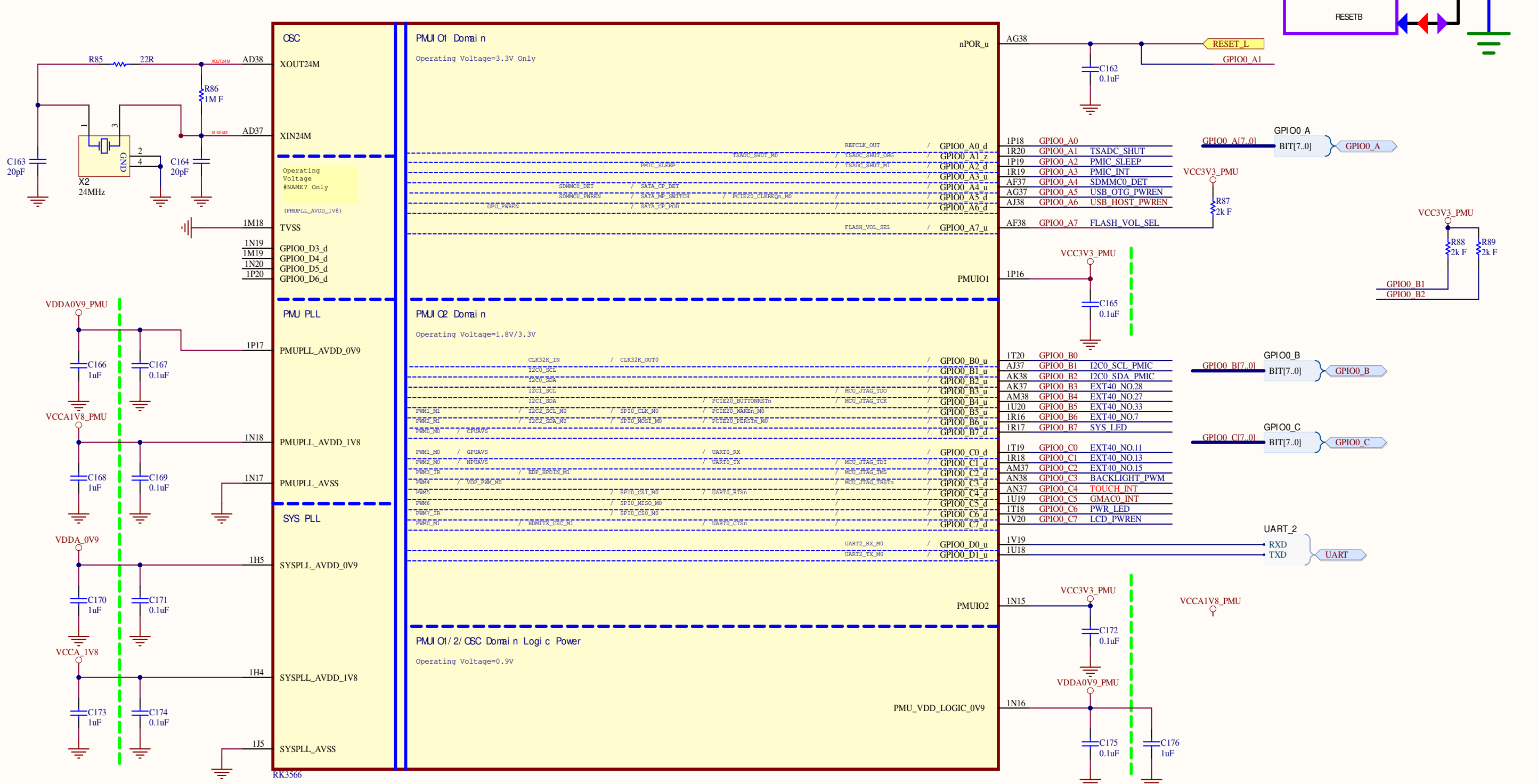
ODROID

RK3568_F (DDR PHY)

		DDR4				LPDDR4				DDR3				LPDDR3													
A DQ0	G2	DDR_DQ0_A	/	DDR4_DQ0_A	/	LPDDR4_DQ0_A	/	DDR3_DQ0	/	LPDDR3_DQ15		DDR4_A0	/	LPDDR4_CLKP_B	/	DDR3_A9	/	---	/	AC0	A7	B CLK P					
A DQ1	F2	DDR_DQ1_A	/	DDR4_DQ1_A	/	LPDDR4_DQ1_A	/	DDR3_DQ1	/	LPDDR3_DQ14		DDR4_A1	/	---	/	DDR3_A2	/	---	/	AC1	ID2	✗					
A DQ2	F1	DDR_DQ2_A	/	DDR4_DQ2_A	/	LPDDR4_DQ2_A	/	DDR3_DQ2	/	LPDDR3_DQ10		DDR4_A2	/	LPDDR4_A1_A	/	DDR3_A4	/	---	/	AC2	C1		A A1				
A DQ3	E1	DDR_DQ3_A	/	DDR4_DQ3_A	/	LPDDR4_DQ3_A	/	DDR3_DQ3	/	LPDDR3_DQ9		DDR4_A3	/	LPDDR4_CKE1_A	/	DDR3_A3	/	---	/	AC3	IC3		A CLKE1				
A DQ4	M2	DDR_DQ4_A	/	DDR4_DQ4_A	/	LPDDR4_DQ4_A	/	DDR3_DQ4	/	LPDDR3_DQ13																	
A DQ5	K1	DDR_DQ5_A	/	DDR4_DQ5_A	/	LPDDR4_DQ5_A	/	DDR3_DQ5	/	LPDDR3_DQ12		DDR4_A4	/	LPDDR4_A3_B	/	DDR3_BA1	/	LPDDR3_A3	/	AC4	1B6	B A3					
A DQ6	K2	DDR_DQ6_A	/	DDR4_DQ6_A	/	LPDDR4_DQ6_A	/	DDR3_DQ6	/	LPDDR3_DQ8		DDR4_A5	/	LPDDR4_A5_B	/	DDR3_A11	/	LPDDR3_A2	/	AC5	B8	B A5					
A DQ7	1E1	DDR_DQ7_A	/	DDR4_DQ7_A	/	LPDDR4_DQ7_A	/	DDR3_DQ7	/	LPDDR3_DQ11		DDR4_A6	/	LPDDR4_A1_B	/	DDR3_A13	/	---	/	AC6	B9	B A1					
												DDR4_A7	/	LPDDR4_ODT0_CA_B	/	DDR3_A8	/	---	/	AC7	A10	B ODT0 CA					
A DM0	1E2	DDR_DM0_A	/	DDR4_DM0_A	/	LPDDR4_DM0_A	/	DDR3_DM0	/	LPDDR3_DM1																	
A DQS0_P	H2	DDR_DQS0P_A	/	DDR4_DQS1P_A	/	LPDDR4_DQS0P_A	/	DDR3_DQS0P	/	LPDDR3_DQS1P		DDR4_A8	/	LPDDR4_ODT0_CA_A	/	DDR3_A6	/	LPDDR3_A9	/	AC8	E2	A ODT0 CA					
A DQS0_N	H1	DDR_DQS0N_A	/	DDR4_DQS1N_A	/	LPDDR4_DQS0N_A	/	DDR3_DQS0N	/	LPDDR3_DQS1N		DDR4_A9	/	LPDDR4_CLKN_B	/	DDR3_A5	/	---	/	AC9	B7	B CLK N					
												DDR4_A10	/	LPDDR4_CKE0_B	/	DDR3_A10	/	---	/	AC10	1A3	B CLKE0					
												DDR4_A11	/	LPDDR4_A0_A	/	DDR3_A7	/	LPDDR3_A8	/	AC11	C2	A A0					
A DQ8	P2	DDR_DQ8_A	/	DDR4_DQ8_A	/	LPDDR4_DQ8_A	/	DDR3_DQ8	/	LPDDR3_DQ25																	
A DQ9	R1	DDR_DQ9_A	/	DDR4_DQ9_A	/	LPDDR4_DQ9_A	/	DDR3_DQ9	/	LPDDR3_DQ24		DDR4_A12	/	LPDDR4_A3_A	/	DDR3_BA2	/	---	/	AC12	1B3	A A3					
A DQ10	R2	DDR_DQ10_A	/	DDR4_DQ10_A	/	LPDDR4_DQ10_A	/	DDR3_DQ10	/	LPDDR3_DQ28		DDR4_A13	/	LPDDR4_A0_B	/	DDR3_A14	/	LPDDR3_A0	/	AC13	A9	B A0					
A DQ11	T2	DDR_DQ11_A	/	DDR4_DQ11_A	/	LPDDR4_DQ11_A	/	DDR3_DQ11	/	LPDDR3_DQ29		DDR4_A14_Weh	/	LPDDR4_A4_A	/	DDR3_A15	/	LPDDR3_A5	/	AC14	1B1	A A4					
A DQ12	M1	DDR_DQ12_A	/	DDR4_DQ12_A	/	LPDDR4_DQ12_A	/	DDR3_DQ12	/	LPDDR3_DQ26		DDR4_A15_Casn	/	LPDDR4_A2_A	/	DDR3_A0	/	---	/	AC15	1C1	A A2					
A DQ13	1F2	DDR_DQ13_A	/	DDR4_DQ13_A	/	LPDDR4_DQ13_A	/	DDR3_DQ13	/	LPDDR3_DQ31																	
A DQ14	1F1	DDR_DQ14_A	/	DDR4_DQ14_A	/	LPDDR4_DQ14_A	/	DDR3_DQ14	/	LPDDR3_DQ30		DDR4_A16_Rasn	/	LPDDR4_A5_A	/	DDR3_RAsn	/	LPDDR3_A7	/	AC16	1A1	A A5					
A DQ15	1G2	DDR_DQ15_A	/	DDR4_DQ15_A	/	LPDDR4_DQ15_A	/	DDR3_DQ15	/	LPDDR3_DQ27		DDR4_A17n	/	LPDDR4_CKE1_B	/	DDR3_Casn	/	---	/	AC17	1A2	B CLKE1					
												DDR4_A18	/	LPDDR4_A2_B	/	DDR3_A1	/	---	/	AC18	1B7	B A2					
												DDR4_A19	/	LPDDR4_A4_B	/	DDR3_A12	/	LPDDR3_A4	/	AC19	1A6	B A4					
A DM1	1G1	DDR_DM1_A	/	DDR4_DM1_A	/	LPDDR4_DM1_A	/	DDR3_DM1	/	LPDDR3_DM3																	
A DQS1_P	N1	DDR_DQS1P_A	/	DDR4_DQS1P_A	/	LPDDR4_DQS1P_A	/	DDR3_DQS1P	/	LPDDR3_DQS3P		DDR4_B0	/	LPDDR4_ODT1_CA_A	/	DDR3_Weh	/	---	/	AC20	1A4	✗					
A DQS1_N	N2	DDR_DQS1N_A	/	DDR4_DQS1N_A	/	LPDDR4_DQS1N_A	/	DDR3_DQS1N	/	LPDDR3_DQS3N		DDR4_B01	/	LPDDR4_ODT1_CA_A	/	DDR3_BA0	/	---	/	AC21	1C2		A CLKE0				
												DDR4_CKE	/	LPDDR4_CKE0_A	/	DDR3_CKE	/	LPDDR3_CKE	/	AC22	B4						
B DQ0	B12	DDR_DQ0_B	/	DDR4_DQ0_B	/	LPDDR4_DQ0_B	/	DDR3_DQ16	/	LPDDR3_DQ1		DDR4_CLKP	/	LPDDR4_CLKP_A	/	DDR3_CLKP	/	LPDDR3_CLKP	/	AC23	A5	A CLK P					
B DQ1	B10	DDR_DQ1_B	/	DDR4_DQ1_B	/	LPDDR4_DQ1_B	/	DDR3_DQ17	/	LPDDR3_DQ5		DDR4_CLKN	/	LPDDR4_CLKN_A	/	DDR3_CLKN	/	LPDDR3_CLKN	/	AC24	B5	A CLK N					
B DQ2	1A8	DDR_DQ2_B	/	DDR4_DQ2_B	/	LPDDR4_DQ2_B	/	DDR3_DQ18	/	LPDDR3_DQ6																	
B DQ3	1A7	DDR_DQ3_B	/	DDR4_DQ3_B	/	LPDDR4_DQ3_B	/	DDR3_DQ19	/	LPDDR3_DQ6		DDR4_CS0n	/	LPDDR4_CS0n_A	/	DDR3_ODT1	/	LPDDR3_ODT0	/	AC25	B3	A CS0					
B DQ4	B13	DDR_DQ4_B	/	DDR4_DQ4_B	/	LPDDR4_DQ4_B	/	DDR3_DQ20	/	LPDDR3_DQ7		DDR4_CS1n	/	LPDDR4_CS1n_A	/	DDR3_CS1n	/	LPDDR3_ODT1	/	AC26	A3	A CS1					
B DQ5	1A10	DDR_DQ5_B	/	DDR4_DQ5_B	/	LPDDR4_DQ5_B	/	DDR3_DQ21	/	LPDDR3_DQ3		DDR4_ODT0	/	LPDDR4_CS1n_B	/	DDR3_ODT0	/	LPDDR3_CS1n	/	AC27	1A5	B CS1					
B DQ6	1B9	DDR_DQ6_B	/	DDR4_DQ6_B	/	LPDDR4_DQ6_B	/	DDR3_DQ22	/	LPDDR3_DQ7		DDR4_ODT1	/	LPDDR4_CS0n_B	/	DDR3_CS0n	/	LPDDR3_CS0n	/	AC28	1B5	B CS0					
B DQ7	1A9	DDR_DQ7_B	/	DDR4_DQ7_B	/	LPDDR4_DQ7_B	/	DDR3_DQ23	/	LPDDR3_DQ0																	
B DM0	1B8	DDR_DM0_B	/	DDR4_DM0_B	/	LPDDR4_DM0_B	/	DDR3_DM2	/	LPDDR3_DM0		DDR4_RESETh	/	LPDDR4_RESETh	/	DDR3_RESETh	/	---	/	AC29	1C7	A RESET					
B DQS0_P	A13	DDR_DQS0P_B	/	DDR4_DQS0P_B	/	LPDDR4_DQS0P_B	/	DDR3_DQS2P	/	LPDDR3_DQS0P		Note: Sequences can not be swap															
B DQS0_N	A12	DDR_DQS0N_B	/	DDR4_DQS0N_B	/	LPDDR4_DQS0N_B	/	DDR3_DQS2N	/	LPDDR3_DQS0N												DDR_RZQ	1F3	DDR RZQ	R1		
B DQ8	B19	DDR_DQ8_B	/	DDR4_DQ8_B	/	LPDDR4_DQ8_B	/	DDR3_DQ24	/	LPDDR3_DQ18_D2																	
B DQ9	A19	DDR_DQ9_B	/	DDR4_DQ9_B	/	LPDDR4_DQ9_B	/	DDR3_DQ25	/	LPDDR3_DQ19_D3																	
B DQ10	A20	DDR_DQ10_B	/	DDR4_DQ10_B	/	LPDDR4_DQ10_B	/	DDR3_DQ26	/	LPDDR3_DQ22_D6																	
B DQ11	B20	DDR_DQ11_B	/	DDR4_DQ11_B	/	LPDDR4_DQ11_B	/	DDR3_DQ27	/	LPDDR3_DQ23_D7																	
B DQ12	A15	DDR_DQ12_B	/	DDR4_DQ12_B	/	LPDDR4_DQ12_B	/	DDR3_DQ28	/	LPDDR3_DQ10_D4												DDR_VREFOUT	1H3	✗			
B DQ13	B15	DDR_DQ13_B	/	DDR4_DQ13_B	/	LPDDR4_DQ13_B	/	DDR3_DQ29	/	LPDDR3_DQ17_D5																	
B DQ14	1C10	DDR_DQ14_B	/	DDR4_DQ14_B	/	LPDDR4_DQ14_B	/	DDR3_DQ30	/	LPDDR3_DQ20_D1																	
B DQ15	B16	DDR_DQ15_B	/	DDR4_DQ15_B	/	LPDDR4_DQ15_B	/	DDR3_DQ31	/	LPDDR3_DQ21_D5																	
B DM1	1A11	DDR_DM1_B	/	DDR4_DM1_B	/	LPDDR4_DM1_B	/	DDR3_DM3	/	LPDDR3_DM2																	
B DQS1_P	A17	DDR_DQS1P_B	/	DDR4_DQS1P_B	/	LPDDR4_DQS1P_B	/	DDR3_DQS3P	/	LPDDR3_DQS2P												DDR_VDDQ_1	1D5				
B DQS1_N	B17	DDR_DQS1N_B	/	DDR4_DQS1N_B	/	LPDDR4_DQS1N_B	/	DDR3_DQS3N	/	LPDDR3_DQS2N												DDR_VDDQ_2	1D6				
																					DDR_VDDQ_3	1D7					
																					DDR_VDDQ_4	1D8					
																					DDR_VDDQ_5	1D9					
																					DDR_VDDQ_6	1E4					
																					DDR_VDDQ_7	1F4					
																					DDR_VDDQ_8	1G4					
																					DDR_VDDQL_1	1E6					
																					DDR_VDDQL_2	1E7					
																					DDR_VDDQL_3	1E9					
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																					DDR_VDDQL_5	1G5					
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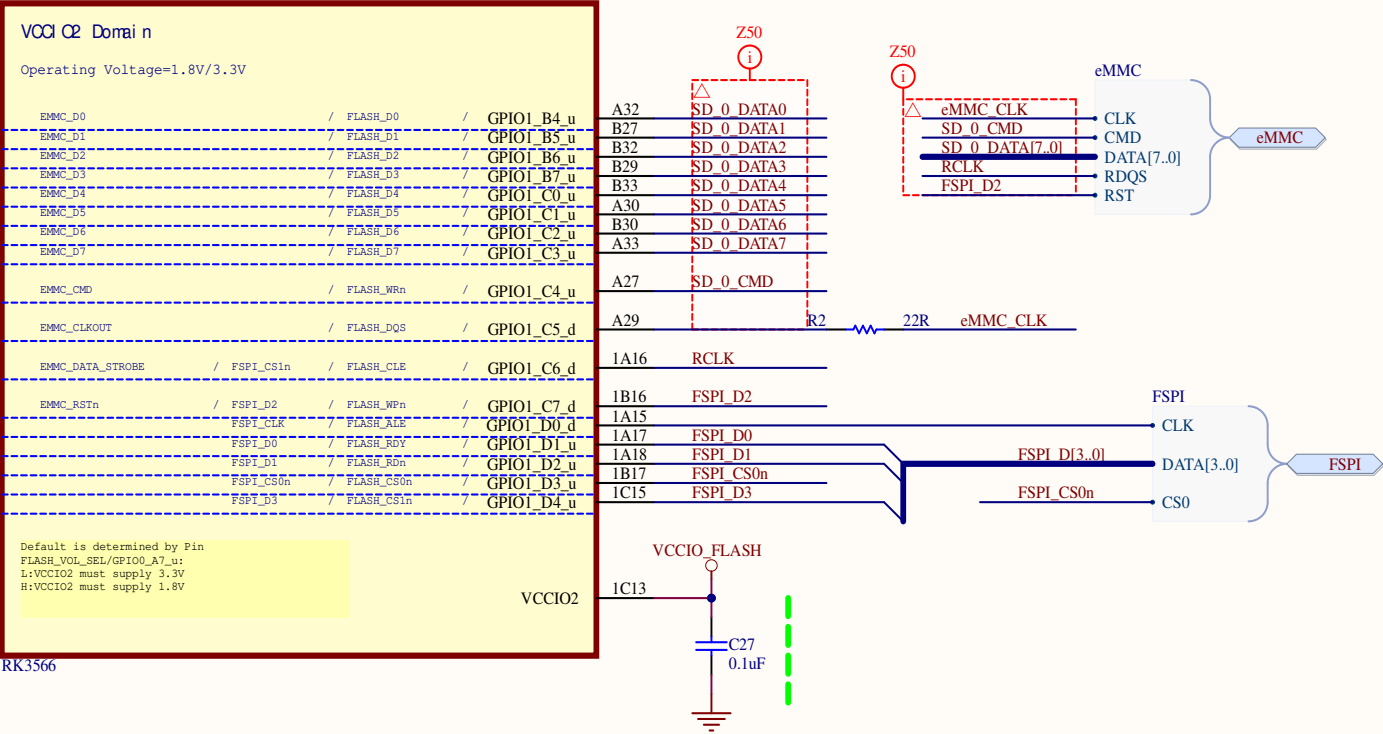
RK3568_G (OSC/ PLL/ PMUI O1/ 2)



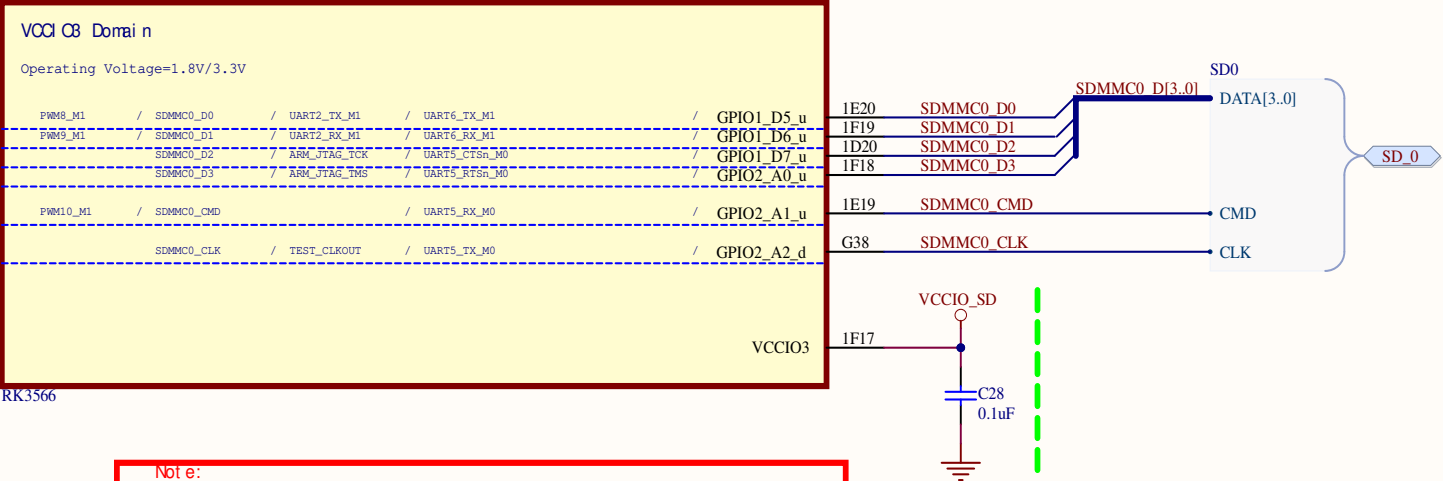
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3566_I (VCCI O2 Domai n)



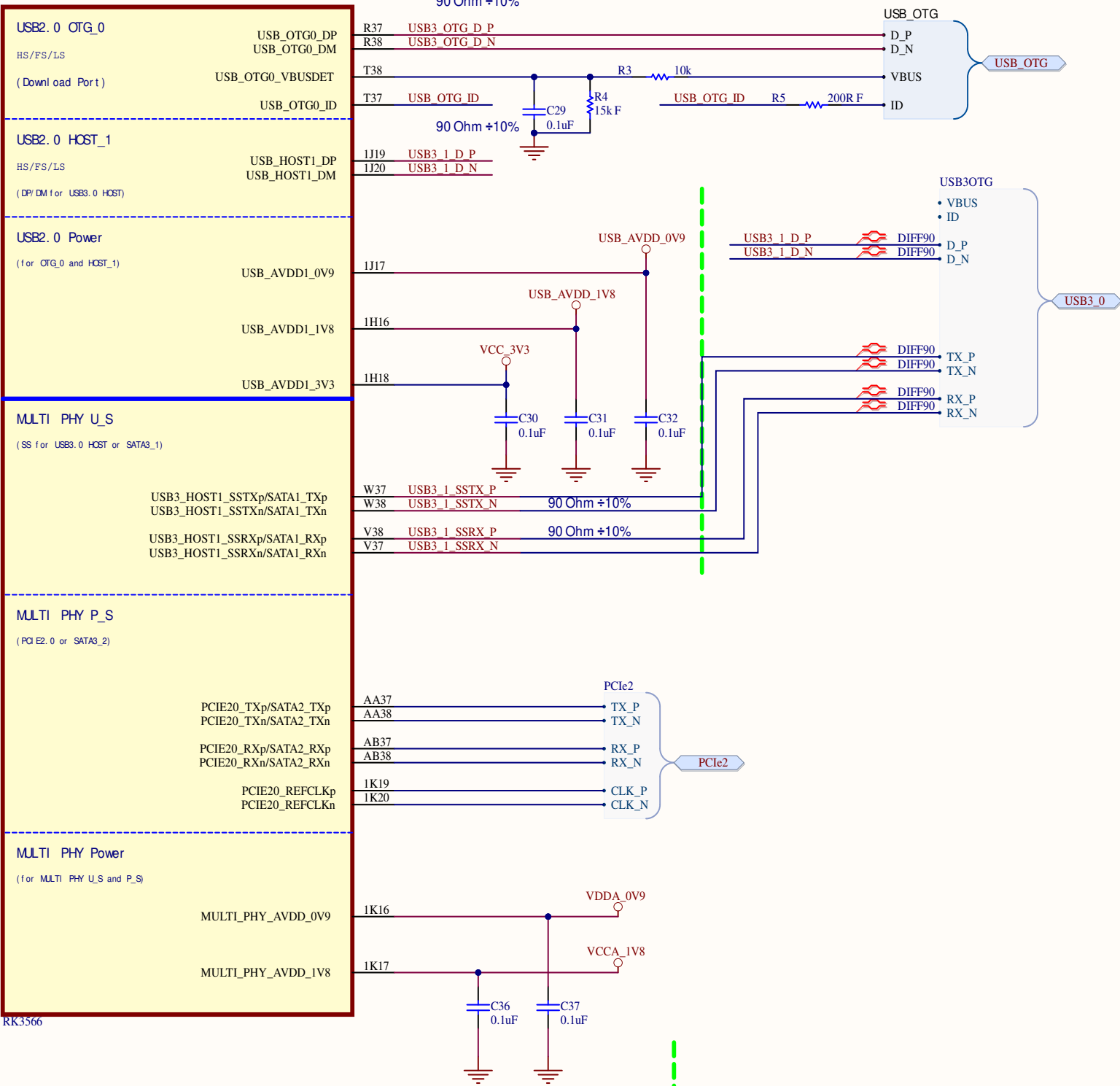
RK3566_J (VCCI O3 Domai n)



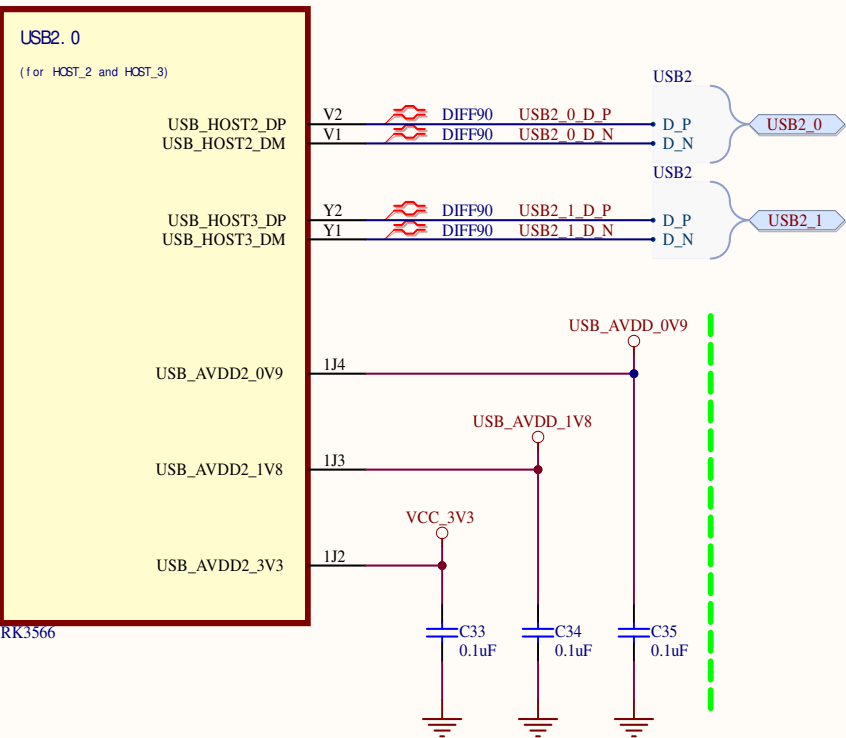
Not e:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3566_U(USB3. 0/ SATA/ QSGM I / PCI e2. 0 x1)



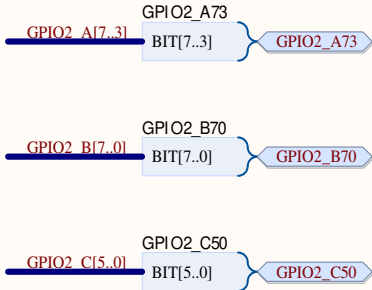
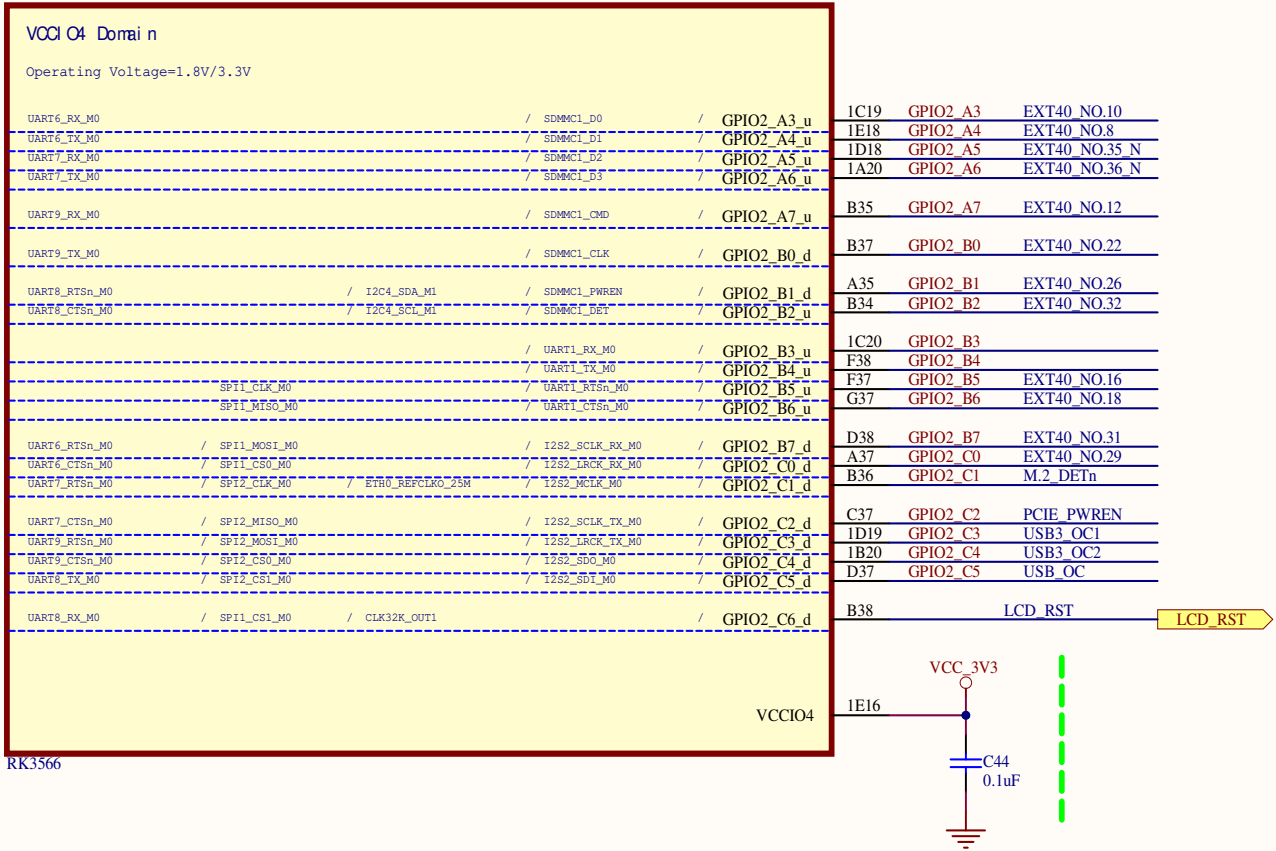
RK3566_V(USB2. 0 HOST)



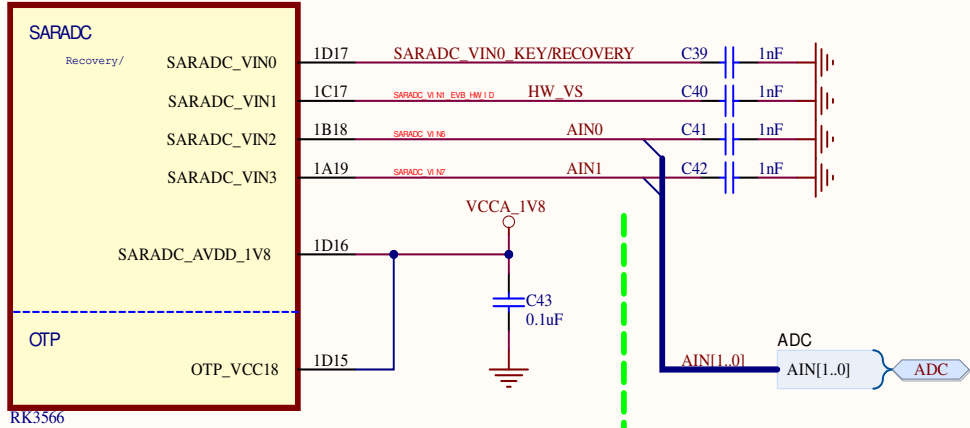
Not e:

Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

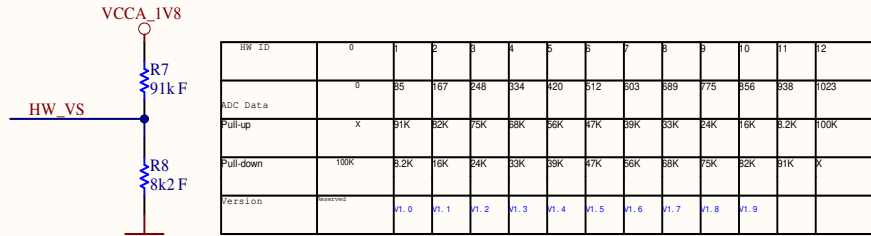
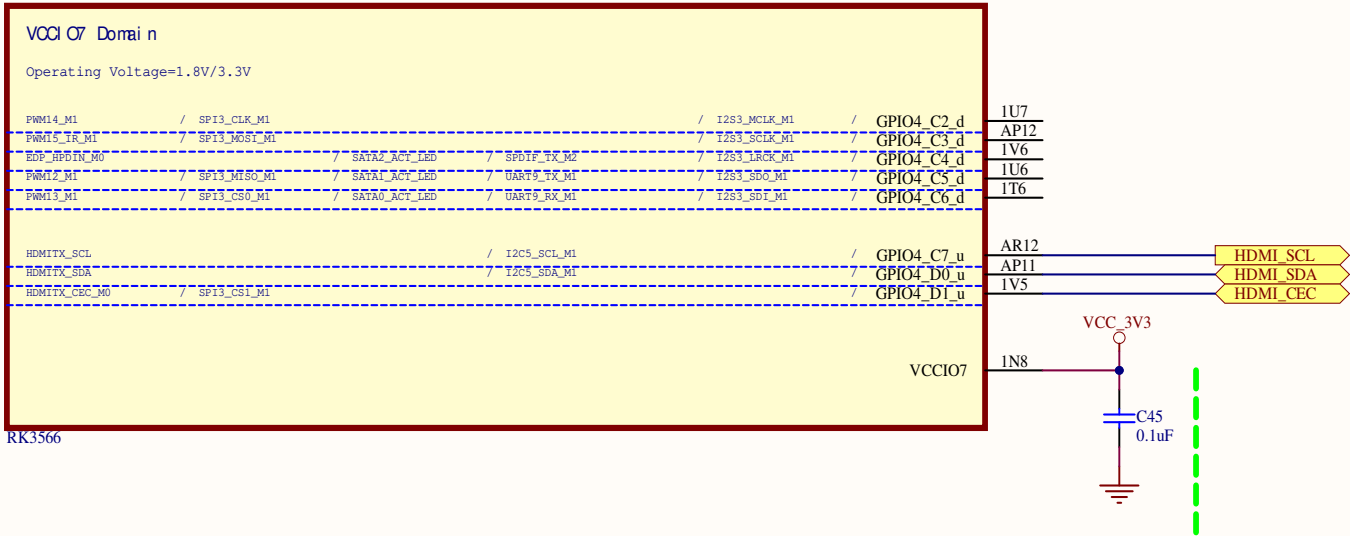
RK3566_K(VCCI O4 Domai n)



RK3566_Q(SARADC/ OTP)



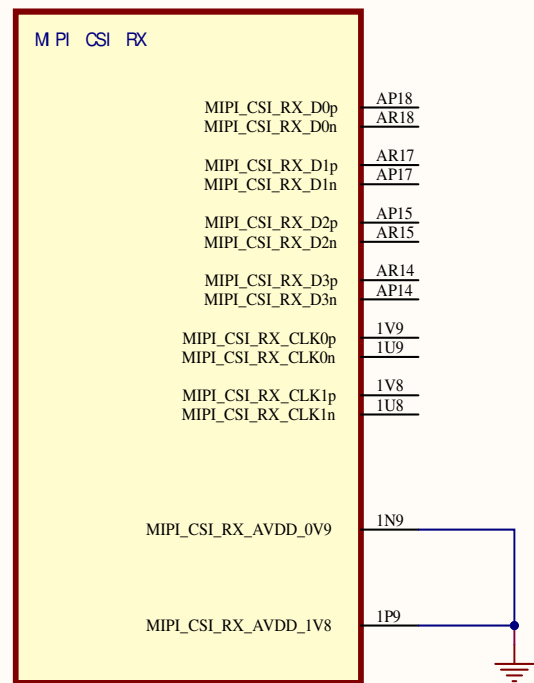
RK3566_N(VCCI O7 Domai n)



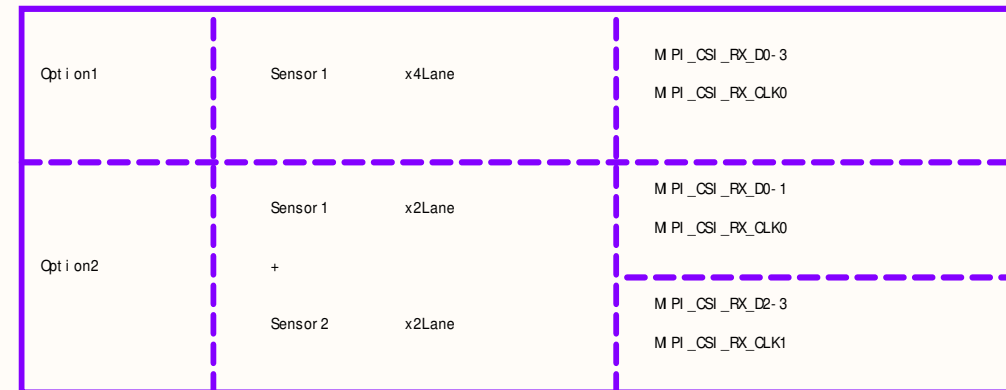
Not e:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3566_P(M PI _CSI _RX)

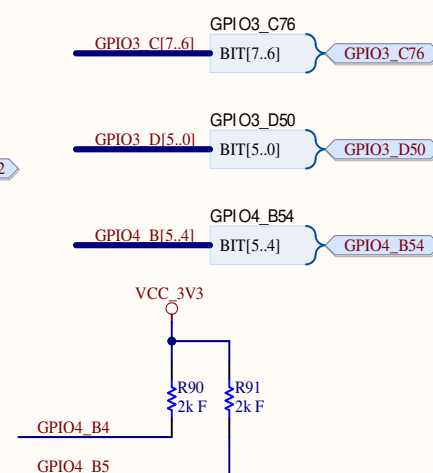


RK3566



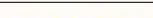
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QTF_D1	D1	--	--	--
QTF_D2	D2	--	--	--
QTF_D3	D3	--	--	--
QTF_D4	D4	D0	--	--
QTF_D5	D5	D1	--	--
QTF_D6	D6	D2	D0	--
QTF_D7	D7	D3	D1	--
QTF_D8	D8	D4	D2	D0
QTF_D9	D9	D5	D3	D1
QTF_D10	D10	D6	D4	D2
QTF_D11	D11	D7	D5	D3
QTF_D12	D12	D8	D6	D4
QTF_D13	D13	D9	D7	D5
QTF_D14	D14	D10	D8	D6
QTF_D15	D15	D11	D9	D7

Support	BT601 YCbCr	422	8bit	input
Support	BT656 YCbCr	422	8bit	input
Support	RAW 8/10/12bit			input
Support	BT1120 YCbCr	422	8/10/12/16bit	input, single/dual-edge sampling
Support	2/4 mixed BT656/BT1120	YCbCr	422	8bit input

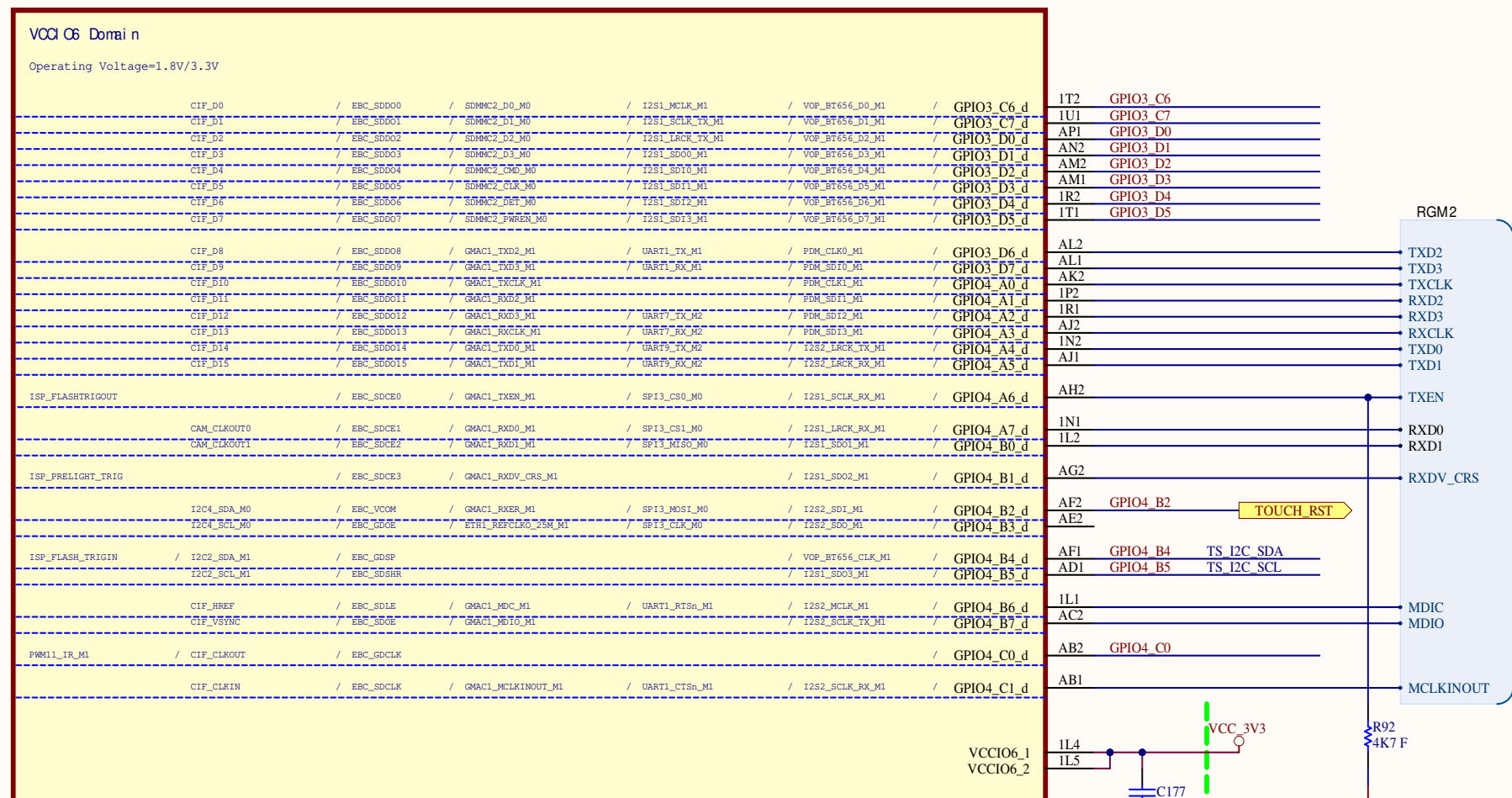


☐ Not e:

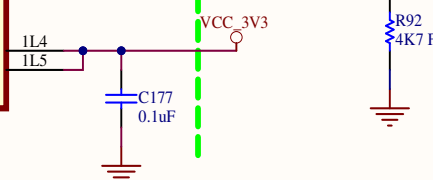
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Title RK3566_VI Interface			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		
Size: A3	Number: 9	Revision: 0.1			
Date: 2023-10-16	Time: 오후 3:23:20	Sheet 9 of 41			
File: RK3566_VIINTERFACE.SchDoc			Designed by: ruppi.kim@hardkernel.com		

RK3566_M(VCCI O6 Domai n)



RK3566



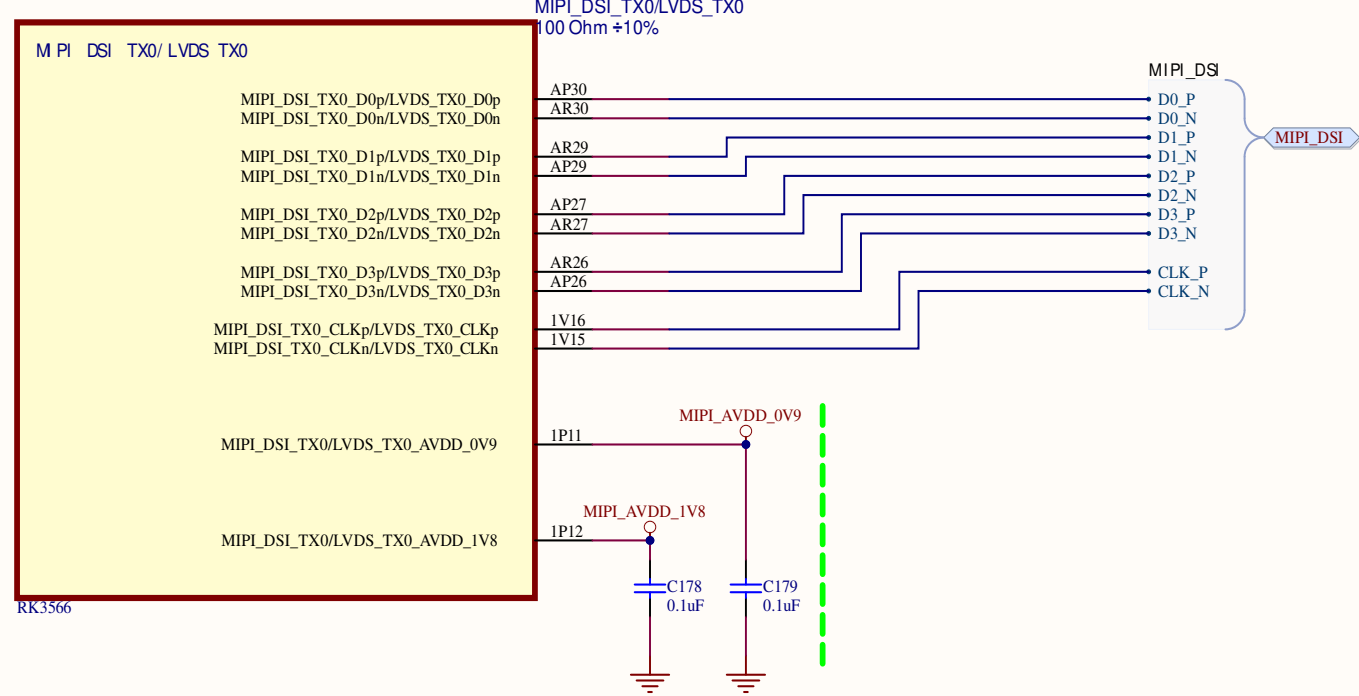
A

E

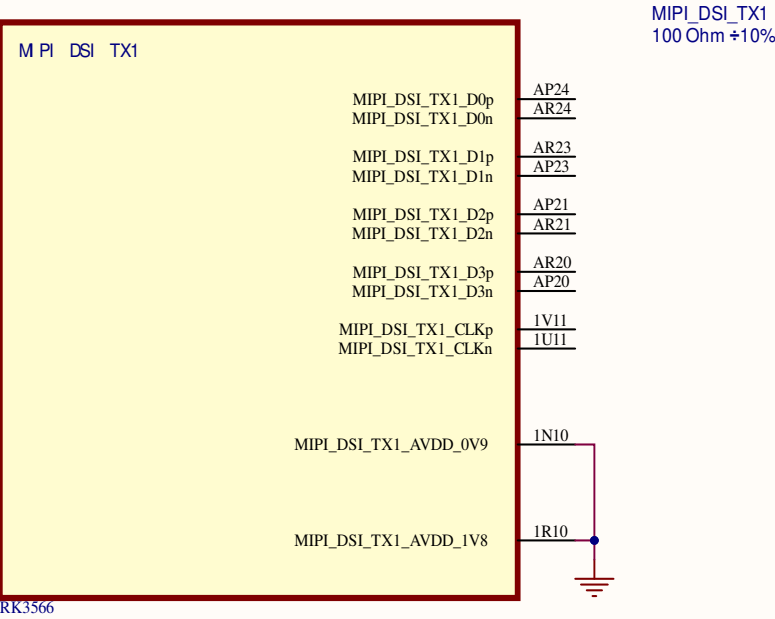
C

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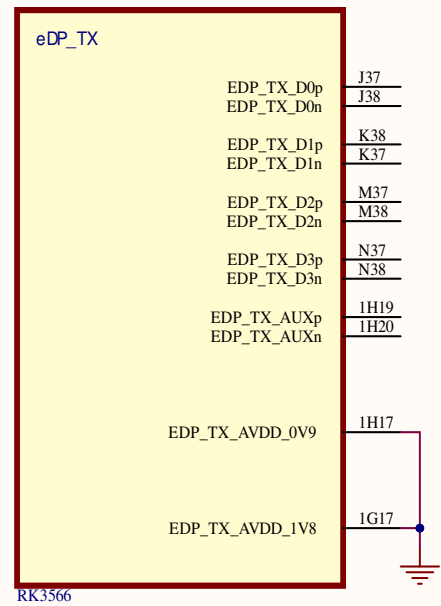
RK3566_R(M PI _DSI _TX0/ LVDS_TX0)



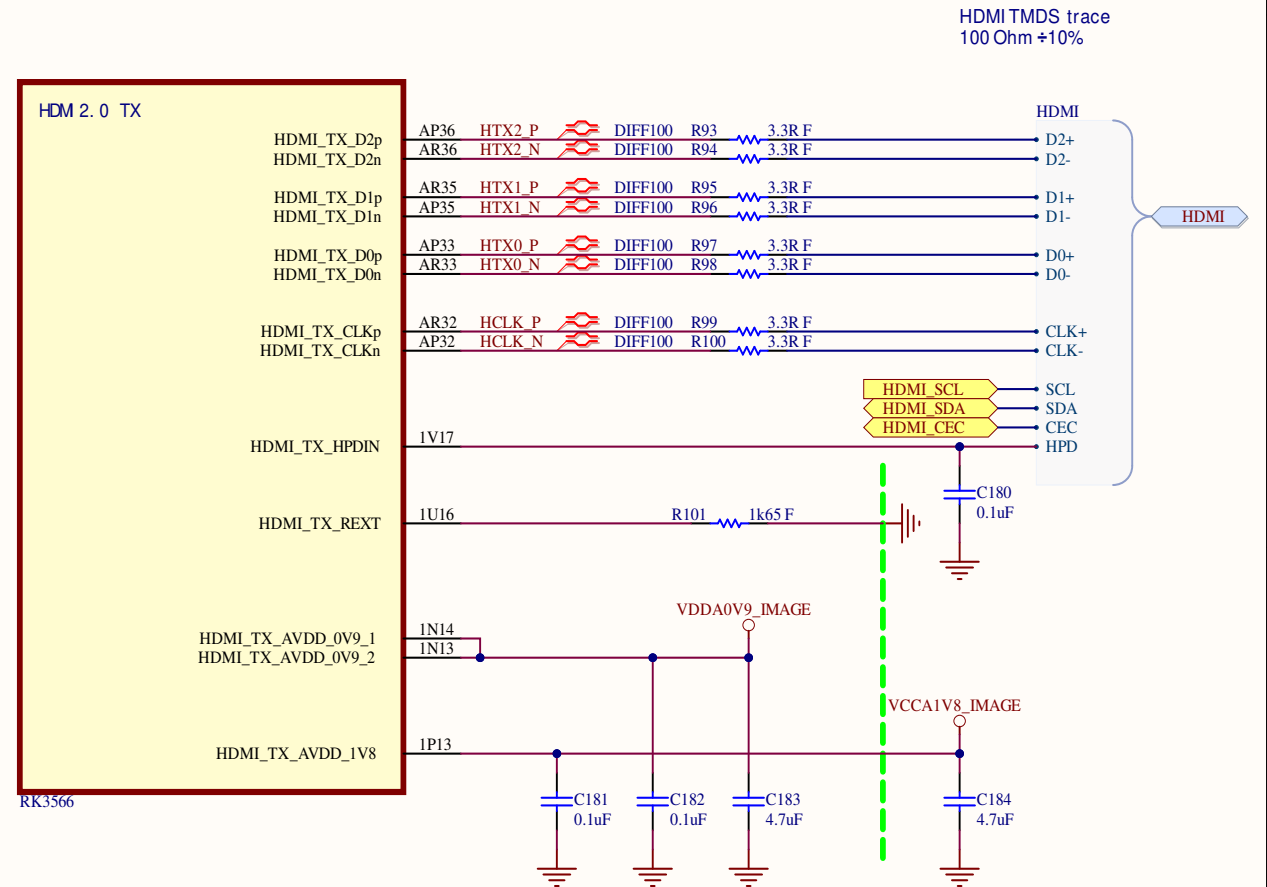
RK3566_S(M PI _DSI _TX1)



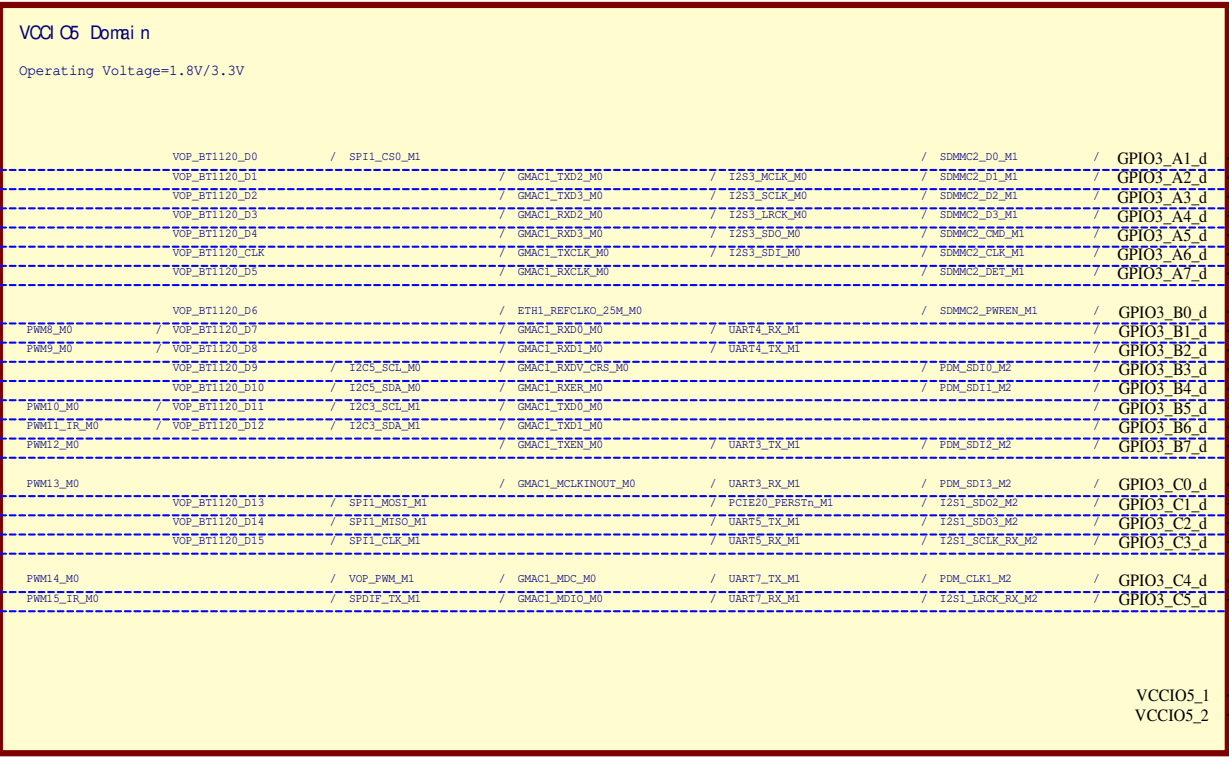
RK3566_T(eDP TX)



RK3566_Q(HDM 2. 0 TX)

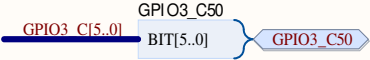
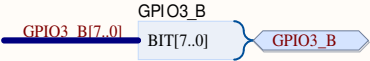
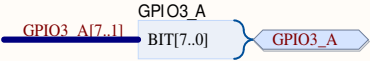
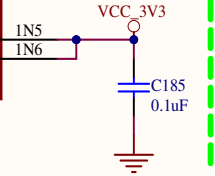


RK3566_L(VCCI O5 Domai n)



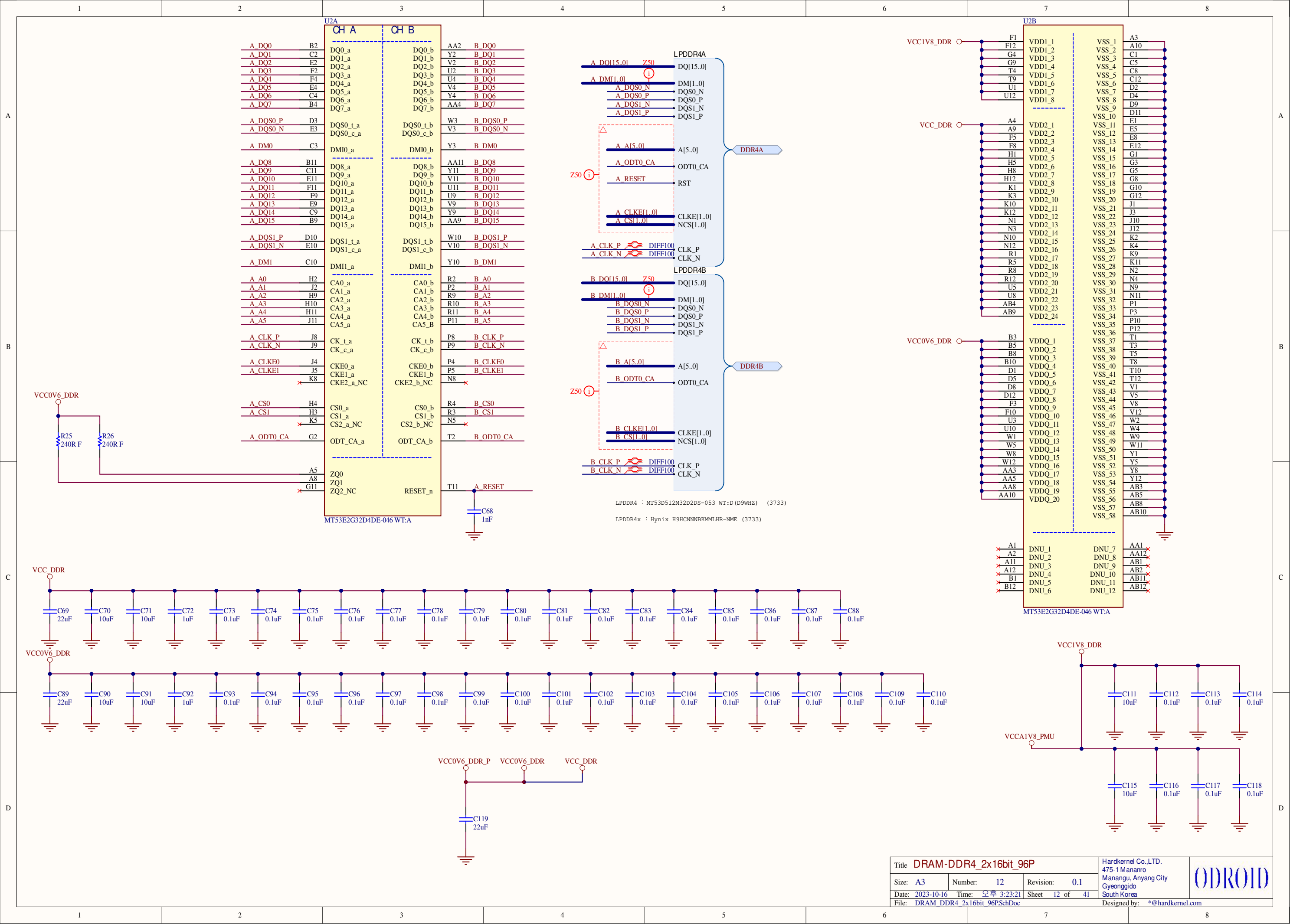
RK3566

IU5	GPIO3_A1	EXT40_NO.24
AR10	GPIO3_A2	GPIO3_A2
AP10	GPIO3_A3	GPIO3_A3_H
AR9	GPIO3_A4	GPIO3_A4_H
AP9	GPIO3_A5	PCIE3_CLKREQn
IU4	GPIO3_A6	PCIE3_PERSTn
IV3	GPIO3_A7	GPIO3_A6
AR7	GPIO3_B0	GPIO3_B0
AP7	GPIO3_B1	
AR6	GPIO3_B2	
AP6	GPIO3_B3	EXT14_NO.13
IU3	GPIO3_B4	EXT14_NO.14
IT4	GPIO3_B5	EXT40_NO.5
IV2	GPIO3_B6	EXT40_NO.3
AP5	GPIO3_B7	GMAC0_nRST
AR4	GPIO3_C0	GPIO3_C0
AP4	GPIO3_C1	EXT40_NO.19
AP3	GPIO3_C2	EXT40_NO.21
AR2	GPIO3_C3	EXT40_NO.23
IP3	GPIO3_C4	EXT14_NO.11
IP4	GPIO3_C5	EXT14_NO.12

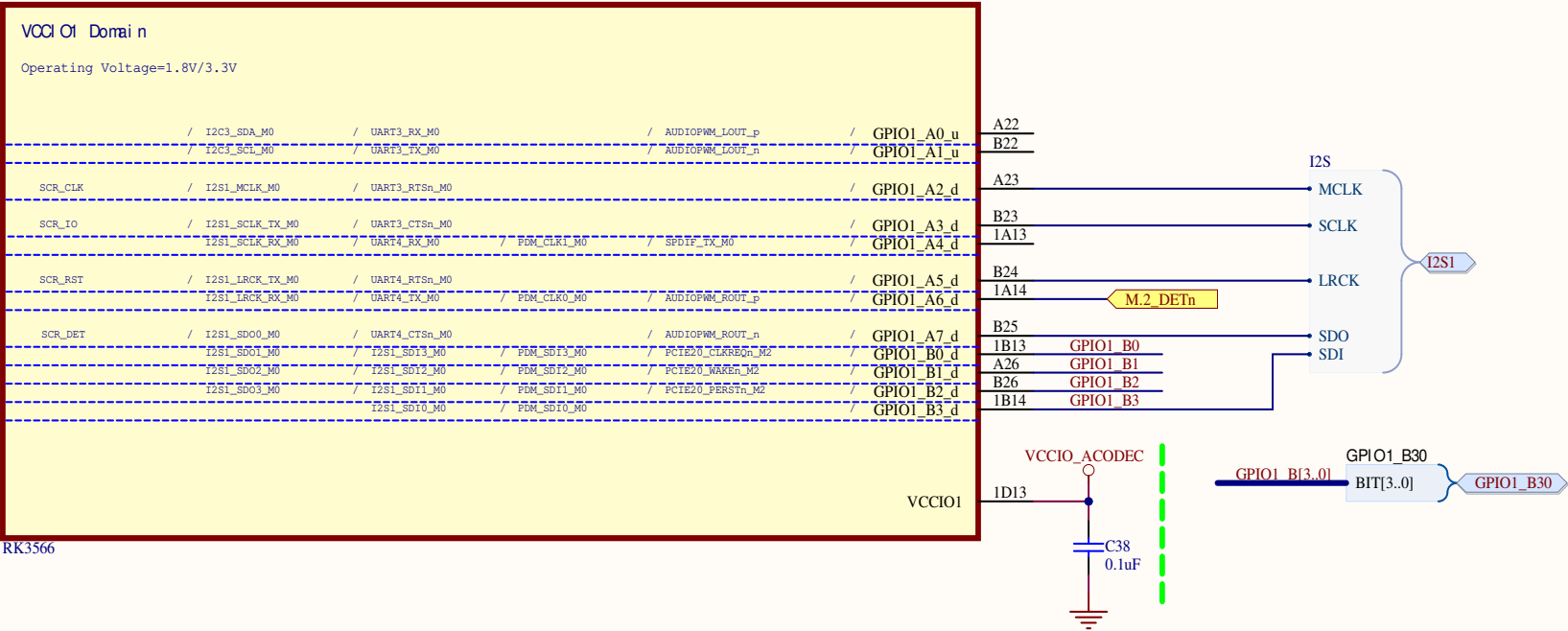


Not e:

Caps of between dashed green lines and U1000 should be placed under the U1000 package



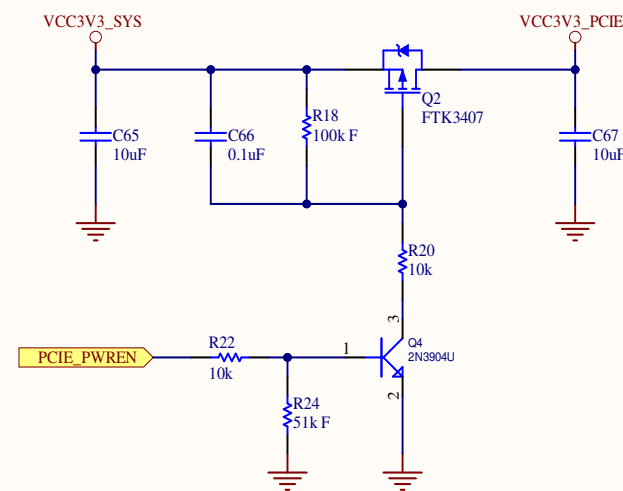
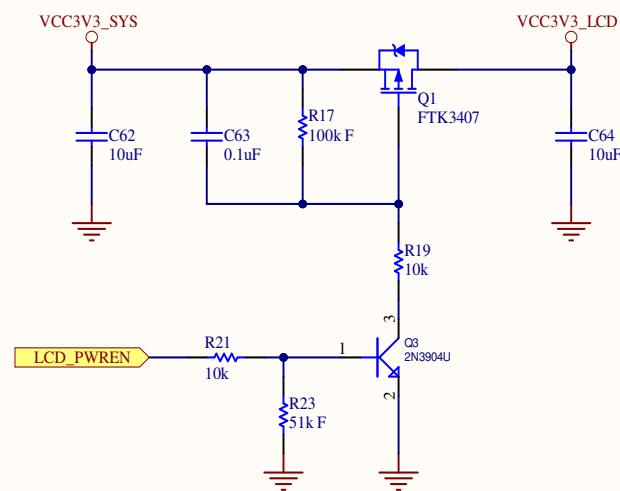
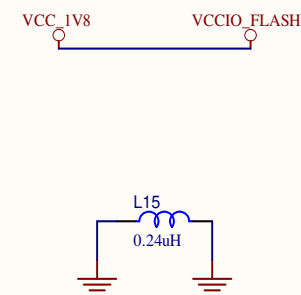
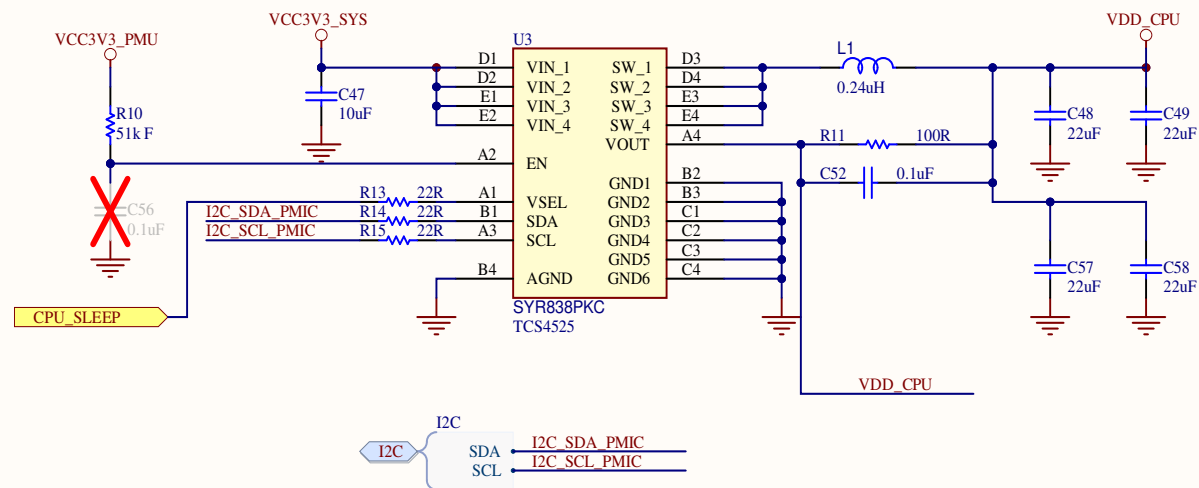
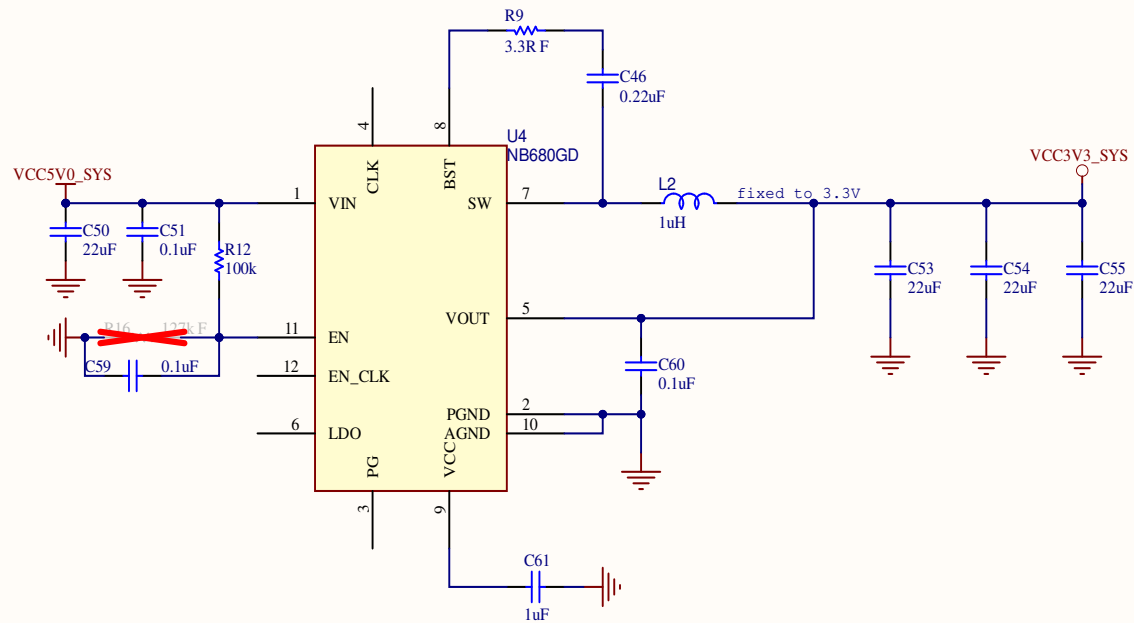
RK3566_H(VCCI O1 Domai n)



Not e:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

Title RK3566_Audio Interface				Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4		Number: 13				
Date: 2023-10-16		Time: 오후 3:23:21		Sheet 13 of 41		
File: RK3566_Audio Interface.SchDoc				Designed by: ruppi.kim@hardkernel.com		



A

A

B

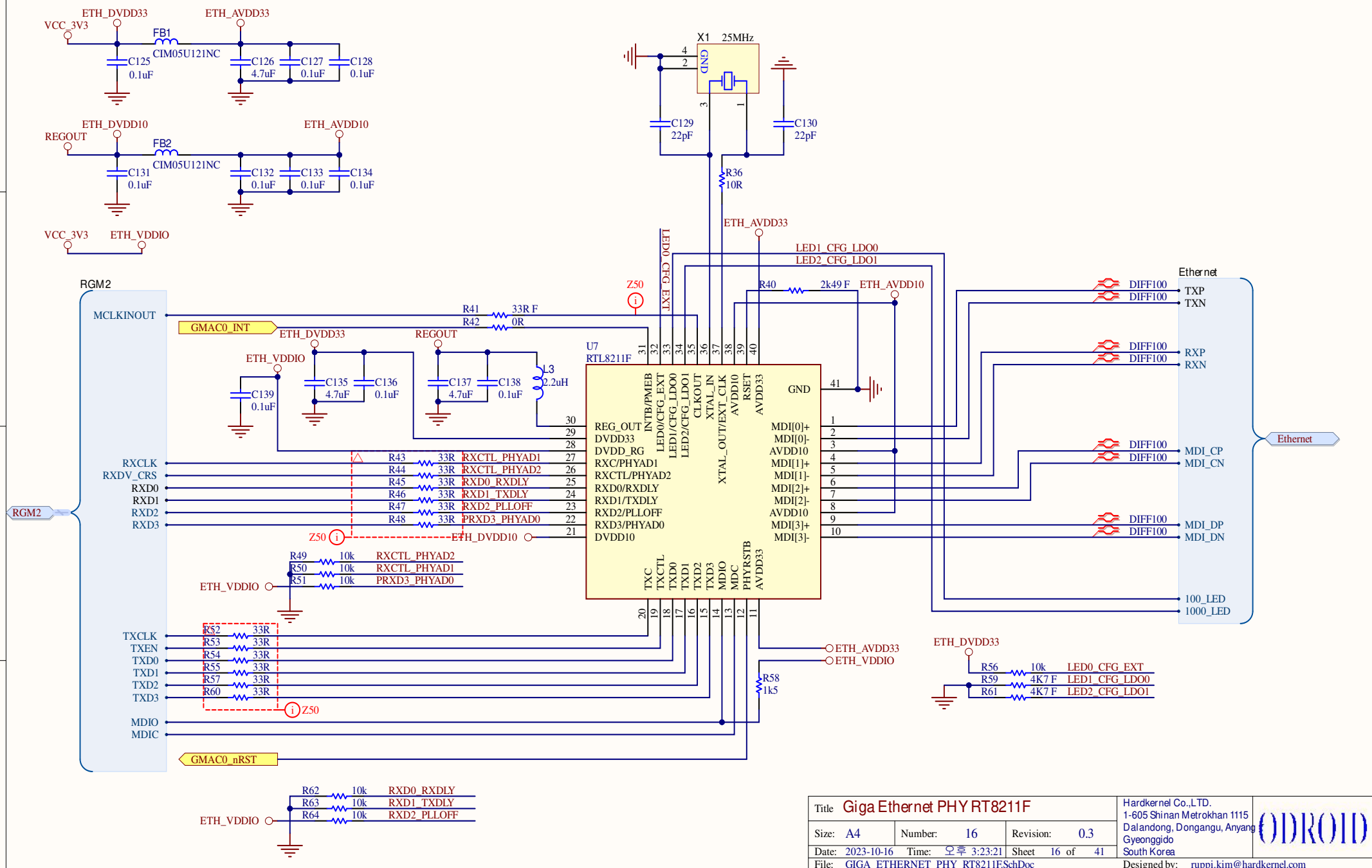
B

C

C

D

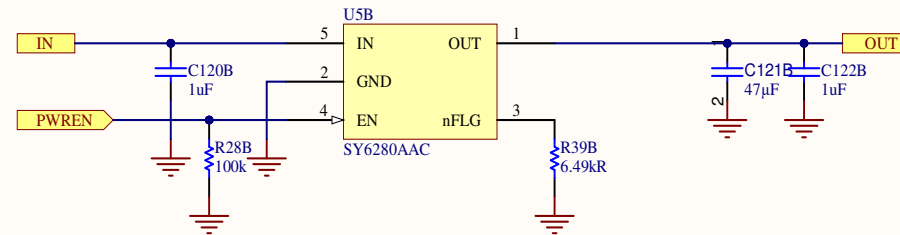
D

Title **Giga Ethernet PHY RT8211F**Size: **A4**Number: **16**Revision: **0.3**Date: **2023-10-16**Time: **오후 3:23:21**Sheet **16** of **41**File: **GIGA_ETHERNET_PHY_RT8211F.SchDoc**

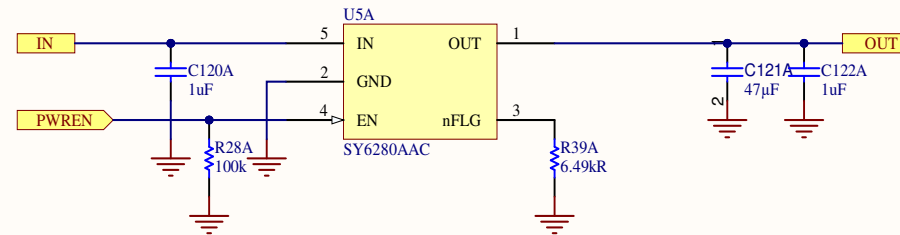
Hardkernel Co.,LTD.
1-605 Shinan Metrokhan 1115
Dalandong, Dongang, Anyang
Gyeonggi-do
South Korea

Designed by: **ruppi.kim@hardkernel.com**

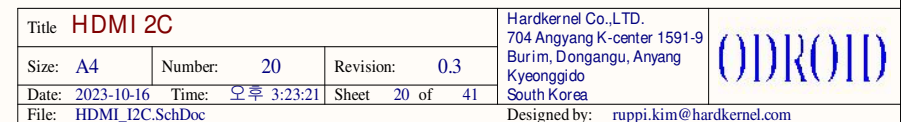
ODROID

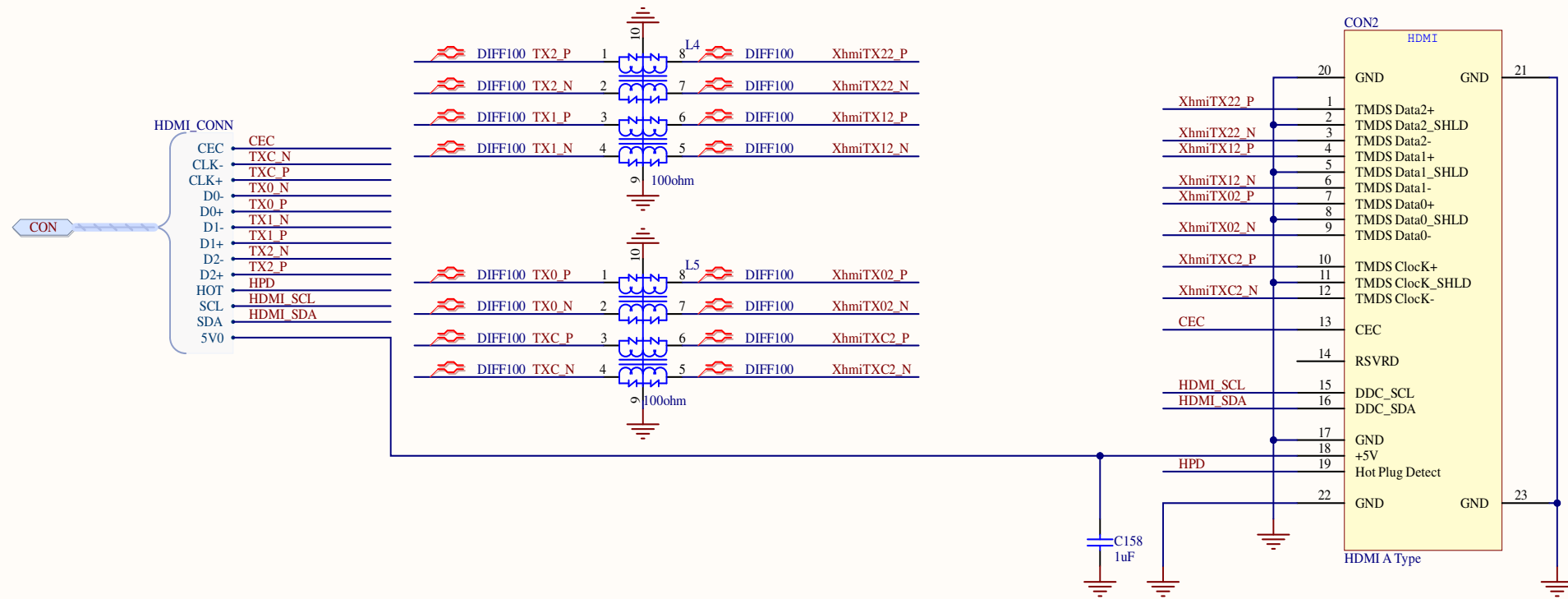


Title USB HOST Power Switch			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		
Size: A4	Number: 18	Revision: 0.1			
Date: 2023-10-16	Time: 오후 3:23:21	Sheet 18 of 41			
File: FC6261B.SchDoc			Designed by: ruppi.kim@hardkernel.com		



Title USB HOST Power Switch			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 18	Revision: 0.1			
Date: 2023-10-16	Time: 오후 3:23:21	Sheet 18 of 41			
File: FC6261B.SchDoc			Designed by: ruppi.kim@hardkernel.com		



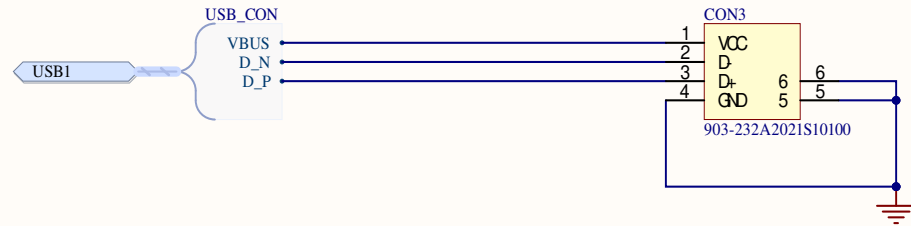
Title **HDMI Type A Connector**Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea**ODROID**Size: **A4**Number: **21**Revision: **0.1**

Date: 2023-10-16

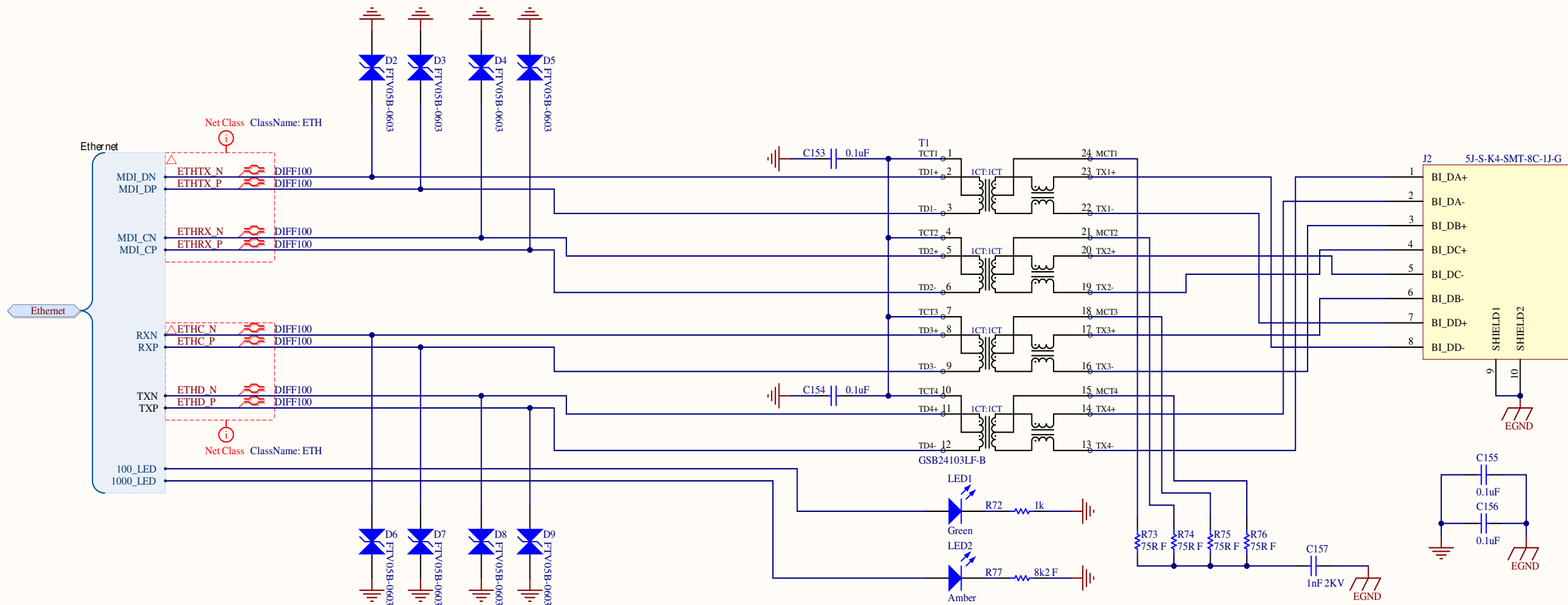
Time: 오후 3:23:22

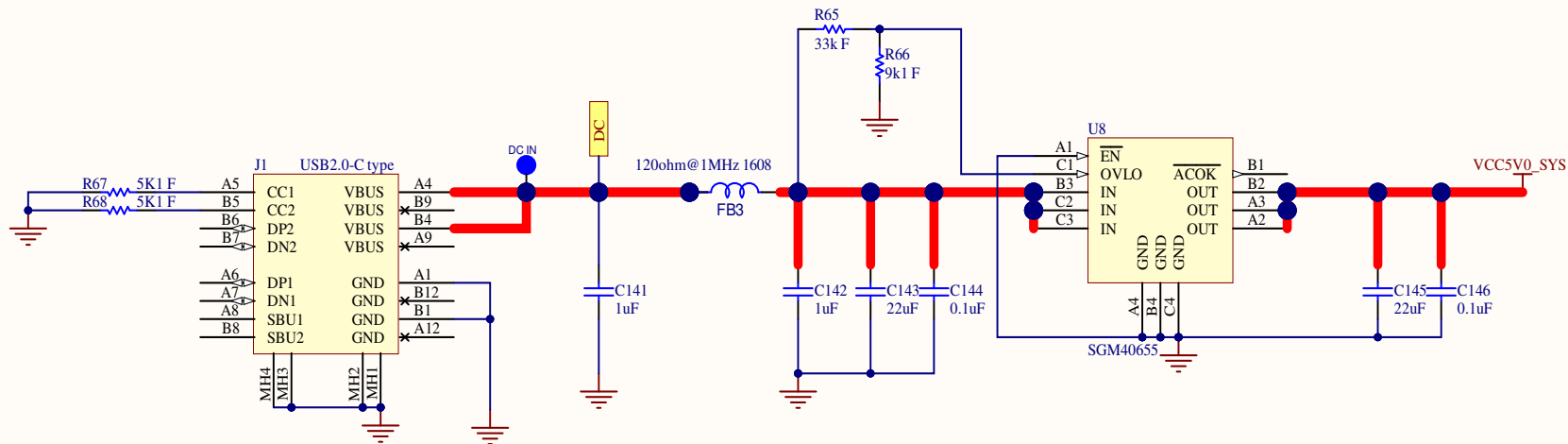
Sheet 21 of 41

File: **CON_HDMI.SchDoc**Designed by: ruppi.kim@hardkernel.com

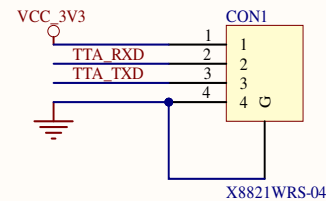
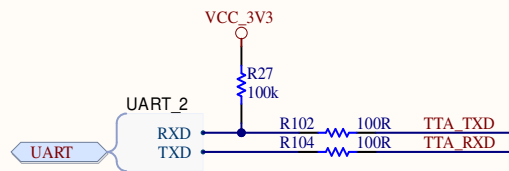


Title USB 2.0 Type A Connector			Hardkernel Co.,LTD. 1-605 Shinan Metrokhan 1115 Dalandong, Dongangu, Anyang Gyeonggido South Korea		ODROID
Size: A4	Number: 23	Revision: 0.3			
Date: 2023-10-16	Time: 오후 3:23:22	Sheet 23 of 41			
File: CON_USB_RA.SchDoc			Designed by: ruppi.kim@hardkernel.com		

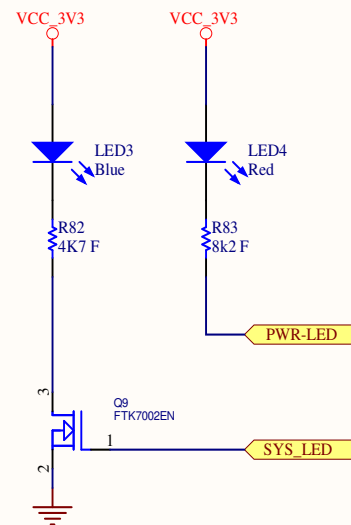




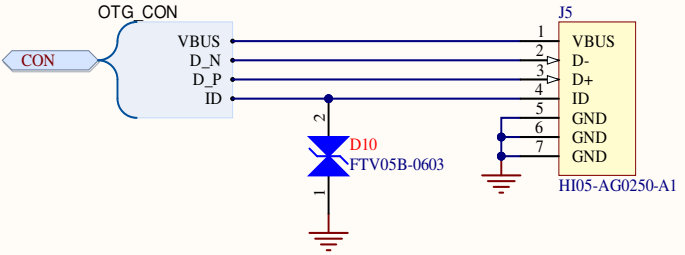
Title DC Jack			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 25	Revision: 0.1			
Date: 2023-10-16	Time: 오후 3:23:22	Sheet 25 of 41			
File: CON_DCJACK.SchDoc			Designed by: ruppi kim@hardkernel.com		



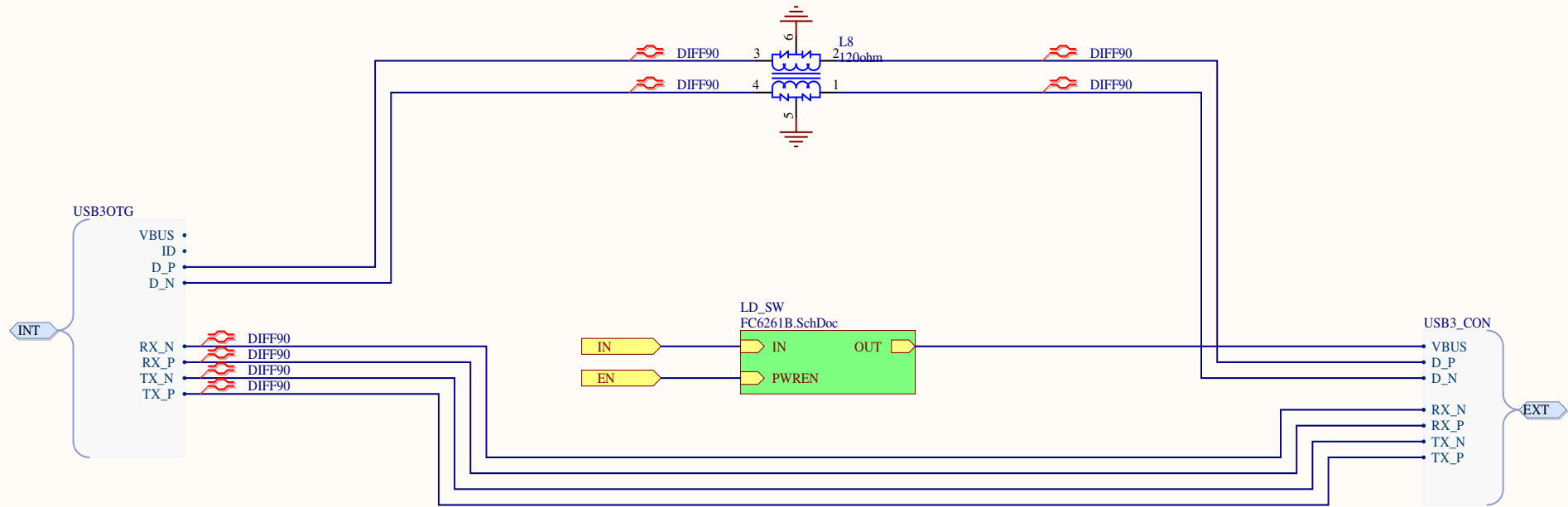
Title UART Connector			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		
Size: A4	Number: 27	Revision: 0.1			
Date: 2023-10-16	Time: 오후 3:23:22	Sheet 27 of 41			
File: CON_UART.SchDoc			Designed by: ruppi.kim@hardkernel.com		

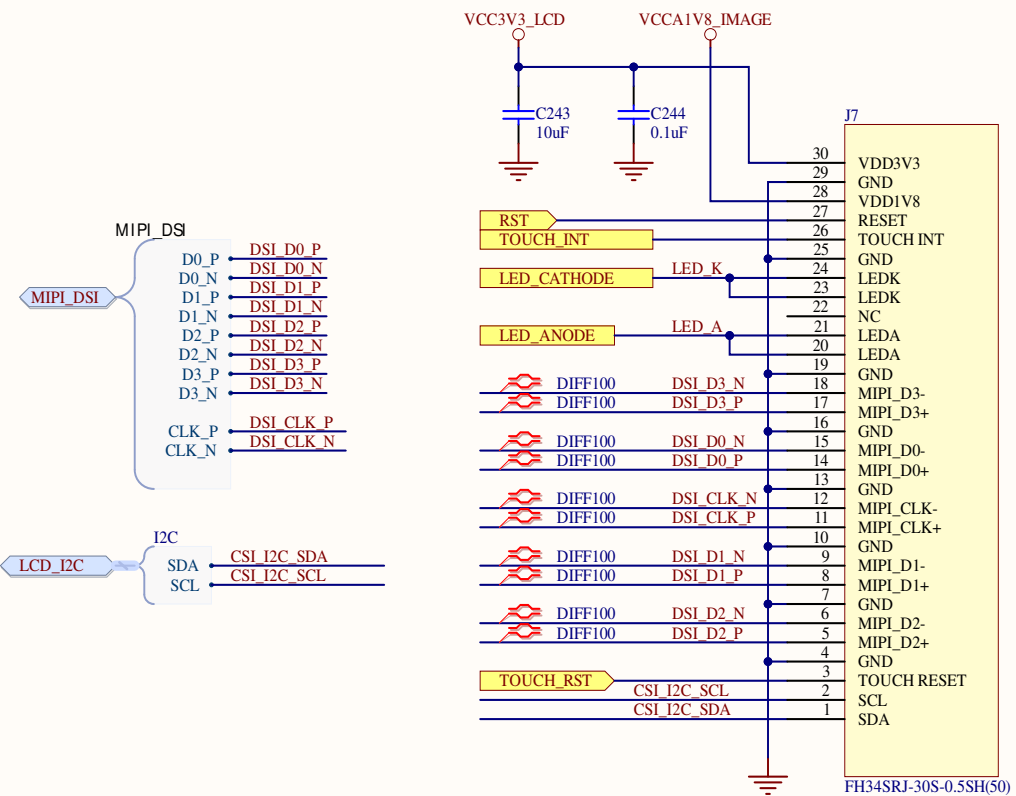


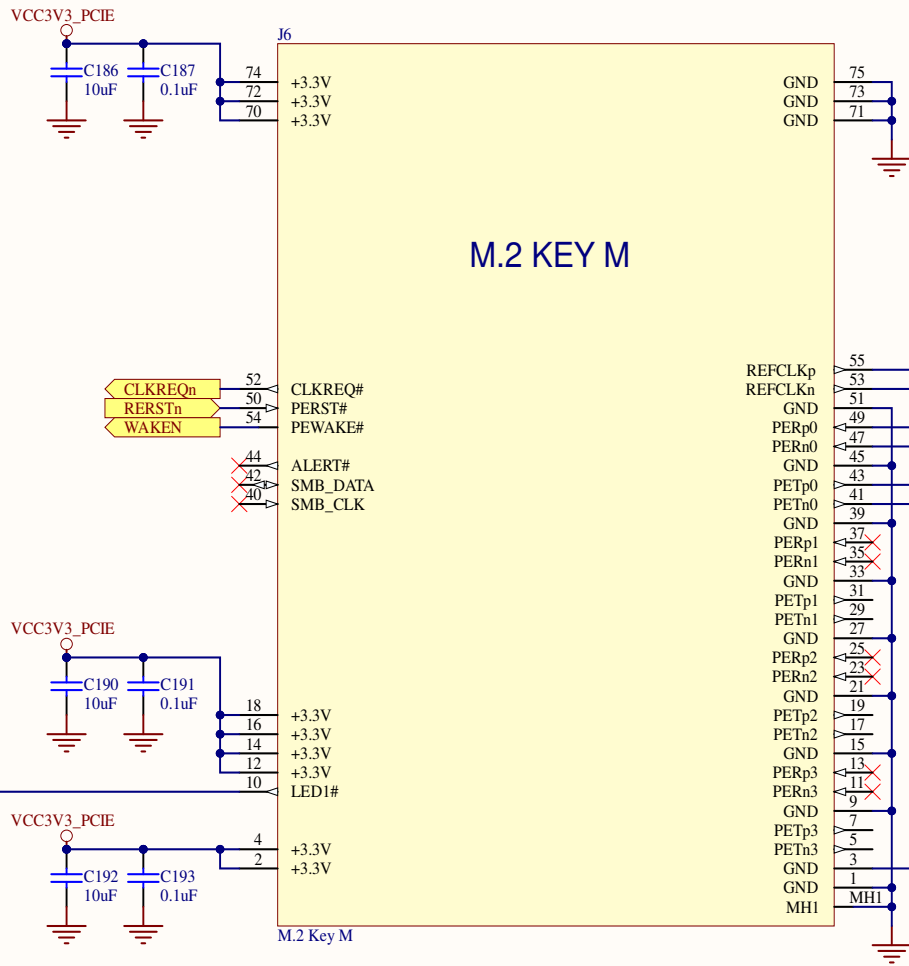
Title Indicator LEDs			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggi-do South Korea		
Size: A4	Number: 29	Revision: 0.1			
Date: 2023-10-16	Time: 오후 3:23:22	Sheet 29 of 41			
File: MIS_LEDS.SchDoc	Designed by: ruppi kim at hardkernel.com				



Title Micro USB Connector			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		
Size: A4	Number: 31	Revision: 0.1			
Date: 2023-10-16	Time: 오후 3:23:22	Sheet 31 of 41			
File: CON_MicroUSB.SchDoc			Designed by: ruppi.kim@hardkernel.com		





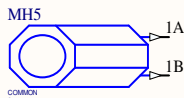
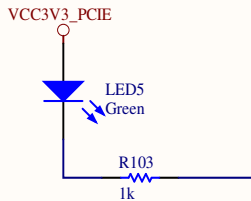


M.2 KEY M

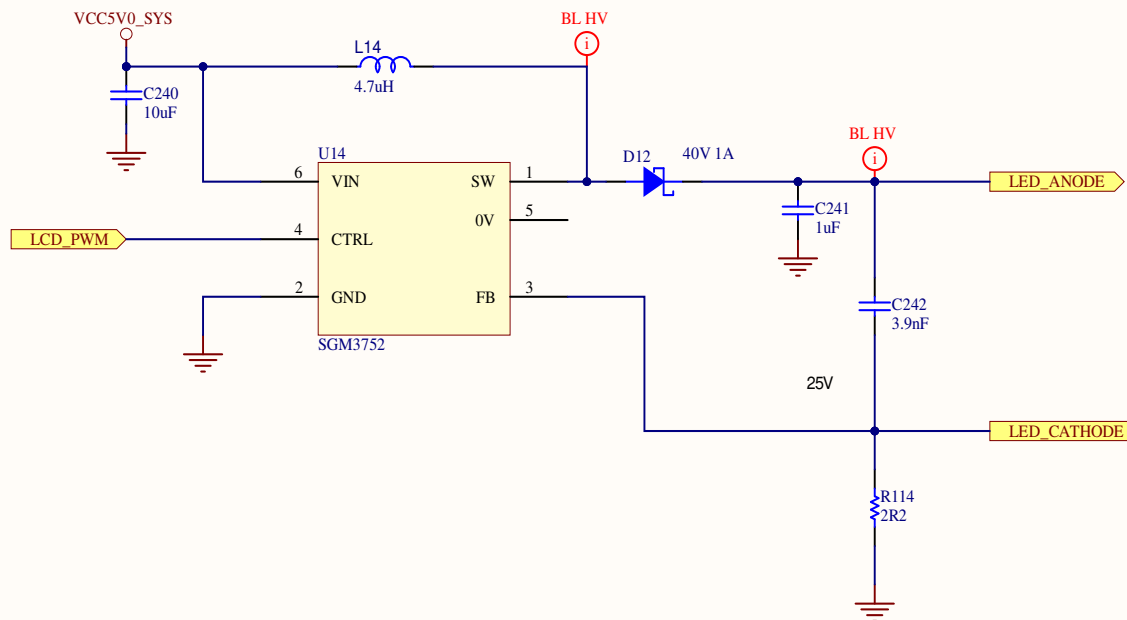
PCIe2

CLK_P
CLK_N

PCIe2



Title M.2 KEY M Connector				Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 37	Revision: 0.1	Designed by: ruppi kim@hardkernel.com			
Date: 2023-10-16	Time: 오후 3:23:22	Sheet 37 of 41				
File: CON_M2.SchDoc						



Title Backlight Driver			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 38	Revision:			
Date: 2023-10-16	Time: 오후 3:23:22	Sheet 38 of 41			
File: BACKLIGHT_SGM3752.SchDoc			Designed by: neal.kim@hardkernel.com		