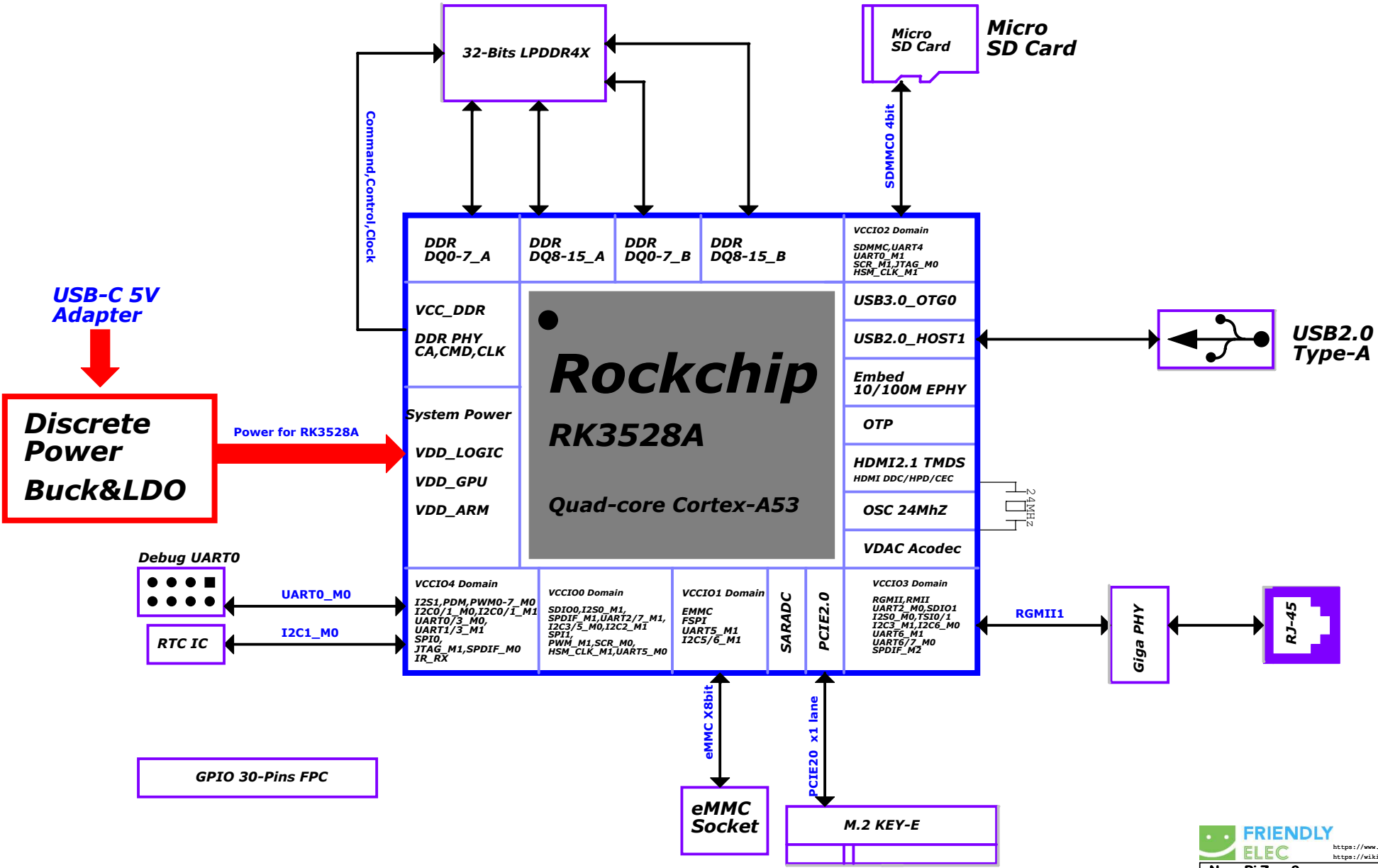
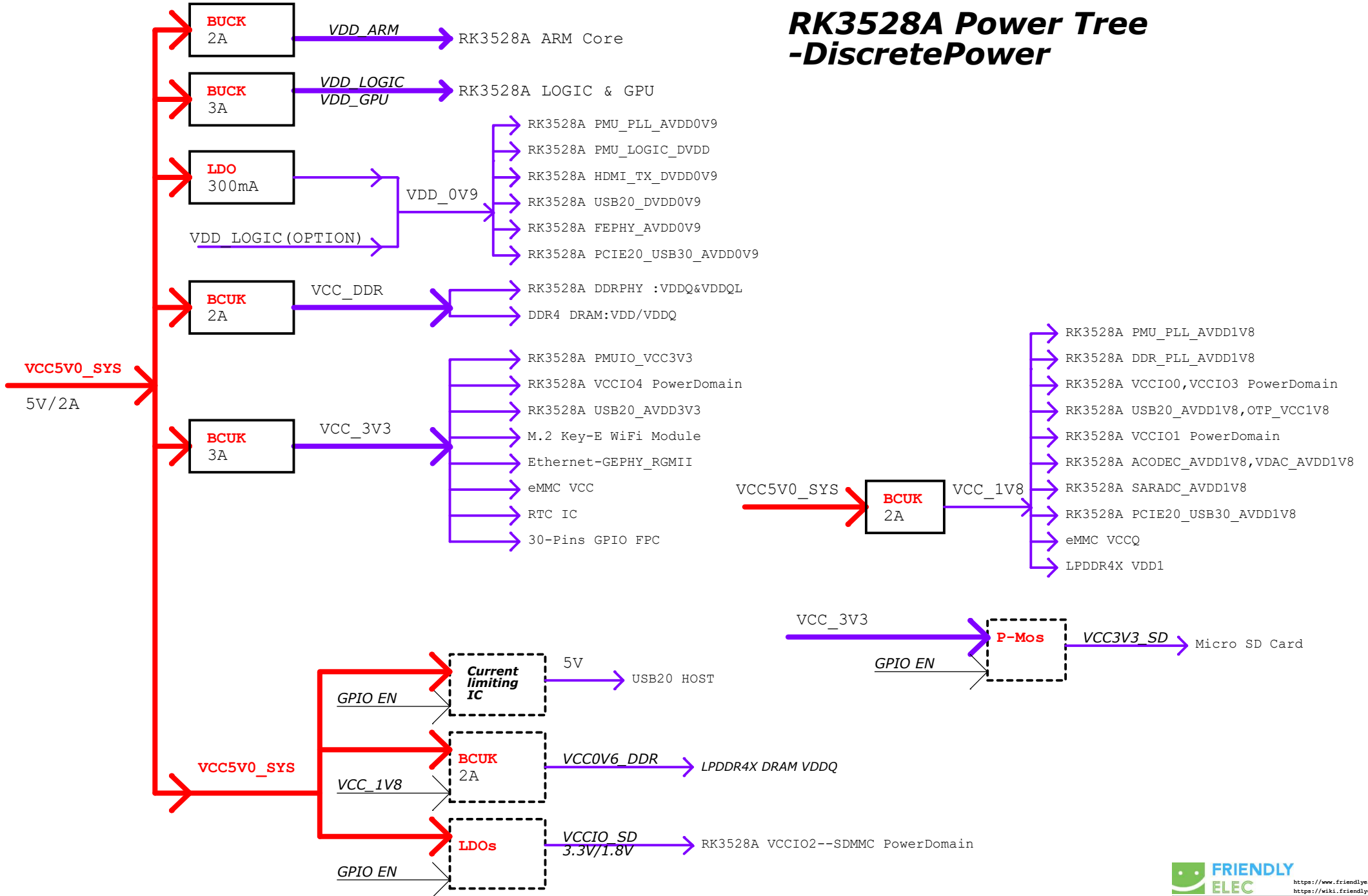


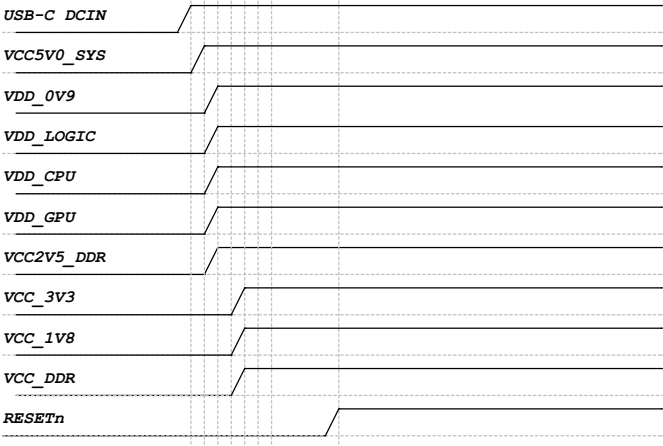
NanoPi Zero2



RK3528A Power Tree -DiscretePower



DiscretePower Power Sequence



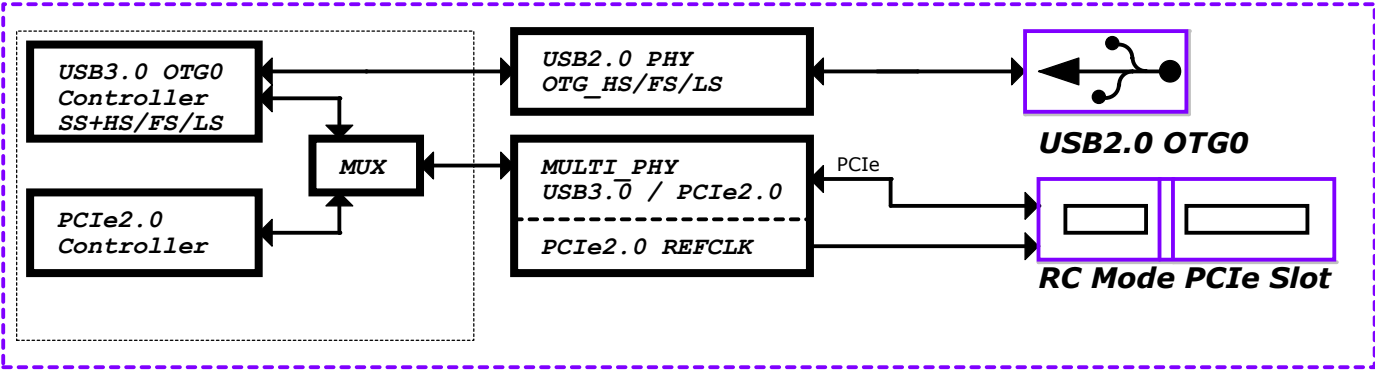
Power Supply	EXT BUCK&LDO	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC5V0_SYS	BUCK1	2.0A	VDD_LOGIC VDD_GPU	Slot:1	0.9V	ON	ON	TBD	TBD
VCC5V0_SYS	BUCK2	2.0A	VDD_ARM	Slot:1	0.95V	ON	ON	TBD	TBD
VCC5V0_SYS	LDO1	0.3A	VDD_0V9	Slot:1	0.9V	ON	ON	TBD	TBD
VCC_3V3	LDO2	1.0A	VCC_1V8	Slot:2	1.8V	ON	ON	TBD	TBD
VCC5V0_SYS	BUCK3	2.0A	VCC_3V3	Slot:2	3.3V	ON	ON	TBD	TBD
VCC5V0_SYS	BUCK4	2.0A	VCC_DDR	Slot:2	ADJ FB=0.6V	ON	ON	TBD	TBD
USB-C DCIN	/	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	ON	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO	Pin 1J13	✓	✗	VCCIO_PMU	VCC_3V3	3.3V	
VCCIO0	Pin 1N6	✓	✓	VCCIO0	VCCIO_WL	1.8V	
VCCIO1	Pin 1P8	✓	✓	VCCIO1	VCCIO_FLASH	1.8V/3.3V	Select as required
VCCIO2	Pin 1B14	✓	✓	VCCIO2	VCCIO_SD	1.8V/3.3V	SD3.0 Voltage=1.8V SD2.0 Voltage=3.3V 3.3V-->1.8V
VCCIO3	Pin 1M13	✓	✓	VCCIO3	VCC_1V8 VCC_3V3	1.8V 3.3V	Select as required
VCCIO4	Pin 1J3	✓	✓	VCCIO4	VCC_3V3	3.3V	

USB3/PCIE Fun Map

Case1: USB2.0 OTG0 + PCIE2.0 x1 Lane



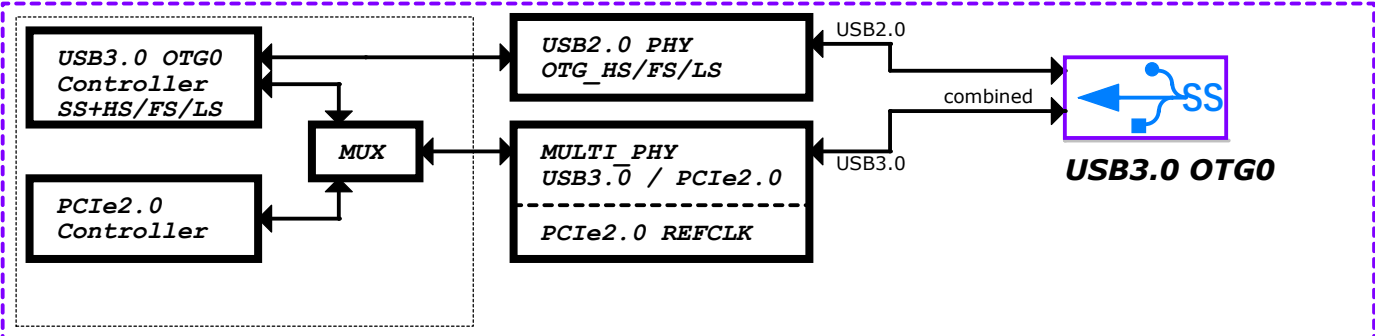
Note 1:

USB3.0 OTG is backward compatible with USB2.0, it needs to occupy the USB2.0 OTG signal pair.

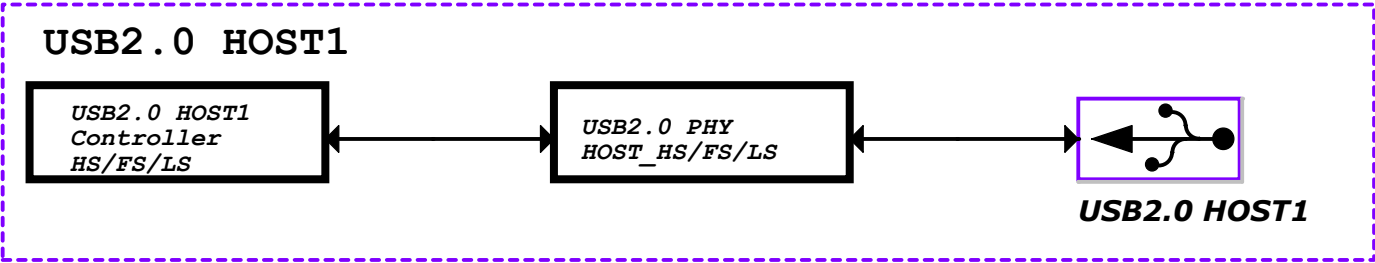
Note 2:

MULTI PHY can be configured for PCIE2.0 or USB3.0 interface. PCIE2.0 only work in RC mode, and support both internal/external clock.

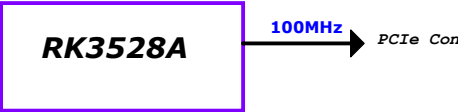
Case2: USB3.0 OTG0



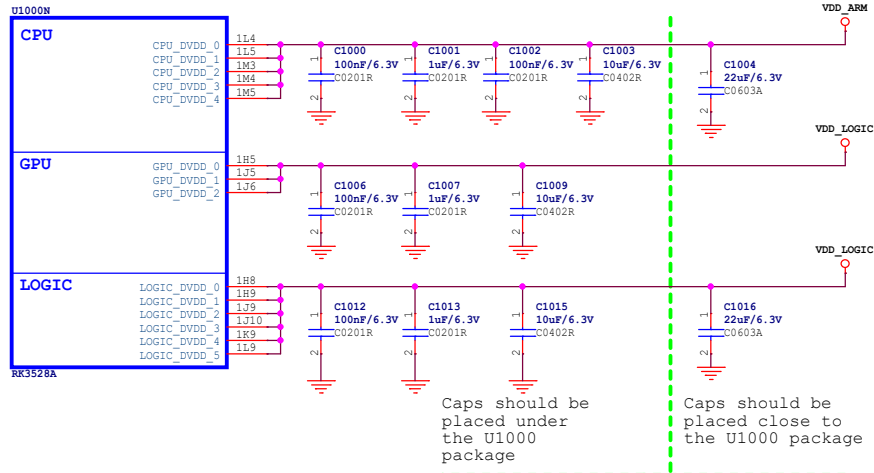
USB2.0 HOST1



PCIE2.0 REFCLK



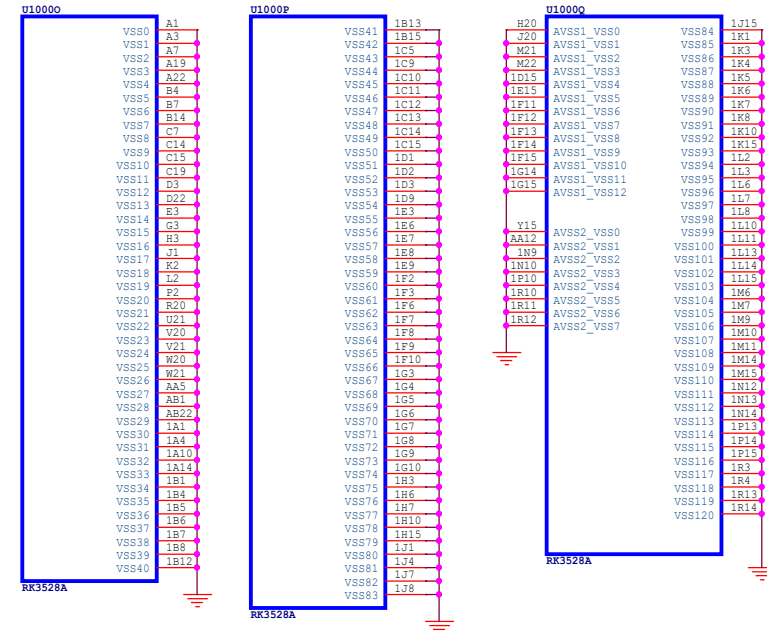
RK3528A_N (POWER)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

RK3528A_O/P/Q (GND)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

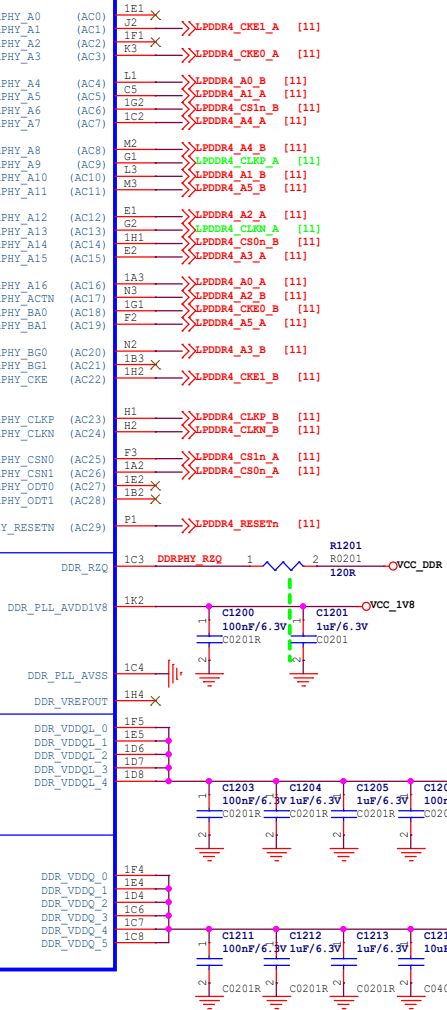
RK3528A_A (DDR PHY)

U1000A									
		DDR4		LPDDR4		DDR3		LPDDR3	
(11)	LPDDR4_DQ0_A	<<<>>>	C4	DDRRHY_A_DQ0	DDR4_DQ0_L_A	LPDDR4_DQ0_A	DDR3_D4	LPDDR3_D0	
(11)	LPDDR4_DQ1_A	<<<>>>	B5	DDRRHY_A_DQ1	DDR4_DQ0_L2_A	LPDDR4_DQ1_A	DDR3_D0	LPDDR3_D1	
(11)	LPDDR4_DQ2_A	<<<>>>	B8	DDRRHY_A_DQ2	DDR4_DQ0_L4_A	LPDDR4_DQ2_A	DDR3_D2	LPDDR3_D2	
(11)	LPDDR4_DQ3_A	<<<>>>	A8	DDRRHY_A_DQ3	DDR4_DQ0_L1_A	LPDDR4_DQ3_A	DDR3_D1	LPDDR3_D3	
(11)	LPDDR4_DQ4_A	<<<>>>	B9	DDRRHY_A_DQ4	DDR4_DQ0_L4_A	LPDDR4_DQ4_A	DDR3_D6	LPDDR3_D4	
(11)	LPDDR4_DQ5_A	<<<>>>	B9	DDRRHY_A_DQ5	DDR4_DQ0_L5_A	LPDDR4_DQ5_A	DDR3_D7	LPDDR3_D5	
(11)	LPDDR4_DQ6_A	<<<>>>	C13	DDRRHY_A_DQ6	DDR4_DQ0_L7_A	LPDDR4_DQ6_A	DDR3_D5	LPDDR3_D6	
(11)	LPDDR4_DQ7_A	<<<>>>	1A8	DDRRHY_A_DQ7	DDR4_DQ0_L3_A	LPDDR4_DQ7_A	DDR3_D3	LPDDR3_D7	
(11)	LPDDR4_DM0_A	<<<>>>	C3	DDRRHY_A_DM0	DDR4_DML_A	LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM0	
(11)	LPDDR4_DQS0P_A	<<<>>>	A6	DDRRHY_A_DQS0P	DDR4_DQSL_P_A	LPDDR4_DQS0P_A	DDR3_DQS0P	LPDDR3_DQS0P	
(11)	LPDDR4_DQS0N_A	<<<>>>	B6	DDRRHY_A_DQS0N	DDR4_DQSL_N_A	LPDDR4_DQS0N_A	DDR3_DQSON	LPDDR3_DQSON	
(11)	LPDDR4_DQ8_A	<<<>>>	C1	DDRRHY_A_DQ8	DDR4_DQ01_A	LPDDR4_DQ8_A	DDR3_D12	LPDDR3_D19	
(11)	LPDDR4_DQ9_A	<<<>>>	C2	DDRRHY_A_DQ9	DDR4_DQ05_A	LPDDR4_DQ9_A	DDR3_D14	LPDDR3_D16	
(11)	LPDDR4_DQ10_A	<<<>>>	C8	DDRRHY_A_DQ10	DDR4_DQ00_A	LPDDR4_DQ10_A	DDR3_D15	LPDDR3_D21	
(11)	LPDDR4_DQ11_A	<<<>>>	1A5	DDRRHY_A_DQ11	DDR4_DQ02_A	LPDDR4_DQ11_A	DDR3_D9	LPDDR3_D17	
(11)	LPDDR4_DQ12_A	<<<>>>	D2	DDRRHY_A_DQ12	DDR4_DQ07_A	LPDDR4_DQ12_A	DDR3_D10	LPDDR3_D20	
(11)	LPDDR4_DQ13_A	<<<>>>	B3	DDRRHY_A_DQ13	DDR4_DQ03_A	LPDDR4_DQ13_A	DDR3_D8	LPDDR3_D23	
(11)	LPDDR4_DQ14_A	<<<>>>	1A7	DDRRHY_A_DQ14	DDR4_DQ04_A	LPDDR4_DQ14_A	DDR3_D13	LPDDR3_D22	
(11)	LPDDR4_DQ15_A	<<<>>>	C11	DDRRHY_A_DQ15	DDR4_DQ06_A	LPDDR4_DQ15_A	DDR3_D11	LPDDR3_D18	
(11)	LPDDR4_DMI_A	<<<>>>	B1	DDRRHY_A_DMI	DDR4_DMU_A	LPDDR4_DMI_A	DDR3_DMI	LPDDR3_DM2	
(11)	LPDDR4_DQS1P_A	<<<>>>	B2	DDRRHY_A_DQS1P	DDR4_DQSU_P_A	LPDDR4_DQS1P_A	DDR3_DQS1P	LPDDR3_DQS2P	
(11)	LPDDR4_DQS1N_A	<<<>>>	A2	DDRRHY_A_DQS1N	DDR4_DQSU_N_A	LPDDR4_DQS1N_A	DDR3_DQS1N	LPDDR3_DQS2N	
(11)	LPDDR4_DQ0_B	<<<>>>	A14	DDRRHY_B_DQ0	DDR4_DQ04_B	LPDDR4_DQ0_B	DDR3_D29	LPDDR3_D14	
(11)	LPDDR4_DQ1_B	<<<>>>	B13	DDRRHY_B_DQ1	DDR4_DQ00_B	LPDDR4_DQ1_B	DDR3_D31	LPDDR3_D12	
(11)	LPDDR4_DQ2_B	<<<>>>	B11	DDRRHY_B_DQ2	DDR4_DQ01_B	LPDDR4_DQ2_B	DDR3_D28	LPDDR3_D13	
(11)	LPDDR4_DQ3_B	<<<>>>	A10	DDRRHY_B_DQ3	DDR4_DQ05_B	LPDDR4_DQ3_B	DDR3_D30	LPDDR3_D18	
(11)	LPDDR4_DQ4_B	<<<>>>	B10	DDRRHY_B_DQ4	DDR4_DQ07_B	LPDDR4_DQ4_B	DDR3_D26	LPDDR3_D9	
(11)	LPDDR4_DQ5_B	<<<>>>	1B11	DDRRHY_B_DQ5	DDR4_DQ03_B	LPDDR4_DQ5_B	DDR3_D24	LPDDR3_D15	
(11)	LPDDR4_DQ6_B	<<<>>>	B15	DDRRHY_B_DQ6	DDR4_DQ06_B	LPDDR4_DQ6_B	DDR3_D27	LPDDR3_D10	
(11)	LPDDR4_DQ7_B	<<<>>>	1B10	DDRRHY_B_DQ7	DDR4_DQ02_B	LPDDR4_DQ7_B	DDR3_D25	LPDDR3_D11	
(11)	LPDDR4_DM0_B	<<<>>>	A15	DDRRHY_B_DM0	DDR4_DMU_B	LPDDR4_DM0_B	DDR3_DM3	LPDDR3_DM1	
(11)	LPDDR4_DQS0P_B	<<<>>>	B12	DDRRHY_B_DQS0P	DDR4_DQSU_P_B	LPDDR4_DQS0P_B	DDR3_DQS3P	LPDDR3_DQS1P	
(11)	LPDDR4_DQS0N_B	<<<>>>	A12	DDRRHY_B_DQS0N	DDR4_DQSU_N_B	LPDDR4_DQS0N_B	DDR3_DQS3N	LPDDR3_DQS1N	
(11)	LPDDR4_DQ8_B	<<<>>>	B18	DDRRHY_B_DQ8	DDR4_DQ01_B	LPDDR4_DQ8_B	DDR3_D17	LPDDR3_D27	
(11)	LPDDR4_DQ9_B	<<<>>>	1A13	DDRRHY_B_DQ9	DDR4_DQ13_B	LPDDR4_DQ9_B	DDR3_D19	LPDDR3_D26	
(11)	LPDDR4_DQ10_B	<<<>>>	A20	DDRRHY_B_DQ10	DDR4_DQ14_B	LPDDR4_DQ10_B	DDR3_D18	LPDDR3_D30	
(11)	LPDDR4_DQ11_B	<<<>>>	B19	DDRRHY_B_DQ11	DDR4_DQ16_B	LPDDR4_DQ11_B	DDR3_D22	LPDDR3_D31	
(11)	LPDDR4_DQ12_B	<<<>>>	B16	DDRRHY_B_DQ12	DDR4_DQ10_B	LPDDR4_DQ12_B	DDR3_D16	LPDDR3_D28	
(11)	LPDDR4_DQ13_B	<<<>>>	B16	DDRRHY_B_DQ13	DDR4_DQ12_B	LPDDR4_DQ13_B	DDR3_D20	LPDDR3_D24	
(11)	LPDDR4_DQ14_B	<<<>>>	1A11	DDRRHY_B_DQ14	DDR4_DQ17_B	LPDDR4_DQ14_B	DDR3_D21	LPDDR3_D25	
(11)	LPDDR4_DQ15_B	<<<>>>	C16	DDRRHY_B_DQ15	DDR4_DQ15_B	LPDDR4_DQ15_B	DDR3_D23	LPDDR3_D29	
(11)	LPDDR4_DMI_B	<<<>>>	C18	DDRRHY_B_DMI	DDR4_DMI_B	LPDDR4_DMI_B	DDR3_DM2	LPDDR3_DM3	
(11)	LPDDR4_DQS1P_B	<<<>>>	B17	DDRRHY_B_DQS1P	DDR4_DQSL_P_B	LPDDR4_DQS1P_B	DDR3_DQS2P	LPDDR3_DQS3P	
(11)	LPDDR4_DQS1N_B	<<<>>>	A17	DDRRHY_B_DQS1N	DDR4_DQSL_N_B	LPDDR4_DQS1N_B	DDR3_DQS2N	LPDDR3_DQS3N	

RK3528A

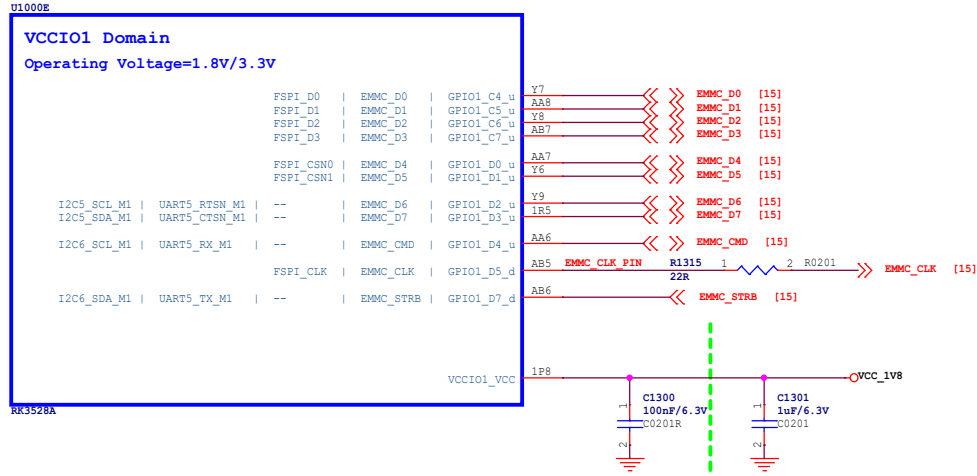
DDR4	LPDDR4	DDR3	LPDDR3
DDR4_A0	LPDDR4_ODT1_B	DDR3_A9	LPDDR3_ODT2
DDR4_A1	LPDDR4_CKE1_A	DDR3_A14	--
DDR4_A2	LPDDR4_ODT0_B	DDR3_A13	LPDDR3_ODT3
DDR4_A3	LPDDR4_CKE0_A	DDR3_A1	--
DDR4_A4	LPDDR4_A0_B	DDR3_A2	LPDDR3_A5
DDR4_A5	LPDDR4_A1_A	DDR3_A4	--
DDR4_A6	LPDDR4_CSN1_B	DDR3_A3	LPDDR3_CSN2
DDR4_A7	LPDDR4_A4_A	DDR3_A6	--
DDR4_A8	LPDDR4_A4_B	DDR3_A5	LPDDR3_A6
DDR4_A9	LPDDR4_CLKP_A	DDR3_A11	LPDDR3_A2
DDR4_A10	LPDDR4_A1_B	DDR3_A0	--
DDR4_A11	LPDDR4_A5_B	DDR3_A7	LPDDR3_A7
DDR4_A12	LPDDR4_A2_A	DDR3_A10	LPDDR3_A4
DDR4_A13	LPDDR4_CLKN_A	DDR3_A8	LPDDR3_A3
DDR4_WEN/A14	LPDDR4_CSN0_B	DDR3_ODT0	LPDDR3_CSN3
DDR4_CASN/A15	LPDDR4_A3_A	DDR3_BA1	LPDDR3_A0
DDR4_RASN/A16	LPDDR4_A0_A	DDR3_CKE0	--
DDR4_ACTN	LPDDR4_A2_B	DDR3_CSN0	LPDDR3_A9
DDR4_BA0	LPDDR4_CKE0_B	DDR3_BA2	LPDDR3_CKE0
DDR4_BA1	LPDDR4_A5_A	DDR3_A12	LPDDR3_A1
DDR4_BG0	LPDDR4_A3_B	DDR3_BA0	LPDDR3_A8
DDR4_BG1	--	DDR3_A15	--
DDR4_CKE	LPDDR4_CKE1_B	DDR3_RASN	--
DDR4_CLKP	LPDDR4_CLKP_B	DDR3_CLKP	LPDDR3_CLKP
DDR4_CLKN	LPDDR4_CLKN_B	DDR3_CLKN	LPDDR3_CLKN
DDR4_CSN0	LPDDR4_CSN1_A	DDR3_CASN	LPDDR3_CSN1
DDR4_CSN1	LPDDR4_CSN0_A	DDR3_CSN1	LPDDR3_CSN0
DDR4_ODT0	LPDDR4_ODT1_A	DDR3_WEN	LPDDR3_ODT0
DDR4_ODT1	LPDDR4_ODT0_A	DDR3_ODT1	LPDDR3_ODT1
DDR4_RESETN	LPDDR4_RESETN	DDR3_RESETN	--

Note: Sequences can not be swap



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

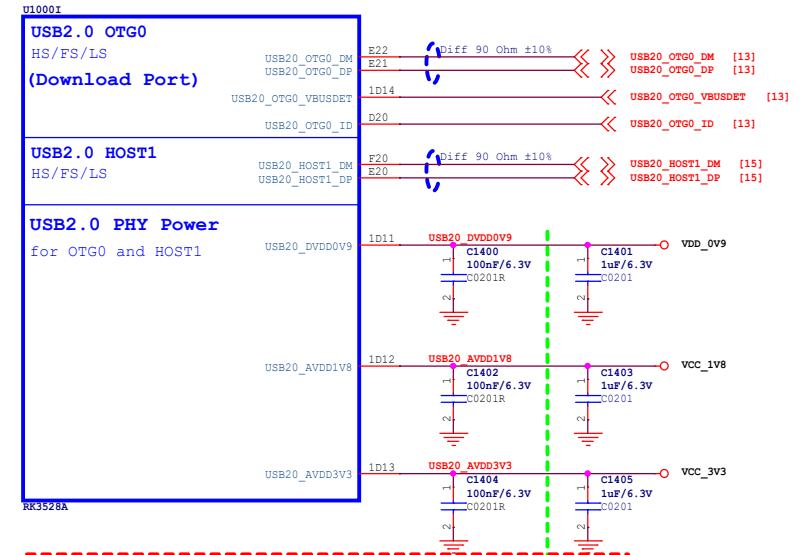
RK3528A_E (VCCIO1 Domain)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

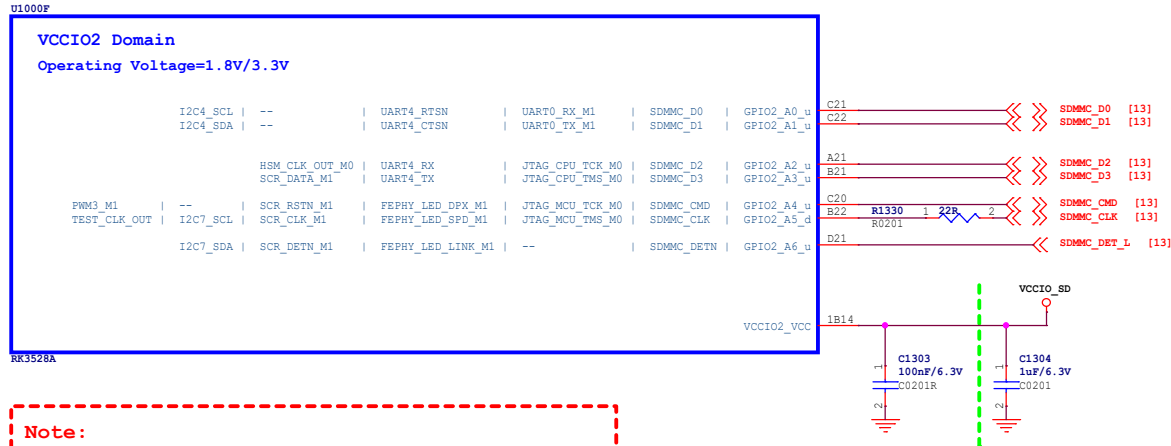
RK3528A_I (USB2.0 OTG/HOST)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

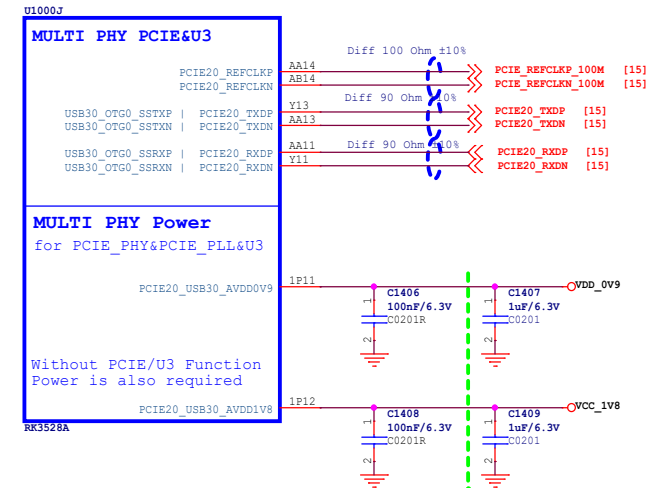
RK3528A_F (VCCIO2 Domain)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

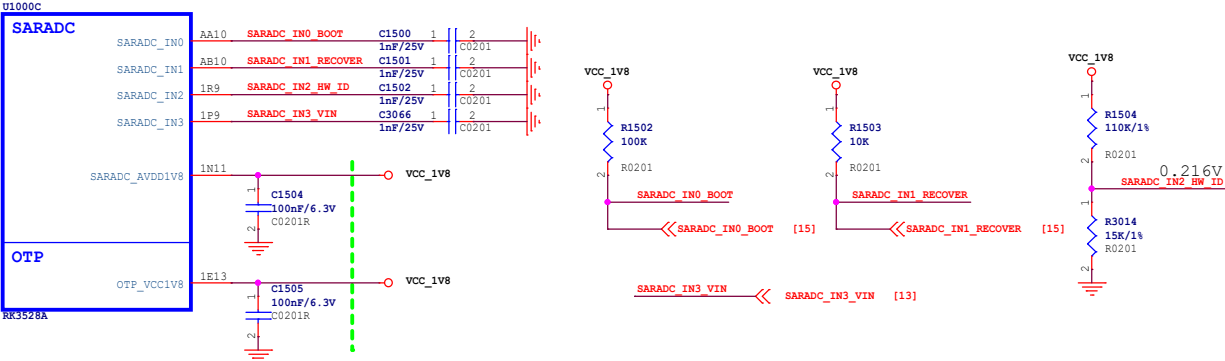
RK3528A_J (PCIE2.0/U3 PHY)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

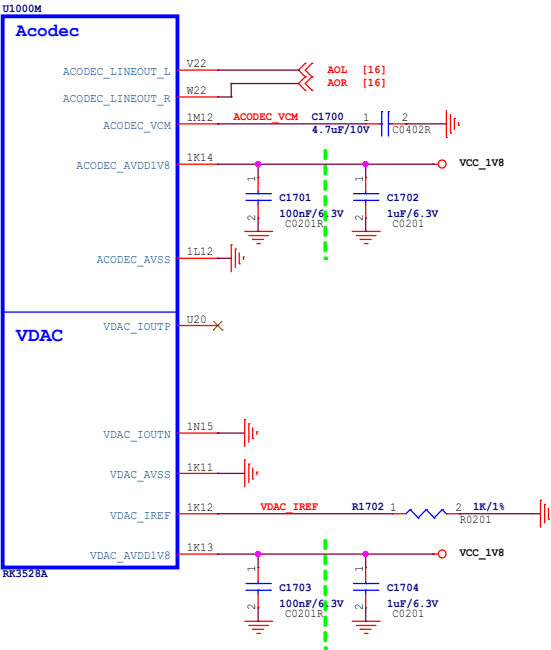
RK3528A_C (Saradc/OTP)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

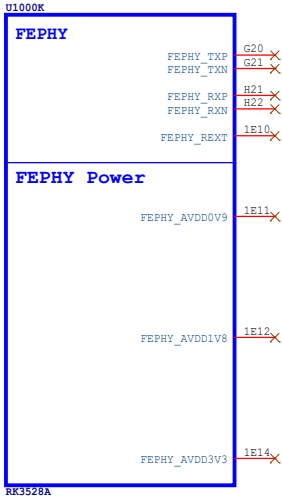
Item	Rup	Rdown	ADC	BOOT MODE
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	12K	114	
LEVEL3	100K	27K	228	FSPI--USB
LEVEL4	100K	51K	342	
LEVEL5	100K	82K	456	
LEVEL6	100K	120K	570	EMMC--USB
LEVEL7	100K	200K	683	EMMC--SD Card--USB
LEVEL8	100K	330K	796	SD Card--USB
LEVEL9	100K	820K	910	
LEVEL10	100K	DNP	1023	FSPI--EMMC--SD Card--USB

RK3528A_M (Acodec/VDAC)

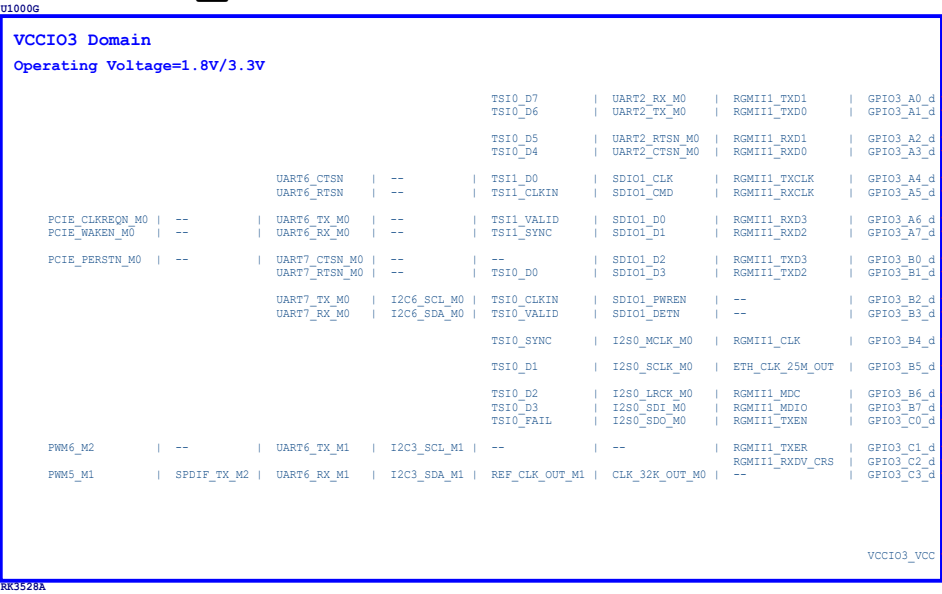


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

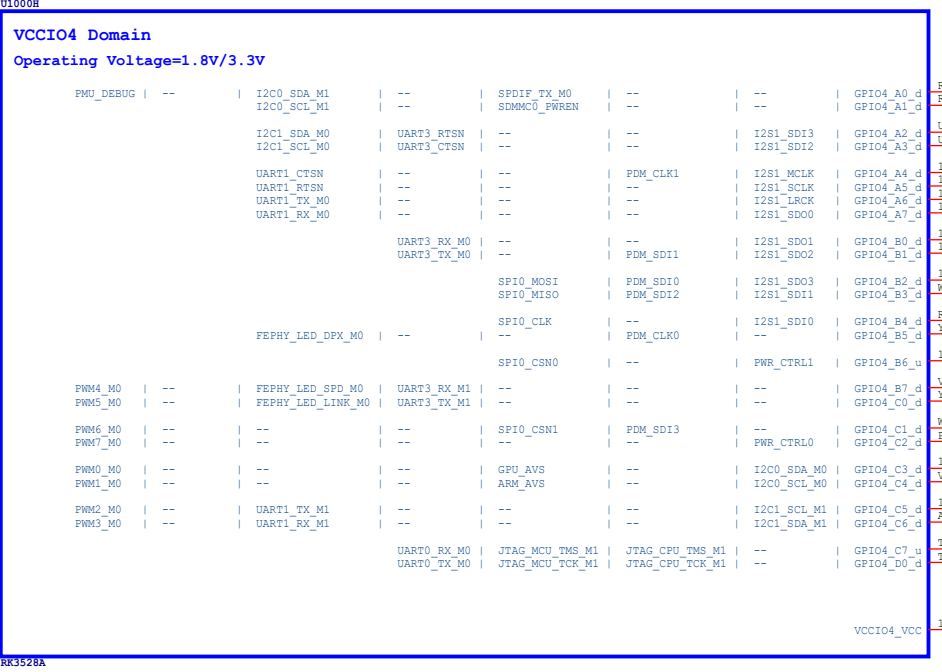
RK3528A_K (Embed FEPHY)



RK3528A_G (VCCIO3 Domain)



RK3528A_H (VCCIO4 Domain)

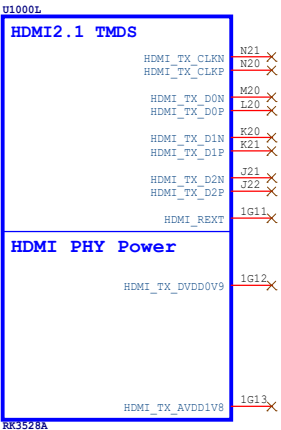


Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.

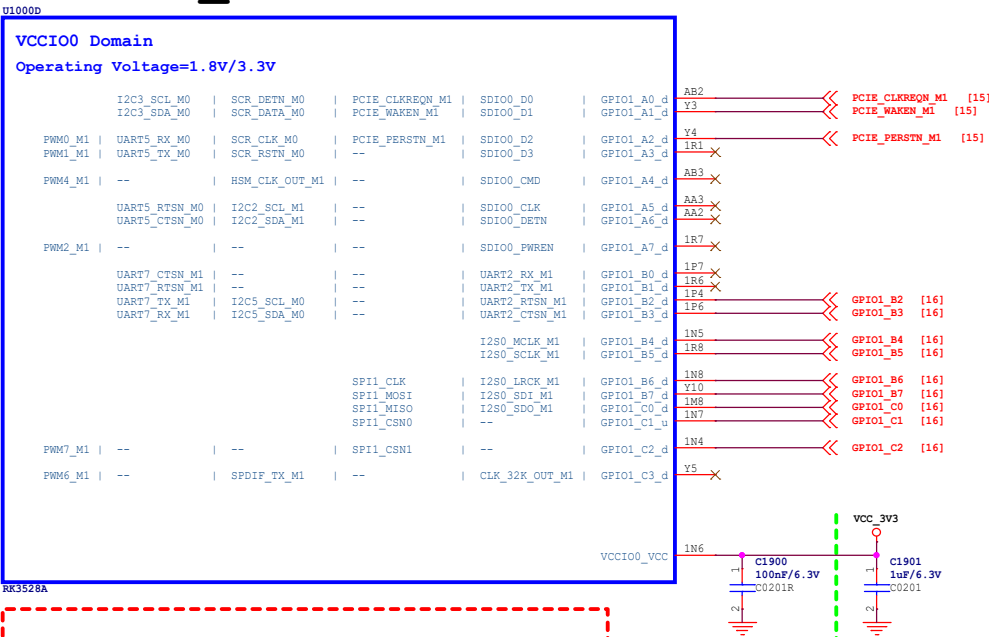
Other caps should be placed close to the U1000 package

RK3528A_L (HDMI PHY)



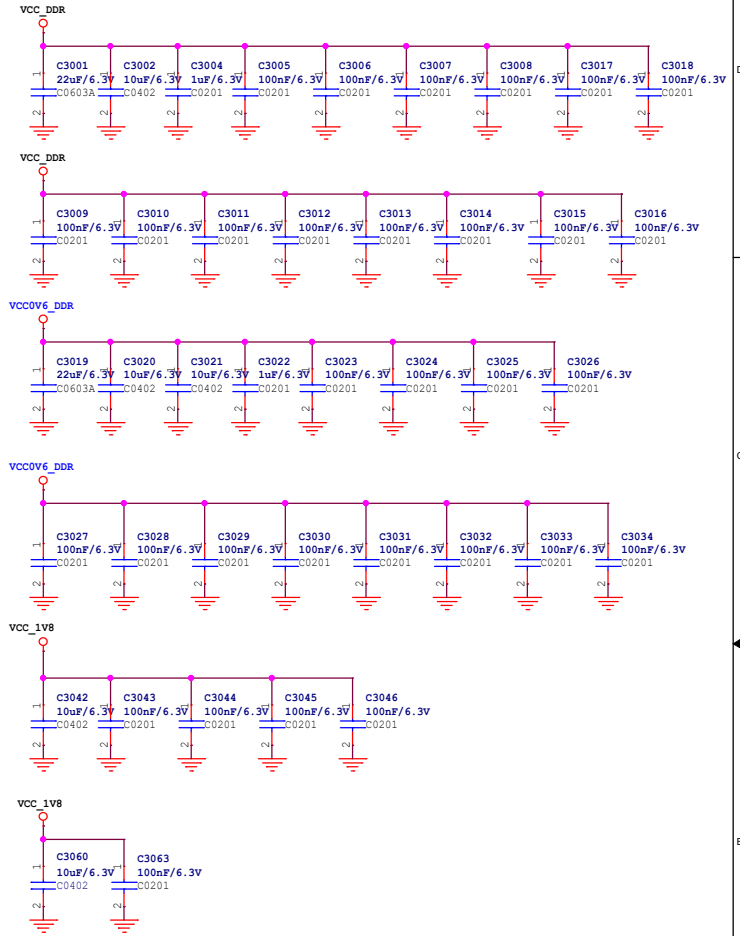
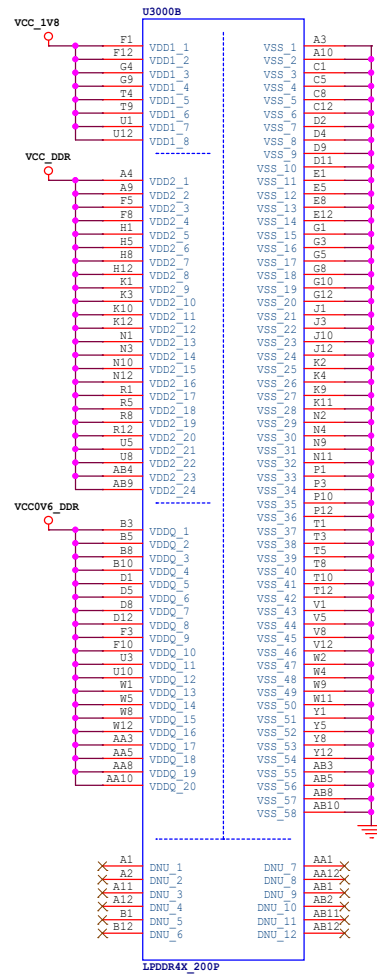
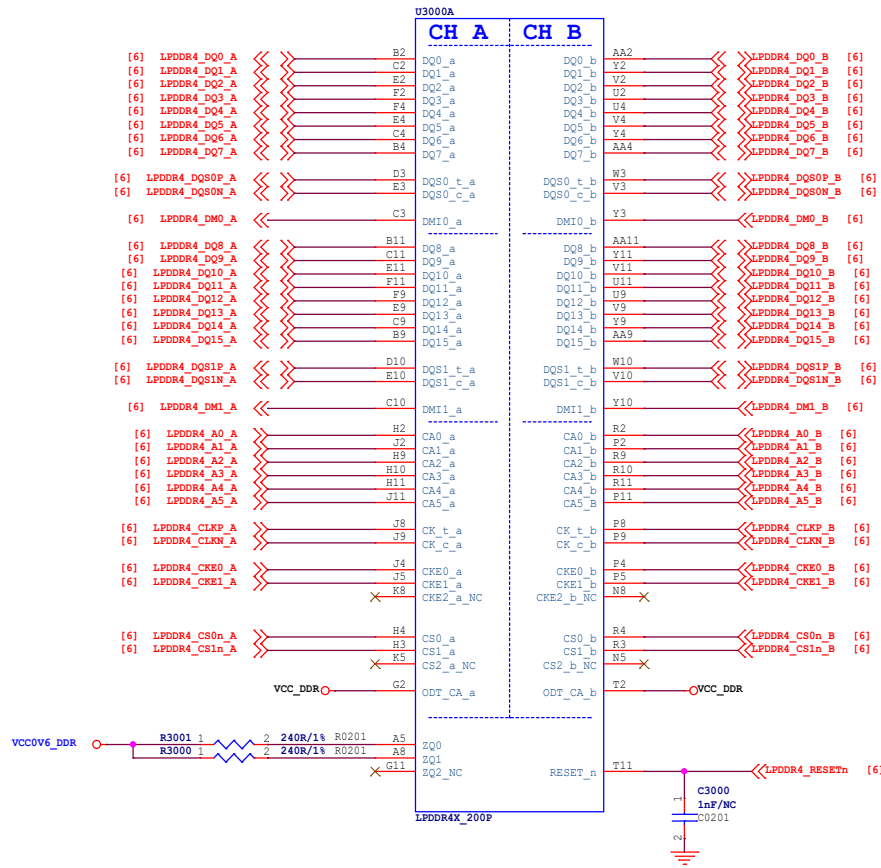
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3528A_D (VCCIO0 Domain)

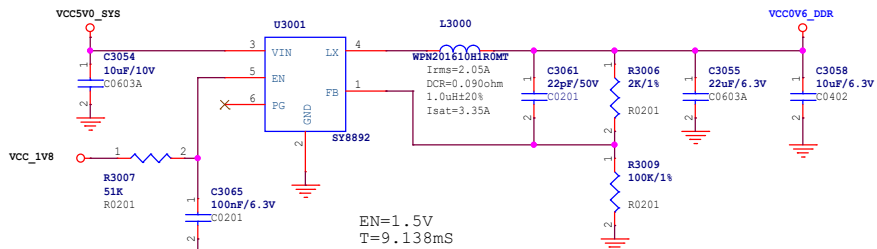


Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

**LPDDR4X
200Ball**

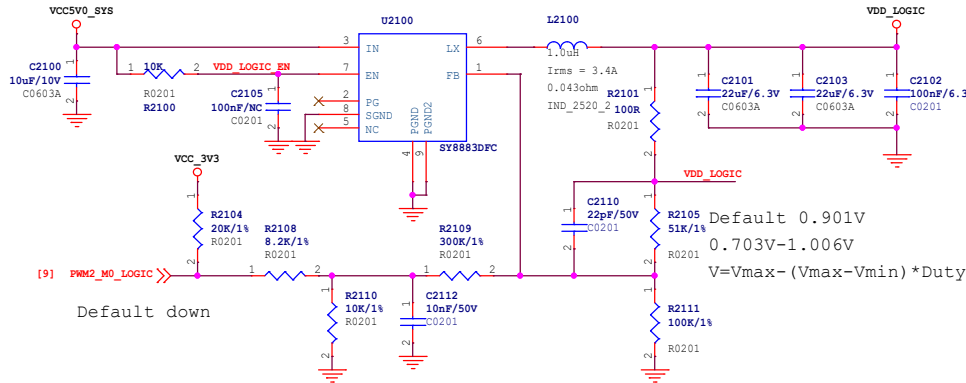


VCC0V6_DDR



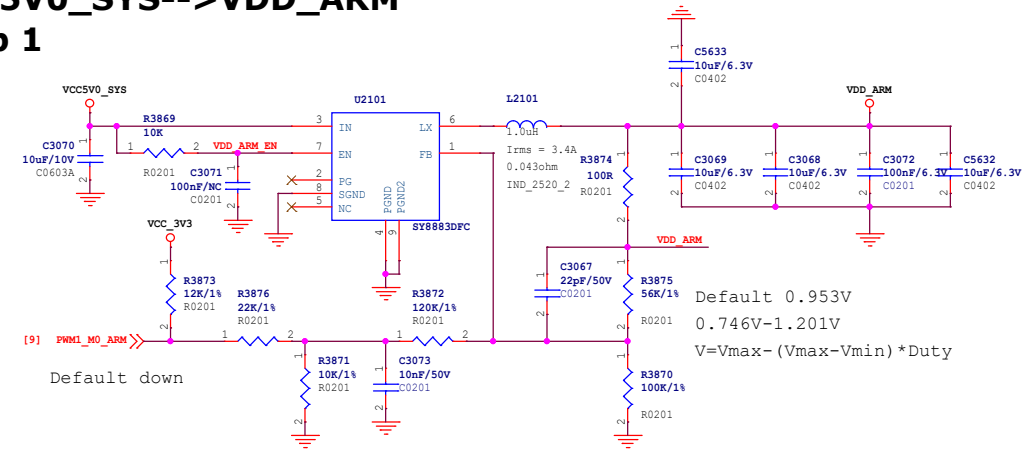
VCC5V0_SYS-->VDD_LOGIC

Step 1



VCC5V0_SYS-->VDD_ARM

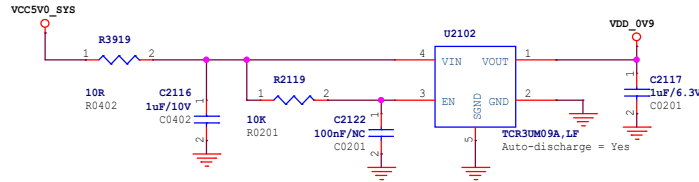
Step 1



VCC5V0_SYS-->VDD_0V9

Step 1

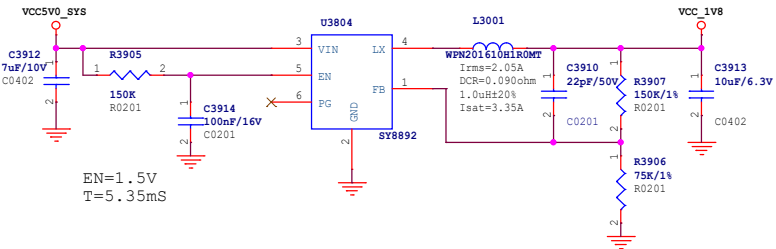
Note:
When LAYOUT, a star must be used,
Branch to each load



VCC_3V3->VCC_1V8

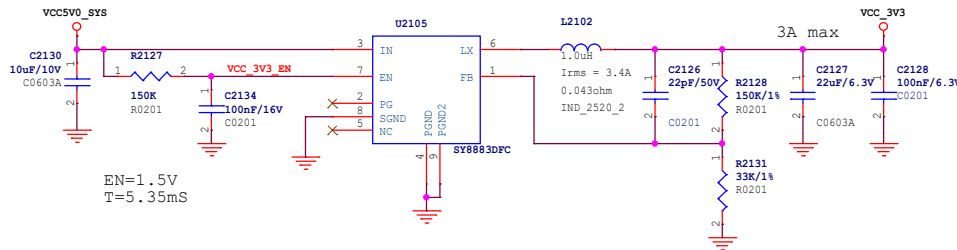
Step 2

Note:
When LAYOUT, a star must be used,
Branch to each load



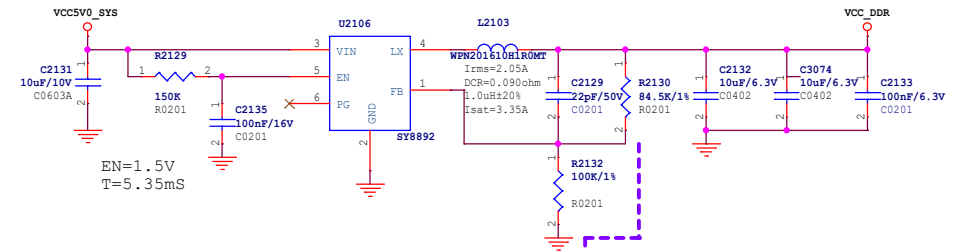
VCC5V0_SYS-->VCC_3V3

Step 2



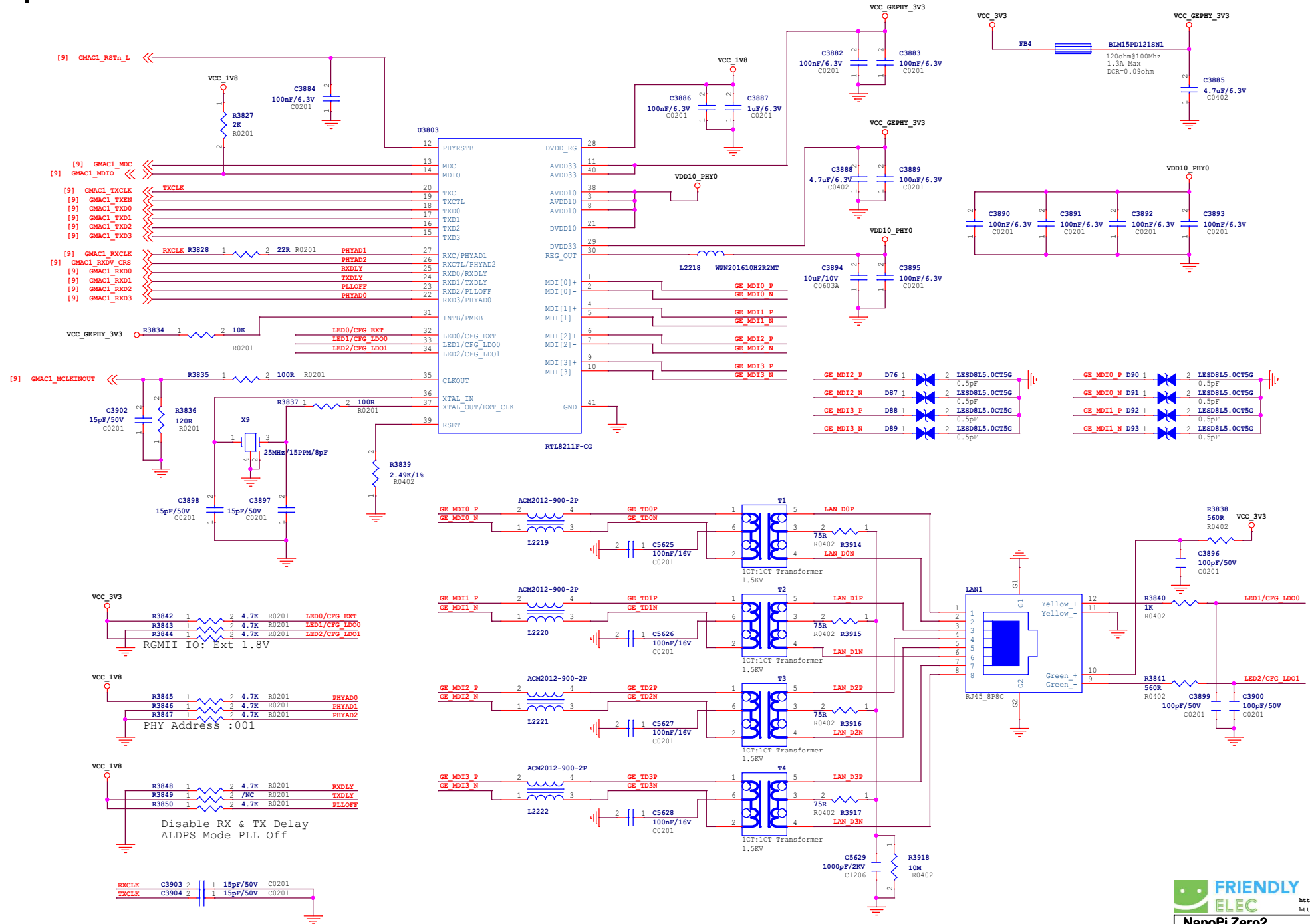
VCC5V0_SYS-->VCC_DDR

Step 2

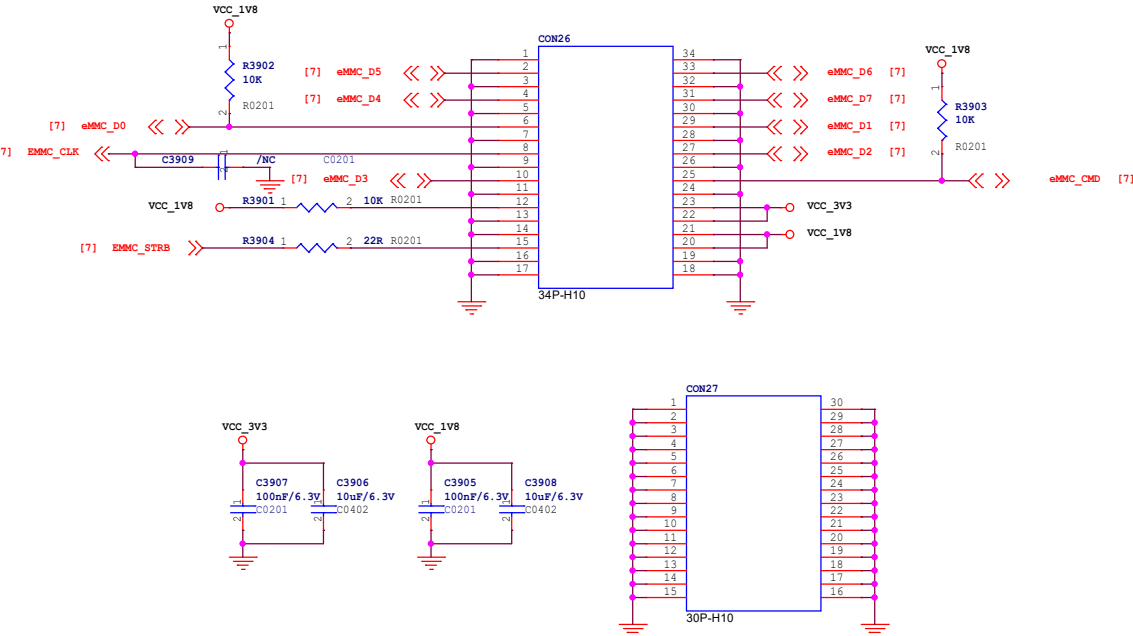


DDR4	1.20V	100K	1%
LPDDR4/4x	1.10V	84.5K	1%
DDR3	1.5V	150K	1%
DDR3L	1.35V	127K	1%
LPDDR3	1.25V	110K	1%

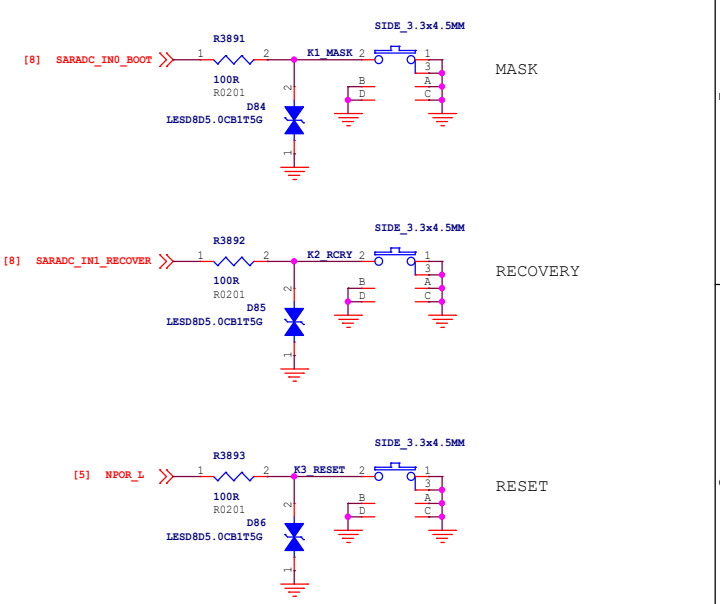
Gbps Ethernet



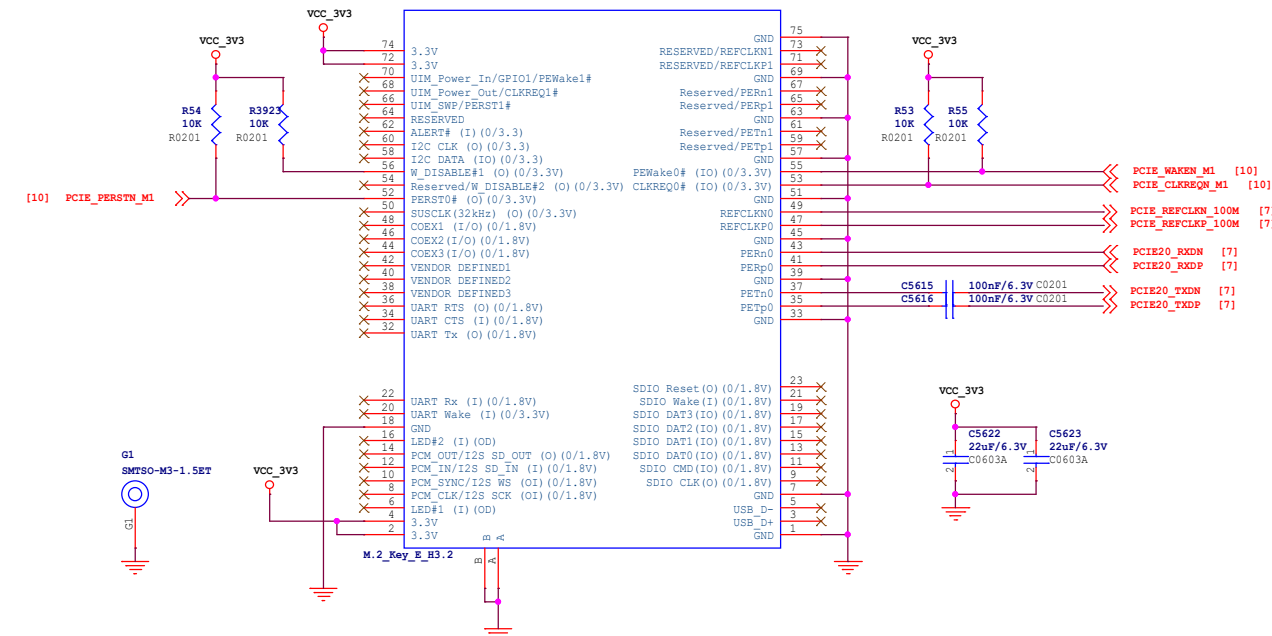
eMMC Socket



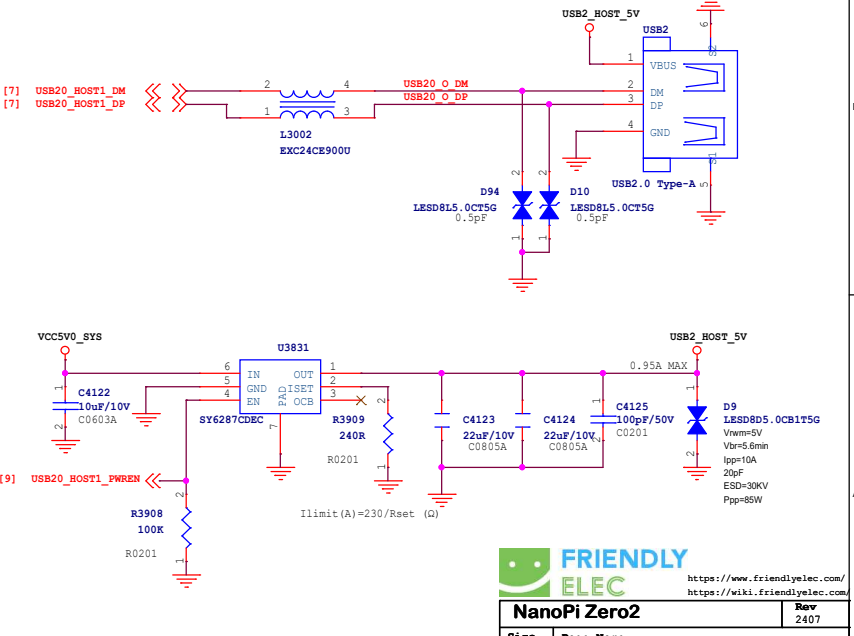
Buttons



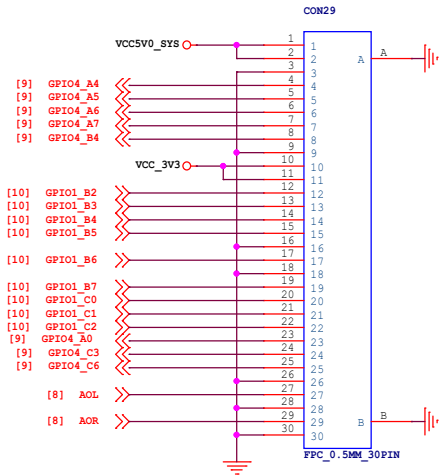
M.2 Key-E PCIe WiFi



USB2.0



GPIO



TABLE

GPIOs	Alt Functions			Level
GPIO4_A0	SPDIF_TX_M0			3.3V
GPIO4_A4	UART1_CTSN	I2S1_MCLK		3.3V
GPIO4_A5	UART1_RTSN	I2S1_SCLK		3.3V
GPIO4_A6	UART1_TX_M0	I2S1_LRCK		3.3V
GPIO4_A7	UART1_RX_M0	I2S1_SDO0		3.3V
GPIO4_B4		I2S1_SDI0		3.3V
GPIO4_C3	PWM0_M0			3.3V
GPIO4_C6	PWM3_M0			3.3V
GPIO1_C1	SPI1_CSN0			3.3V
GPIO1_C2	SPI1_CSN1			3.3V
GPIO1_B6	SPI1_CLK	I2S0_LRCK_M1		3.3V
GPIO1_B7	SPI1_MOSI	I2S0_SDI_M1		3.3V
GPIO1_C0	SPI1_MISO	I2S0_SDO_M1		3.3V
GPIO1_B4		I2S0_MCLK_M1		3.3V
GPIO1_B5		I2S0_SCLK_M1		3.3V
GPIO1_B2	I2C5_SCL_M0*	UART7_TX_M1		3.3V
GPIO1_B3	I2C5_SDA_M0*	UART7_RX_M1		3.3V

* An external 2.2K pull-up resistor is required.