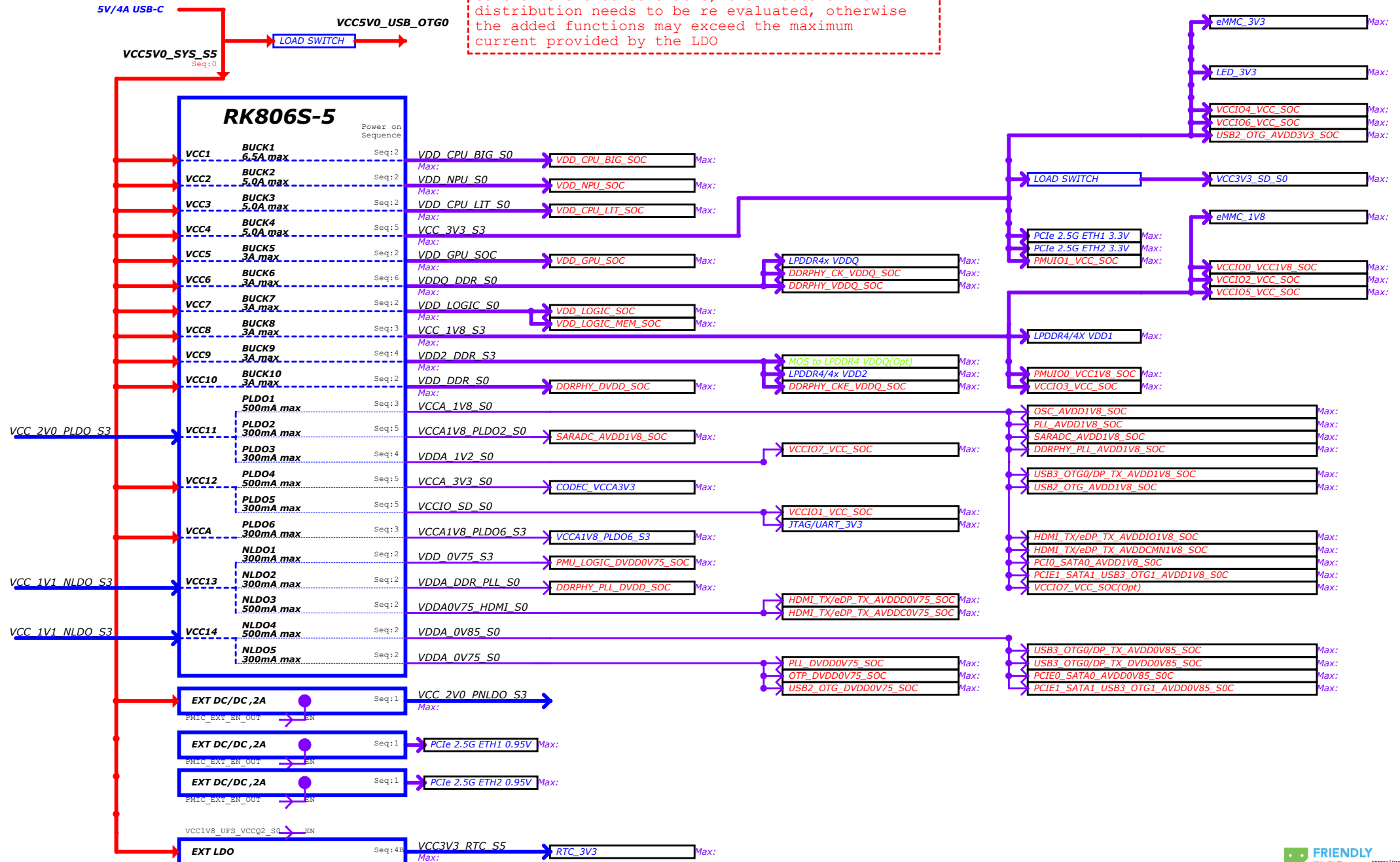


NanoPi R76S

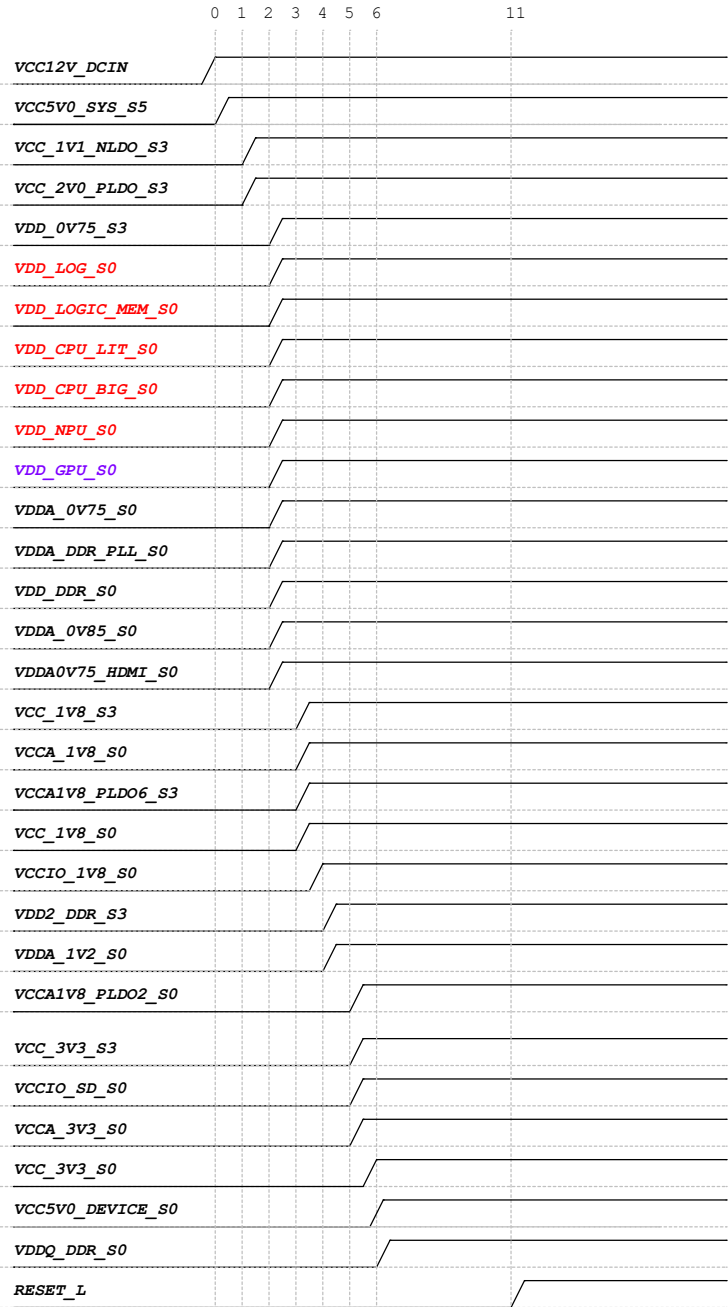
Power Tree

Note:

The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic. If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re-evaluated, otherwise the added functions may exceed the maximum current provided by the LDO.



Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC5V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK3	5A	VDD_CPU_LIT_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	0.61V-LP4/4x 0.51V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK7	3A	VDD_LOGIC_S0 VDD_LOGIC_MEM_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x 1.05V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_PLDO2_S0	Slot:5	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO4	0.5A	VCCA_3V3_S0	Slot:5	3.0V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA0V75_HDMI_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETn								
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_2V0_PLDO_S3	Slot:1	2.1V	ON	2.0V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	6A	VCC5V0_SYS_S5	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_DEVICE_S0	Slot:5A	5.2V	ON	5.2V	TBD	TBD
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	TBD	TBD
VCC_1V8_S3	SWITCH	2A	VCCIO_1V8_S0	Slot:3A	1.8V	ON	1.8V	TBD	TBD

Note:

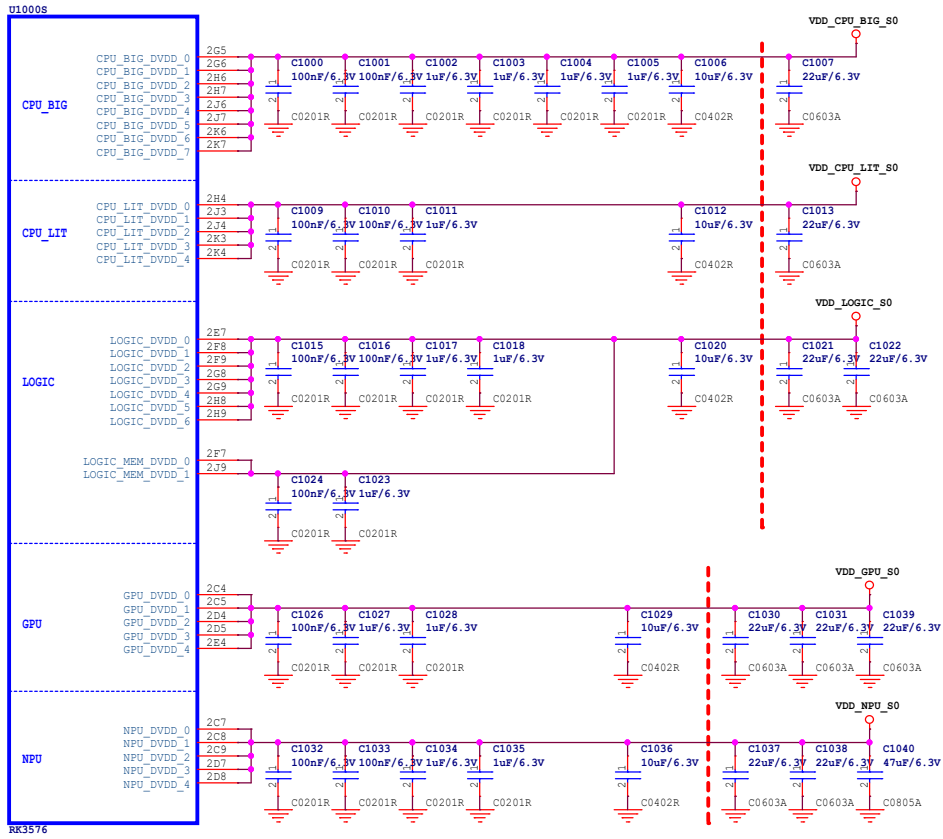
The power suffix S0, S3 or S5 means:
S5: Keep power on during power down
S3: Keep power on during sleeping
S0: Power off during sleeping

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO0	Pin 2K11	1.8V Only	PMUIO0_VCC1V8	VCC_1V8	1.8V
PMUIO1	Pin 1U20	1.8V or 3.3V	PMUIO1_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO0	Pin 1J20	1.8V Only	VCCIO0_VCC1V8	VCC_1V8	1.8V
VCCIO1	Pin 2A8	1.8V or 3.3V	VCCIO1_VCC	VCC_1V8 VCC_3V3	1.8V/3.3V
VCCIO2	Pin 2A2	1.8V or 3.3V	VCCIO2_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO3	Pin 2B10	1.8V or 3.3V	VCCIO3_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO4	Pin 2A7	1.8V or 3.3V	VCCIO4_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO5	Pin 2A4/2A5	1.8V or 3.3V	VCCIO5_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO6	Pin 2N3	1.8V or 3.3V	VCCIO6_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO7	Pin 2M3	1.2V or 1.8V	VCCIO7_VCC	VCC_1V2 VCC_1V8	1.2V

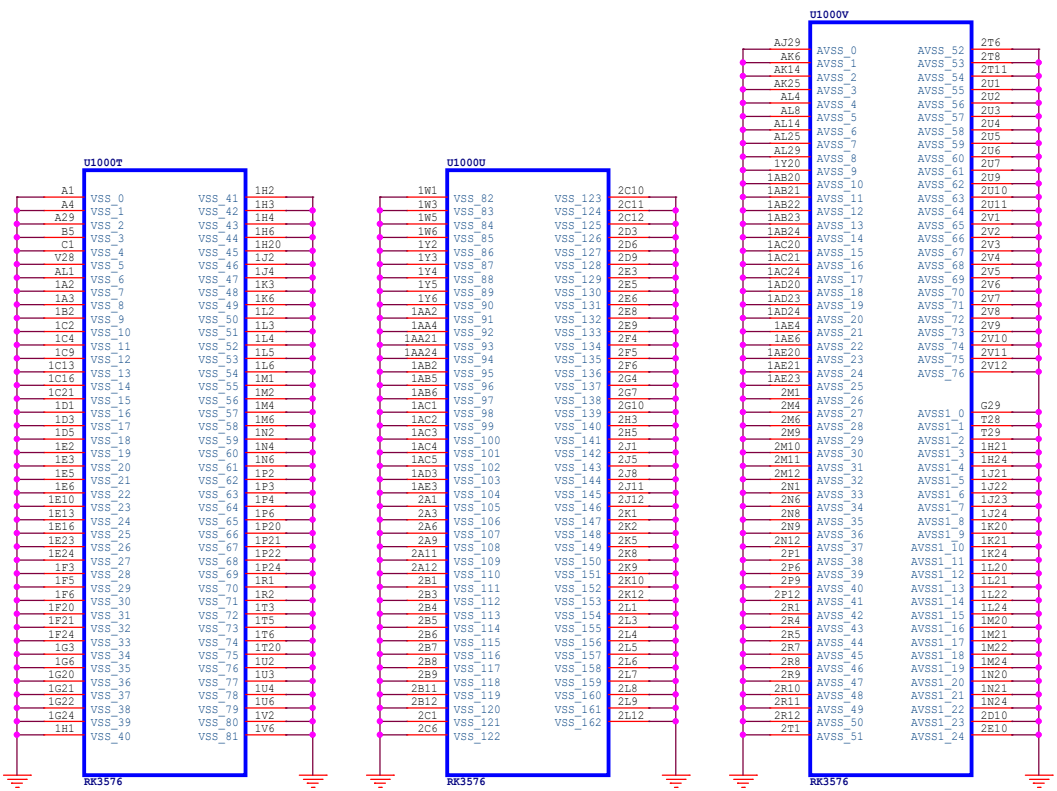
IO Type	Operating Voltage
1.8V Only	VCCIO*_VCC1V8=1.8V
1.2V or 1.8V	VCCIO*_VCC=1.2V or 1.8V
1.8V or 3.3V	VCCIO*_VCC=1.8V or 3.3V

RK3576_S (Power)

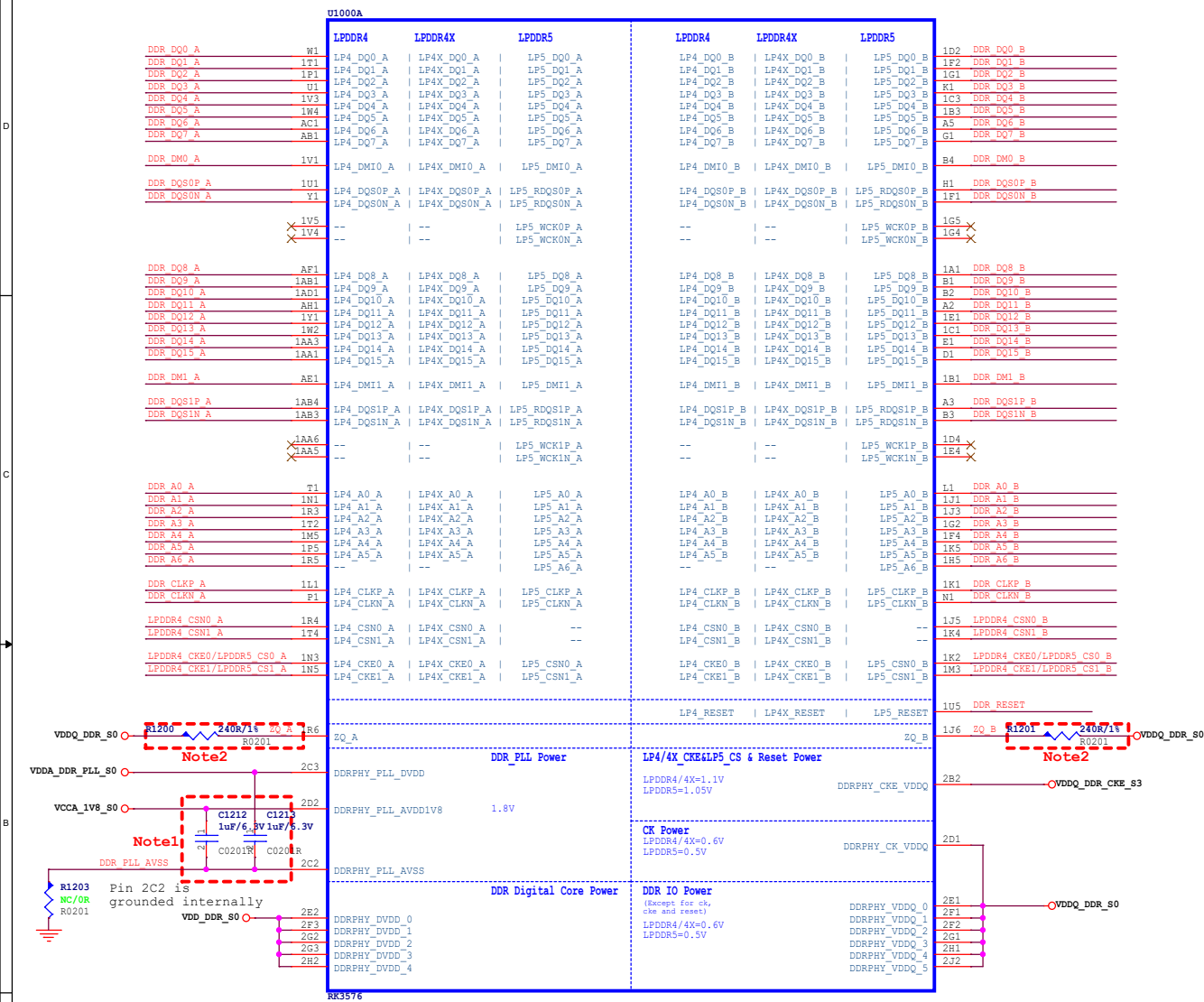


Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

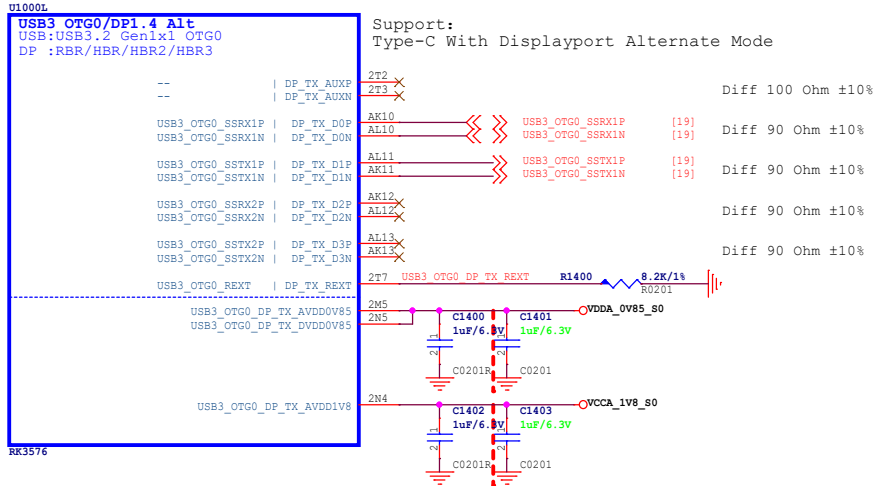
RK3576_T/U/V (GND)



RK3576_A (DDRPHY)



RK3576_L (USB3/DP)

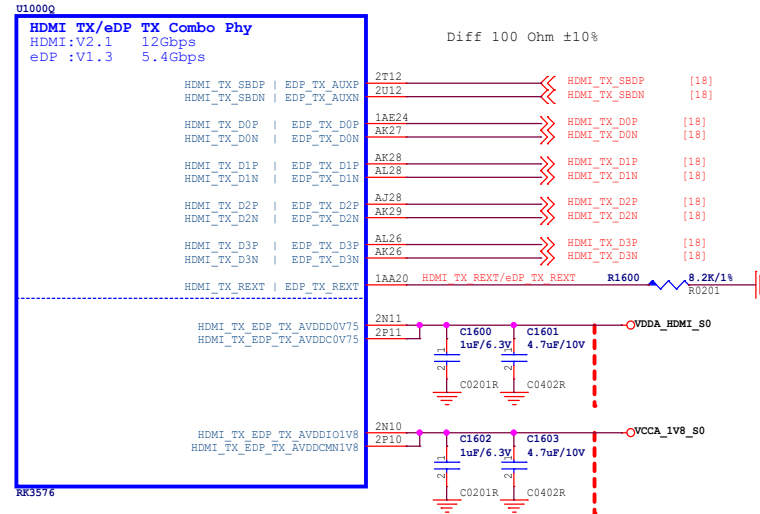


Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_Q (HDMI/eDP)

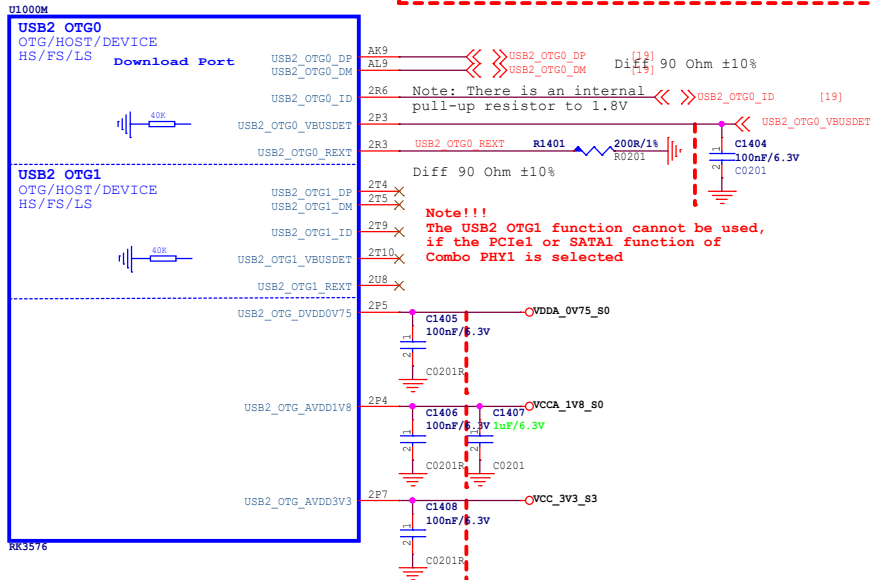
Note:
HDMI 2.1 supports up to 4Kx2K@120Hz
eDP :V1.3 5.4Gbps



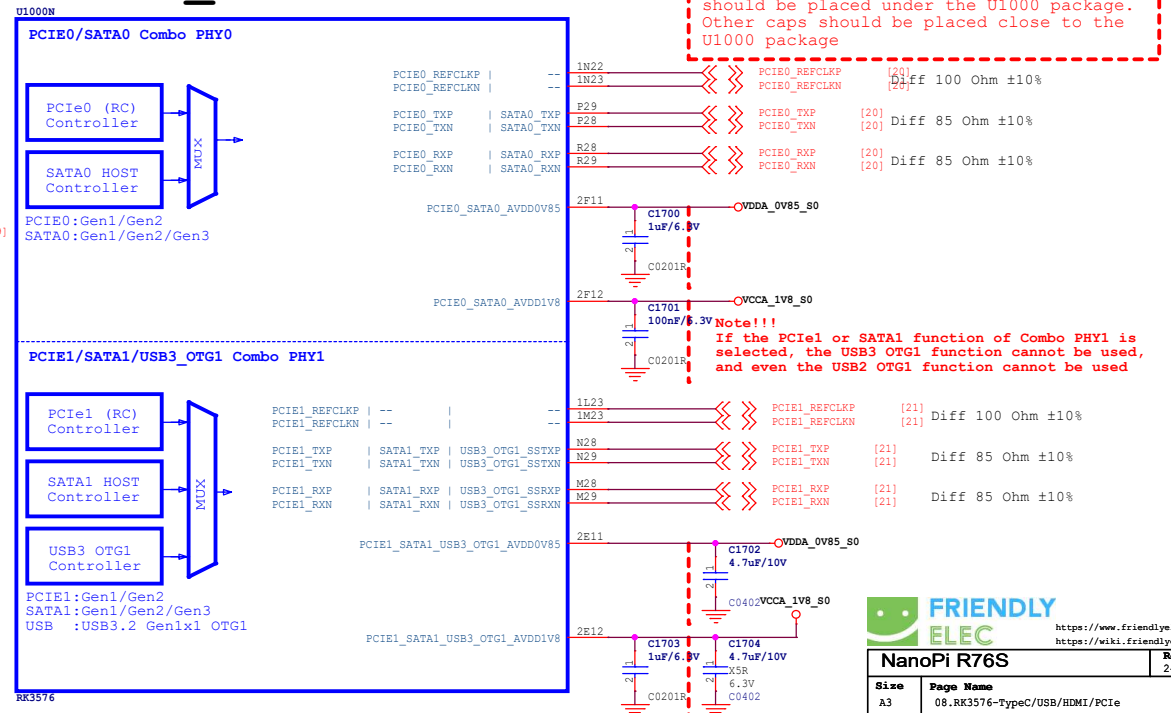
Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

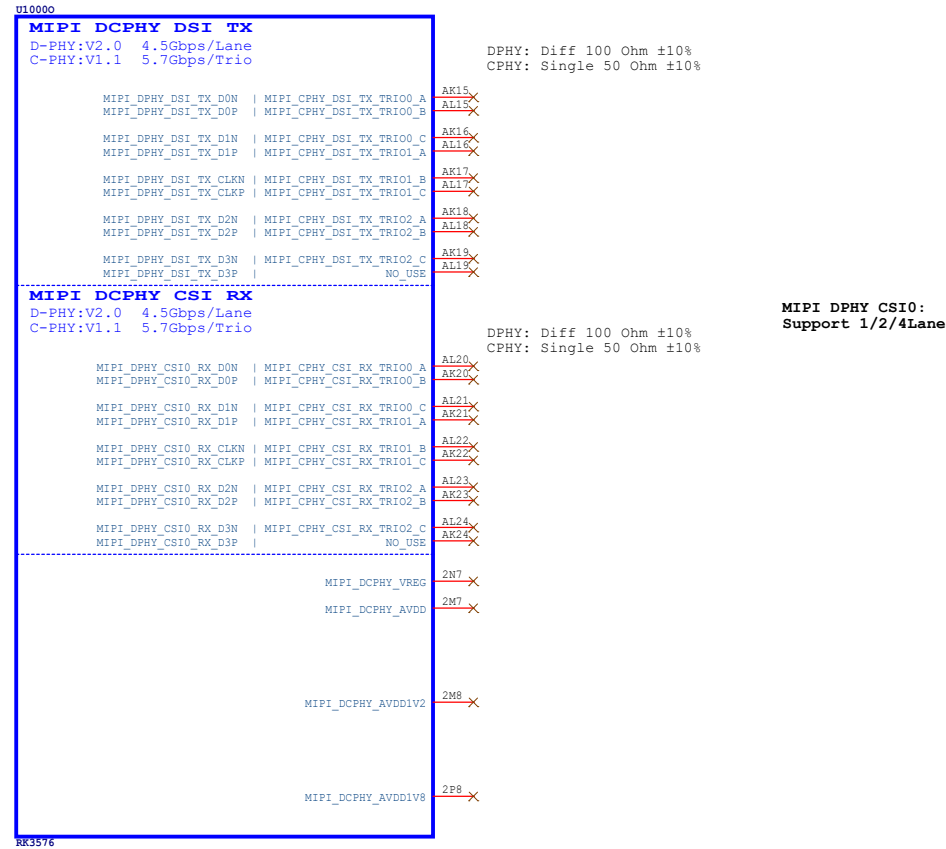
RK3576_M (USB2)



RK3576_N (PCIe/SATA/USB3)



RK3576_O (MIPI DCPHY)

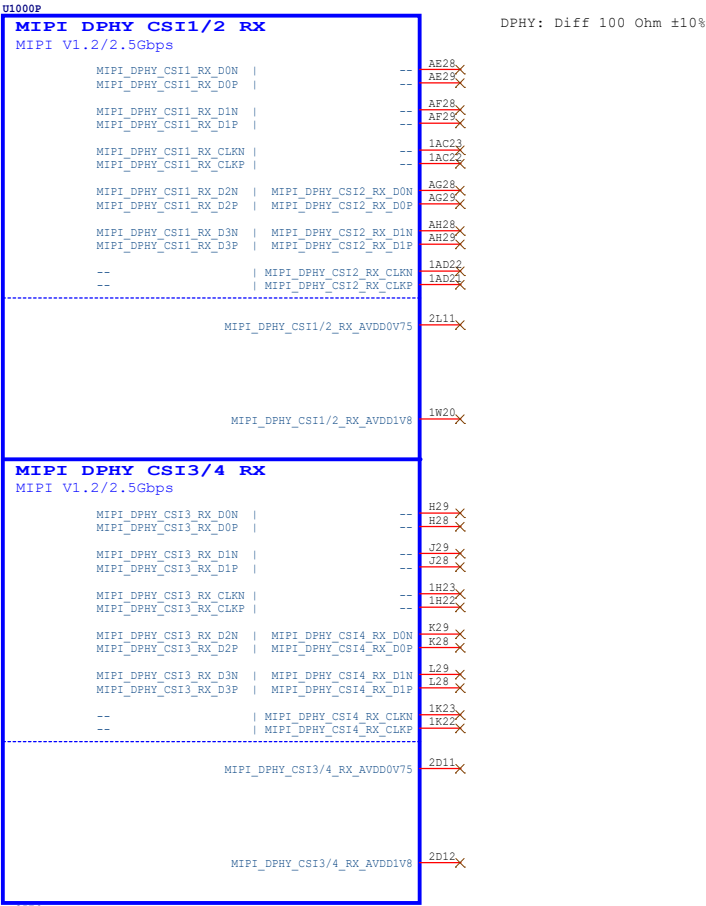


RK3576

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3576_P (MIPI DPHY CSI RX)

Support MIPI DPHY CSI1: 1/2/4Lane
Support MIPI DPHY CSI2: 1/2Lane
Support MIPI DPHY CSI3: 1/2/4Lane
Support MIPI DPHY CSI4: 1/2Lane
Support MIPI DPHY CSI1 2Lane + MIPI DPHY CSI2 2Lane

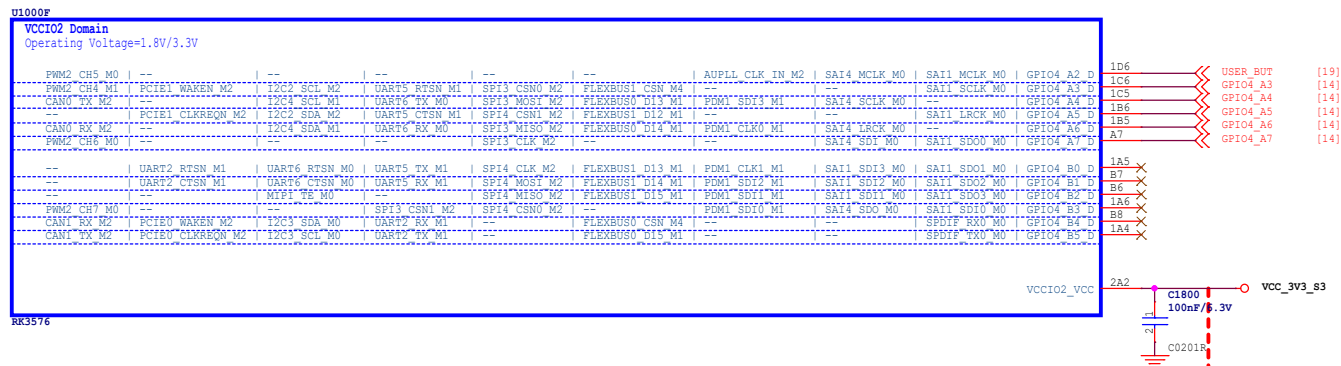


RK3576

Support MIPI DPHY CSI3: 1/2/4Lane
Support MIPI DPHY CSI4: 1/2Lane
Support MIPI DPHY CSI1 2Lane + MIPI DPHY CSI2 2Lane
Support MIPI DPHY CSI3 2Lane + MIPI DPHY CSI4 2Lane

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

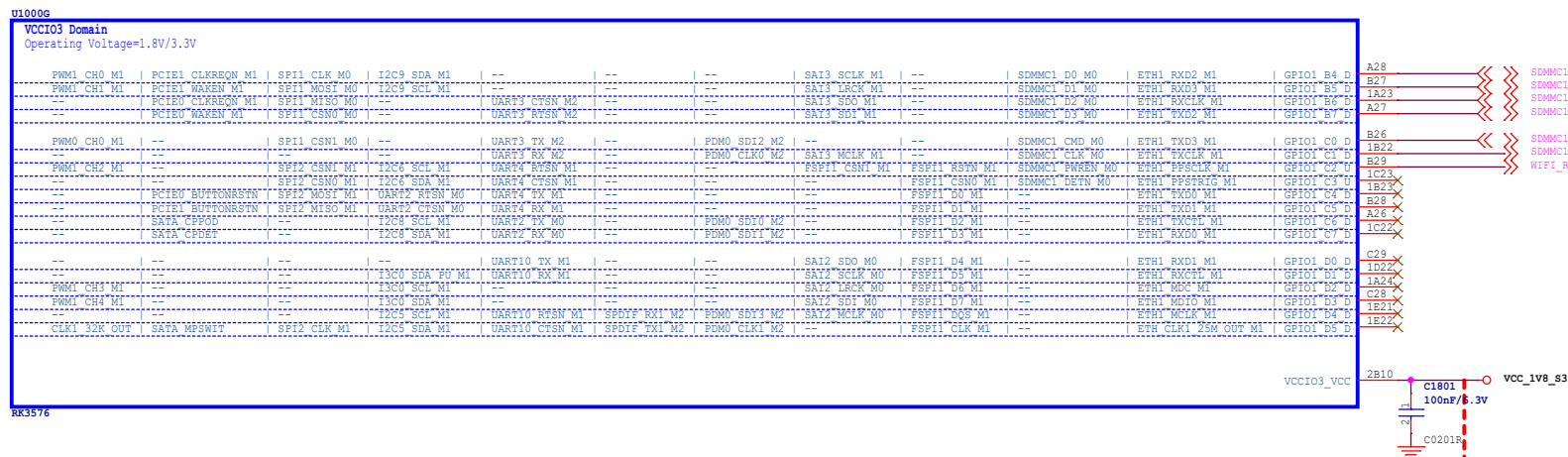
RK3576 F (VCCIO2)



Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

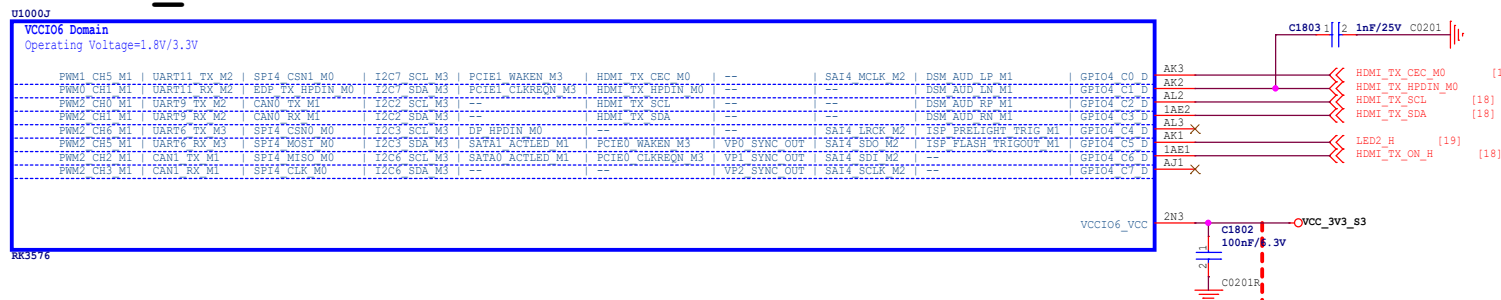
RK3576 G (VCCIO3)



Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576 J (VCCIO6)



Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_H (VCCIO4)

U1000H

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

--	--	I2C4_SCL_M2	SPI4_CSN1_M3	UART8_TX_M1	--	SA10_SDO0_M0	ETH0_RXD0_M1	SDMMC1_D0_M1	VI_CIF_D15	GPIO2_A6_D	B22
--	--	I2C4_SDA_M2	--	UART8_RX_M1	--	SA10_SSD1_M0	ETH0_TXD1_M1	SDMMC1_D1_M1	VI_CIF_D14	GPIO2_A7_D	B20
--	--	--	--	UART1_TX_M1	PD00_SDI3_M3	SA10_SDI0_M0	ETH0_TXD1_M1	SDMMC1_D2_M1	VI_CIF_D13	GPIO2_B0_D	B19
--	--	--	--	UART1_RX_M1	PD00_SDI2_M3	SA10_SDI1_M0	ETH0_RXD0_M1	SDMMC1_D3_M1	VI_CIF_D12	GPIO2_B1_D	I1A18
--	--	PCIE0_CLKREQ0_M0	SPI4_CSN0_M3	UART1_CSN_M1	PD00_SDI1_M3	SA10_SDI2_M0	ETH0_RXD1_M1	SDMMC1_D4_M1	VI_CIF_D11	GPIO2_B2_D	I1A18
--	--	PCIE1_CLKREQ0_M0	SPI4_CLK_M3	UART1_RTSN_M1	PD00_CLK1_M3	SA10_SDI0_M0	ETH0_TXD1_M1	SDMMC1_CLK_M1	VI_CIF_D10	GPIO2_B3_D	I1B18
--	--	SATA0_ACTL0_M0	SPI4_MOST_M3	UART1_CSN_M0	PD00_SDI0_M3	SA10_SDI1_M0	ETH0_RXD2_M1	SDMMC1_PAREN_M1	VI_CIF_D9	GPIO2_B4_D	A19
--	--	SATA1_ACTL0_M0	SPI4_MISO_M3	UART1_RTSN_M0	PD00_CLK0_M0	SA10_MCLK_M0	ETH0_TXD2_M1	SDMMC1_D5_M1	VI_CIF_D8	GPIO2_B5_D	I1C18
--	--	I2C6_SCL_M2	UART8_RTSN_M1	UART7_RX_M0	--	SA10_SDI2_M0	ETH0_RXD3_M1	ETH1_PTP_REFCLK_M0	VI_CIF_D7	GPIO2_B6_D	A21
--	--	I2C6_SDA_M2	UART8_CSN_M1	UART7_RX_M0	--	SA10_LCK0_M0	ETH0_RXD2_M1	--	VI_CIF_D6	GPIO2_B7_D	B21
PWM1_CH0_M2	--	--	--	UART9_RX_M0	PD01_SDI1_M0	--	ETH0_PTP_REFCLK_M1	ETH1_RXD2_M0	VI_CIF_D5	GPIO2_C0_D	A17
PWM1_CH1_M2	--	--	--	SPI1_CSN1_M1	UART9_TX_M0	PD01_CLK1_M0	ETH0_PPSCLK_M1	ETH1_RXD3_M0	VI_CIF_D4	GPIO2_C1_D	I1A18
PWM1_CH2_M2	--	--	--	SPI1_MOST_M1	UART11_CSN_M1	PD01_SDI2_M0	SA12_SCLK_M1	ETH0_PPSRGT_M1	ETH1_RXCLK_M0	VI_CIF_D3	I1D18
PWM1_CH3_M2	--	--	--	SPI1_MISO_M1	UART11_RTSN_M1	PD01_SDI3_M0	SA12_LCK0_M1	ETH1_RXD2_M0	VI_CIF_D2	GPIO2_C2_D	A15
PWM1_CH4_M2	--	--	--	SPI1_CSN0_M1	UART11_RX_M1	PD01_SDI0_M0	SA12_SSD1_M1	ETH1_RXD3_M0	VI_CIF_D1	GPIO2_C3_D	I1A18
PWM1_CH5_M2	--	--	--	SPI1_CLK_M1	UART11_RX_M1	PD01_CLK0_M0	SA12_SDI1_M1	ETH1_TXCLK_M0	VI_CIF_D0	GPIO2_C4_D	I1C18
PWM1_CH6_M2	--	--	--	I2C5_SCL_M2	--	--	SA14_SCL0_M3	ETH1_RXD0_M0	--	GPIO2_C5_D	I1A18
PWM1_CH7_M2	--	--	--	I2C5_SDA_M2	--	--	SA14_LCK0_M3	ETH1_TXD1_M0	--	GPIO2_C6_D	B15
PWM2_CH0_M2	--	--	--	I2C6_SCL_M2	--	--	SA14_SDI3_M3	ETH1_TXCLK_M0	--	GPIO2_D0_D	B16
PWM2_CH1_M2	--	--	--	I2C6_SDA_M2	--	--	SA14_SSD1_M3	ETH1_RXD0_M0	--	GPIO2_D1_D	I1A18
PWM2_CH2_M2	--	--	--	I3C1_SCL_M0	--	--	SA14_MCLK_M3	ETH1_RXD1_M0	--	GPIO2_D2_D	B17
PWM2_CH3_M2	--	--	--	I3C1_SDA_M0	--	--	--	ETH1_RXD2_M0	--	GPIO2_D3_D	B18
PWM2_CH4_M2	--	--	--	I2C9_SDA_M2	--	--	--	ETH1_MDC_M0	--	GPIO2_D4_D	I1B18
PWM2_CH5_M2	--	--	--	I2C9_SCL_M2	--	--	--	ETH1_MDIO_M0	--	GPIO2_D5_D	I1B18
PWM2_CH6_M2	--	--	--	I3C1_SDA_PU_M0	--	--	--	ETH1_CLK0_25M_OUT_M0	--	GPIO2_D6_D	I1D18
PWM2_CH7_M2	--	--	--	SPI3_CSN1_M0	UART9_CSN_M0	SPI01_RX0_M2	SA11_MCLK_M2	ETH0_RXD0_M1	--	GPIO2_D7_D	I1E18
--	--	--	--	SPI3_CLK_M0	UART3_TX_M0	--	SA13_SCL0_M2	ETH0_MDIO_M1	--	GPIO3_A0_D	I1D18
--	--	--	--	SPI3_MOST_M0	UART3_RX_M0	--	SA13_LCK0_M2	ETH0_MDC_M1	--	GPIO3_A1_D	I1B18
--	--	--	--	SPI3_MISO_M0	UART3_CSN_M0	SPI01_RX1_M1	SA13_SSD1_M2	ETH0_RXD1_M1	--	GPIO3_A2_D	I1A18
--	--	--	--	SPI3_CSN0_M0	UART3_RTSN_M0	SPI01_RX1_M1	SA13_SDI1_M2	ETH0_RXD2_M1	--	GPIO3_A3_D	I1A18

VCCIO4_VCC

C1900

100nF/6.3V 1uF/6.3V

C1901

100nF/6.3V 1uF/6.3V

C2019R

C20201R

VCC_3V3_S3

Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3576_I (VCCIO5)

U1000I

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH0_M3	--	SPI2_CLK_M2	UART1_CSN_M2	FLEXBUS0_CSN_M0	--	FLEXBUS1_D11	DSMC_RDYN	SA14_SDI1_M1	ETH_CLK0_25M_OUT_M0	VO_EBC_SDO0H	VO_LCDC_D23	GPIO3_A4_D	I013	
PWM1_CH1_M3	--	SPI2_CSN0_M2	UART1_RTSN_M2	--	--	FLEXBUS1_D10	DSMC_DATA13	SA14_SDI2_M1	ETH_MDIO_M0	VO_EBC_SDO0L	VO_LCDC_D22	GPIO3_A5_D	A9	
PWM1_CH2_M3	--	UART10_CSN_M0	UART1_RX_M2	--	--	FLEXBUS1_D9	DSMC_DATA13	SA14_SDI3_M1	ETH_RXD0_M0	VO_EBC_SDO0L	VO_LCDC_D21	GPIO3_A6_D	I1A7	
PWM1_CH3_M3	--	UART10_RTSN_M0	UART1_TX_M2	--	--	FLEXBUS1_D8	DSMC_DATA13	SA14_SDI4_M1	ETH_RXD1_M0	VO_EBC_SDO0L	VO_LCDC_D20	GPIO3_A7_D	B13	
PWM2_CH0_M3	--	SPI2_MOST_M2	UART10_RX_M0	--	--	FLEXBUS1_D7	DSMC_CSN1	SA14_MCLK_M1	ETH0_MCLK_M0	VO_EBC_SDO0L	VO_LCDC_D19	GPIO3_B0_D	B14	
PWM2_CH1_M3	--	SPI2_CSN0_M1	UART10_TX_M0	--	--	FLEXBUS1_D6	DSMC_DATA12	SA14_MCLK_M1	ETH0_RXD1_M0	VO_EBC_SDO0L	VO_LCDC_D18	GPIO3_B1_D	I1A11	
PWM2_CH2_M3	--	I2C9_SDA_M3	UART9_RX_M0	--	--	FLEXBUS1_D5	DSMC_DATA11	SA14_SDI0_M1	ETH0_TXD1_M0	VO_EBC_SDO0L	VO_LCDC_D17	GPIO3_B2_D	A13	
PWM2_CH3_M3	--	I2C9_SCL_M3	UART9_TX_M0	--	--	FLEXBUS1_D4	DSMC_DATA11	SA14_SDI1_M1	ETH0_TXD2_M0	VO_EBC_SDO0L	VO_LCDC_D16	GPIO3_B3_D	A11	
PWM1_CH4_M3	--	--	UART9_RTSN_M1	--	--	FLEXBUS1_D3	DSMC_DATA10	SPI01_RX1_M0	ETH0_RXD1_M0	VO_EBC_SDO0L	VO_LCDC_D15	GPIO3_B4_D	B10	
PWM1_CH5_M3	--	--	UART9_CSN_M1	--	--	FLEXBUS1_D2	DSMC_DATA10	SPI01_RX1_M0	ETH0_RXD2_M0	VO_EBC_SDO0L	VO_LCDC_D14	GPIO3_B5_D	I1A9	
PWM1_CH6_M3	--	--	SPI3_CSN0_M1	--	--	FLEXBUS1_D1	DSMC_DATA10	SPI01_RX1_M0	ETH0_TXCLK_M0	VO_EBC_SDO0L	VO_LCDC_D13	GPIO3_B6_D	I1D12	
PWM2_CH7_M3	--	I2C4_SDA_M3	UART9_CSN_M1	FLEXBUS1_CSN_M0	--	FLEXBUS1_D0	DSMC_DQ00	SA11_SDI1_M1	ETH0_PPSRGT_M0	VO_EBC_SDO0L	VO_LCDC_D12	GPIO3_B7_D	I1D12	
--	--	I2C4_SCL_M3	UART3_RTSN_M1	UART2_TX_M2	--	--	FLEXBUS1_D9	DSMC_DATA7	SA11_SDI0_M1	ETH0_PPSCLK_M0	VO_EBC_SDO0L	VO_LCDC_D11	GPIO3_C0_D	I1E9
CAND_RX_M3	--	I2C9_SDA_M3	SPI2_MISO_M2	UART11_RTSN_M0	--	--	FLEXBUS1_D8	DSMC_DATA6	SA11_SDI1_M1	ETH0_PTP_REFCLK_M0	VO_EBC_SDO0L	VO_LCDC_D10	GPIO3_C1_D	I1B10
PWM2_CH0_M3	--	I2C9_SCL_M3	SPI4_MISO_M1	UART11_RTSN_M0	--	--	FLEXBUS1_D7	DSMC_DATA6	SA11_SDI2_M1	ETH0_RXD1_M0	VO_EBC_SDO0L	VO_LCDC_D9	GPIO3_C2_D	B9
PWM2_CH1_M3	--	I2C9_SDA_M3	SPI4_MOST_M1	UART11_CSN_M0	FLEXBUS0_CSN_M2	--	FLEXBUS1_D6	DSMC_DATA6	SA11_SDI3_M1	ETH0_RXD2_M0	VO_EBC_SDO0L	VO_LCDC_D8	GPIO3_C3_D	I1D9
CAND_TX_M3	--	I2C5_SCL_M3	SPI2_CSN0_M2	UART11_TX_M0	--	--	FLEXBUS1_D5	DSMC_DATA5	SA11_SDI0_M1	--	VO_EBC_SDO0L	VO_LCDC_D7	GPIO3_C4_D	I1B9
PWM2_CH2_M3	--	--	SPI1_MISO_M2	UART9_RX_M0	--	--	FLEXBUS1_D4	DSMC_DATA4	SA11_SDI1_M1	--	VO_EBC_SDO0L	VO_LCDC_D6	GPIO3_C5_D	I1D7
--	--	--	SPI1_MOST_M2	UART9_TX_M0	--	--	FLEXBUS1_D3	DSMC_DATA4	SA11_SDI2_M1	--	VO_EBC_SDO0L	VO_LCDC_D5	GPIO3_C6_D	I1C7
--	--	--	SPI1_CLK_M2	UART9_RTSN_M0	--	--	FLEXBUS1_D2	DSMC_DATA4	SA11_SDI3_M1	--	VO_EBC_SDO0L	VO_LCDC_D4	GPIO3_C7_D	I1C7
PWM2_CH3_M3	--	--	SPI3_CSN0_M2	UART8_CSN_M0	--	--	FLEXBUS1_D1	DSMC_DATA1	SA11_MCLK_M1	--	VO_EBC_SDO0L	VO_LCDC_D3	GPIO3_D0_D	I1C12
--	--	--	SPI4_CLK_M1	--	FLEXBUS1_CSN_M2	--	FLEXBUS1_D0	DSMC_CSN2	SA12_MCLK_M2	ETH0_PPSCLK_M0	VO_EBC_SDO0L	VO_LCDC_D2	GPIO3_D1_D	I1A10
PWM2_CH4_M3	--	I3C1_SCL_M2	SPI4_CSN1_M1	UART2_RTSN_M2	FLEXBUS0_CSN_M3	FLEXBUS1_D15_M0	FLEXBUS1_D12	DSMC_CSN3	SA12_SDI1_M2	ETH0_RXD3_M0	VO_EBC_SDO0L	VO_LCDC_D1	GPIO3_D2_D	B12
PWM2_CH5_M3	--	I3C1_SDA_M2	SPI4_MISO_M1	UART2_CSN_M2	--	--	FLEXBUS1_D11	DSMC_CSN0	SA12_SDI2_M2	ETH0_RXD2_M0	VO_EBC_SDO0L	VO_LCDC_D0	GPIO3_D3_D	I1E12
--	--	--	SPI3_CLK_M1	UART9_RX_M0	--	--	FLEXBUS1_D10	DSMC_CSN0	SA12_SDI3_M2	ETH0_RXD1_M0	VO_EBC_SDO0L	VO_LCDC_D0	GPIO3_D4_D	I1D12
--	--	--	SPI3_MISO_M1	UART9_TX_M0	--	--	FLEXBUS1_D9	DSMC_CSN0	SA12_SDI0_M2	ETH0_RXD2_M0	VO_EBC_SDO0L	VO_LCDC_D0	GPIO3_D5_D	I1D10
PWM2_CH6_M3	--	--	SPI3_CSN0_M1	UART9_CSN_M0	--	--	FLEXBUS1_D8	DSMC_CSN0	SA12_SDI1_M2	ETH0_RXD3_M0	VO_EBC_SDO0L	VO_LCDC_D0	GPIO3_D6_D	I1C10
PWM2_CH7_M3	--	--	SPI3_CSN0_M1	UART9_RTSN_M0	FLEXBUS1_CSN_M1	FLEXBUS1_D14_M0	FLEXBUS1_D11_M0	DSMC_ASSEN	SA14_SCL0_M1	CAM_CLK0_OUT_M0	VO_EBC_SDO0L	VO_LCDC_D0	GPIO3_D7_D	I1B7
MIPI_TE_M2	I2C7_SCL_M2	SPI1_CSN1_M2	UART3_TX_M1	FLEXBUS1_CSN_M3	FLEXBUS1_D14_M0	FLEXBUS0_D13_M0	DSMC_INT0	SA14_LCK0_M1	CAM_CLK1_OUT_M0	SPI01_RX0_M1	--	GPIO4_A0_D	I1B12	
I2C7_SDA_M2	--	--	UART3_RX_M0	FLEXBUS1_CSN_M3	FLEXBUS1_D14_M0	FLEXBUS0_D13_M0	DSMC_INT0	SA14_SDI0_M1	CAM_CLK1_OUT_M0	SPI01_RX0_M1	--	GPIO4_A0_D	I1B7	

VCCIO5_VCC_0

VCCIO5_VCC_1

C1902

100nF/6.3V 1uF/6.3V

C1903

100nF/6.3V 1uF/6.3V

C20201R

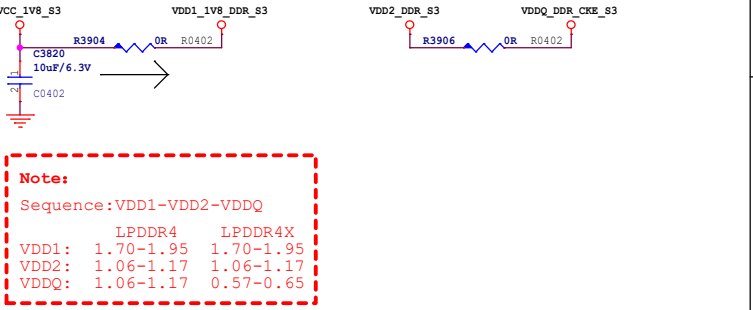
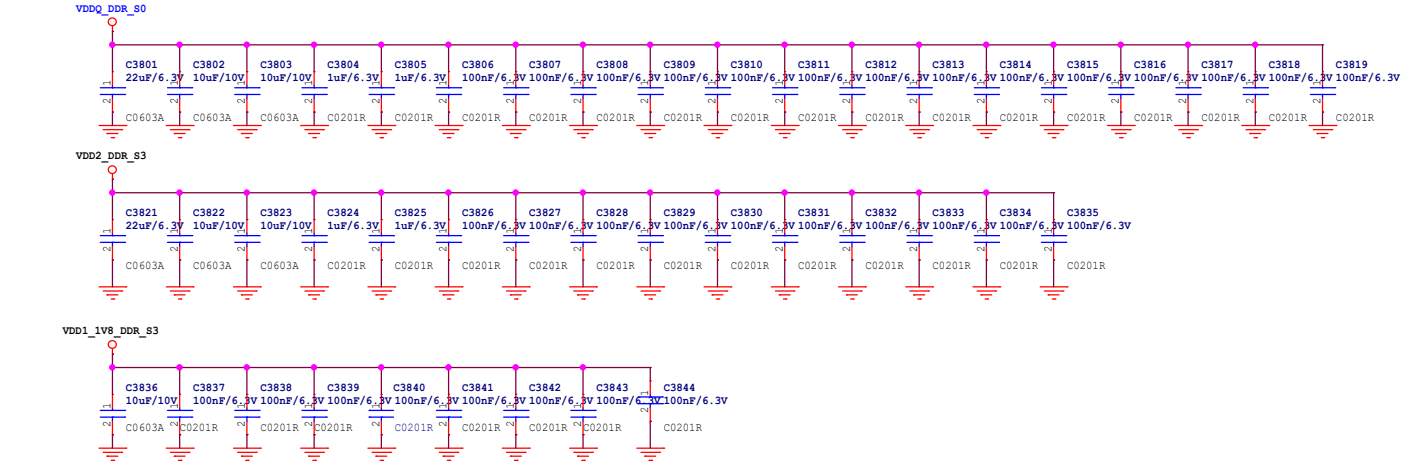
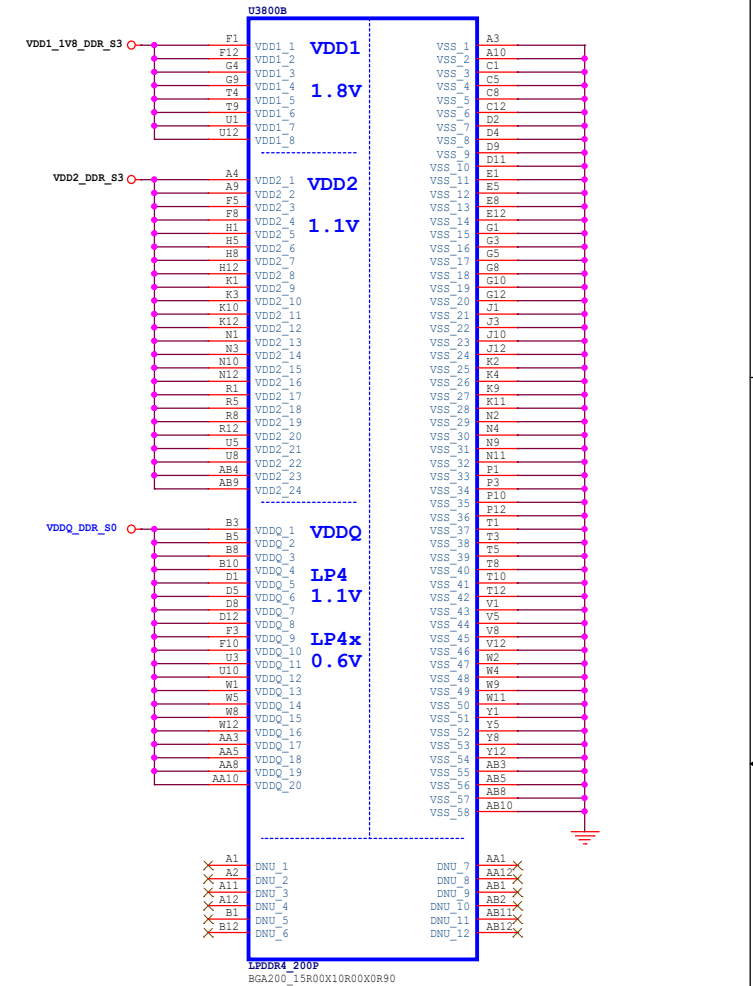
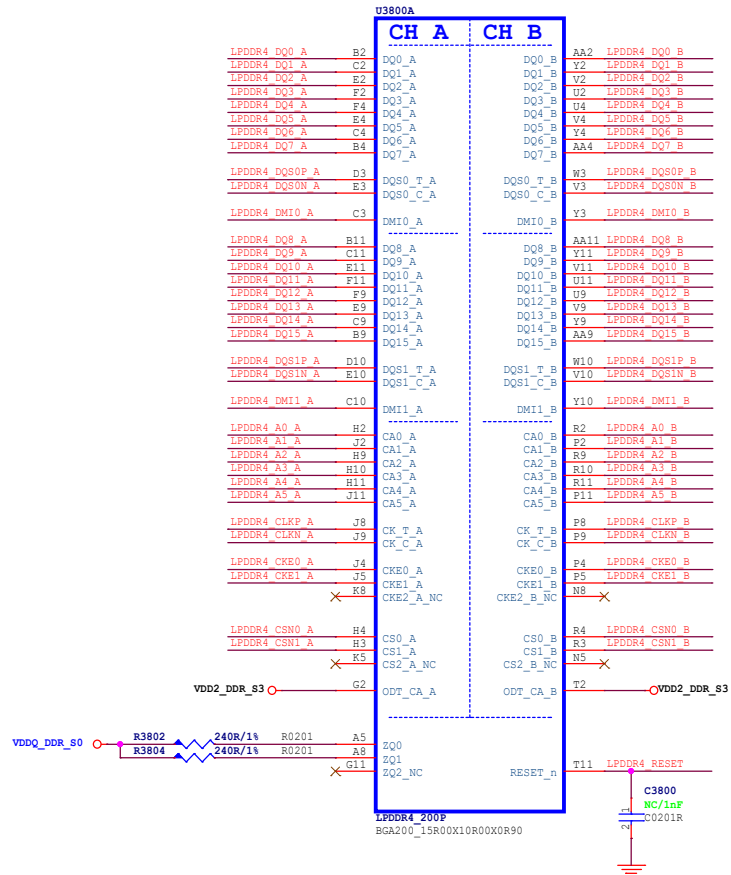
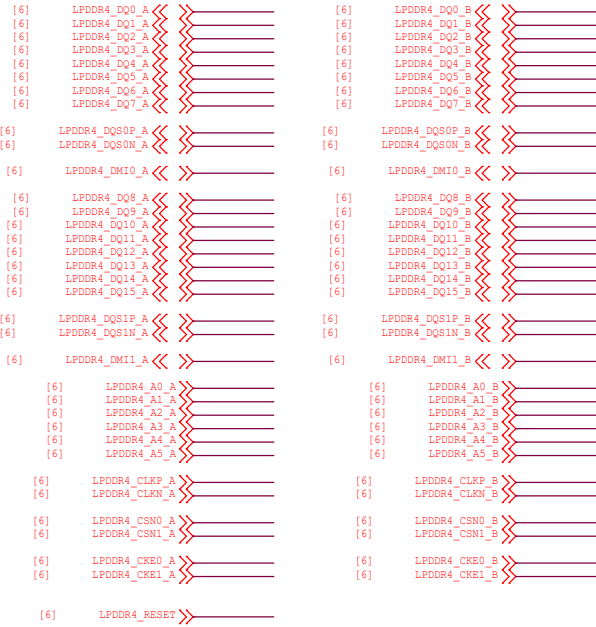
C20201R

VCC_1V8_S3

Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

LPDDR4X



Note:
Sequence: VDD1-VDD2-VDDQ

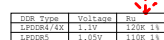
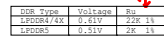
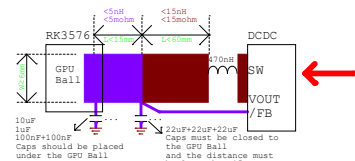
	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65

I2C1_SDA_M0_RK806 >>>
I2C1_SCL_M0_RK806 >>>

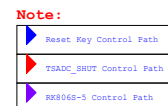
PMIC_PMR_CTRL1 >>>
PMIC_PMR_CTRL2 >>>

[5] PMIC_INT_L <<<
[5] RESET_L >>>

PMIC_EXT_EN_OUT <<<
[14,19] PMRGN_L >>>



Note:
I2C Mode:CS(pin18) connected to VCCA(pin21);
SPI Mode(Def):CS(pin18) floating or connected to GND



The schematic diagram illustrates the power supply section of the AD9289, featuring two main regulators: VCC2_VDDO and VCC3_VDDO. The VCC2_VDDO regulator is a buck converter with an input capacitor C2354 (1uF/6.3V) and an output capacitor C2359 (2uF/10V). The VCC3_VDDO regulator is a buck converter with an input capacitor C2364 (2uF/6.3V) and an output capacitor C2371 (1uF/6.3V). The diagram shows the internal structure of the regulators, including the power MOSFETs, diodes, and various control nodes. The output voltages are specified as 1.8V, 1.8V, 1.2V, 3.0V, 3.3V, 0.75V, 0.85V, 0.75V, 0.85V, and 0.75V. The diagram also includes a table of component values and their locations.

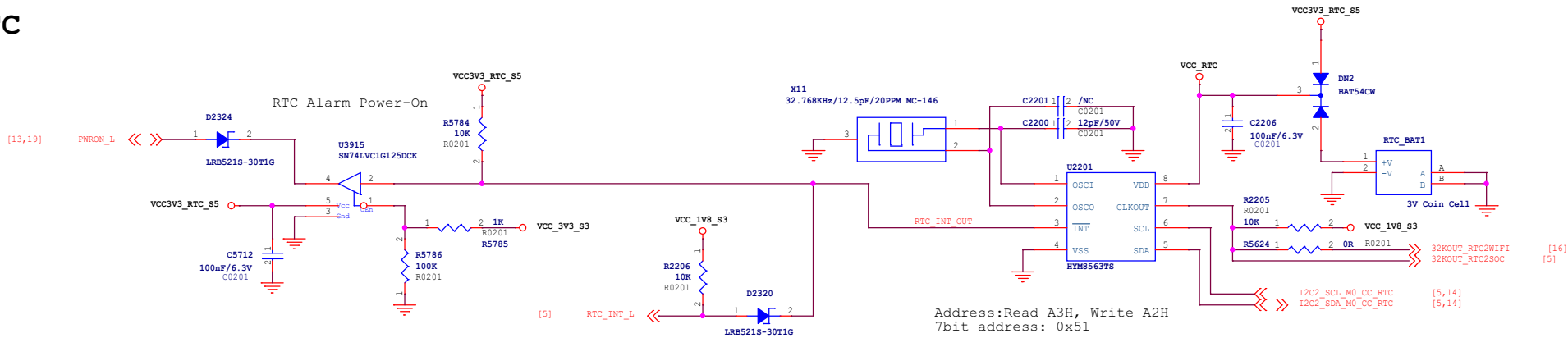
Component	Value	Location
C2354	1uF/6.3V	U2301
C2359	2uF/10V	U2302
C2364	2uF/6.3V	U2303
C2371	1uF/6.3V	U2304
R2354	0.5A	U2301
R2355	0.3A	U2301
R2356	0.3A	U2301
R2359	0.5A	U2302
R2364	0.3A	U2303
R2371	0.5A	U2304

Note:

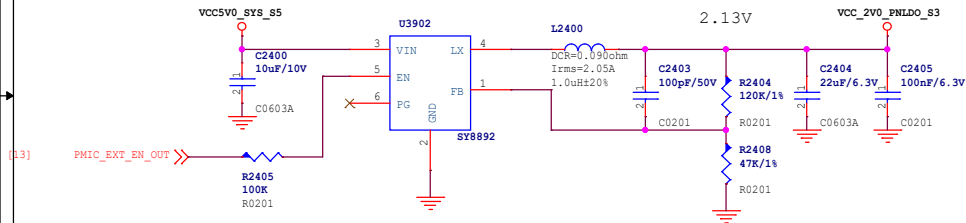
The RK806 LDO power distribution of the reference schematics is only suitable for the interface used in the reference schematics.

If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added

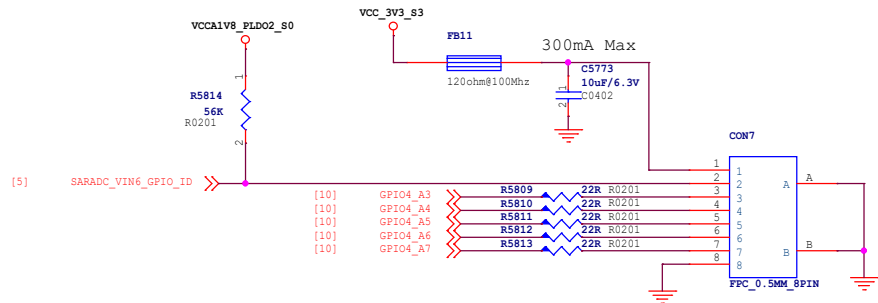
RTC



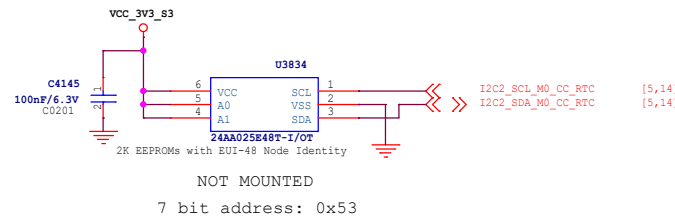
VCC_2V0_PLDO_NLDO_S3



GPIO



EUI-48 Node Identity



Config Table for GPIO				
Pin#	GPIO	SPI	I2C	UART
3	GPIO4_A3	SPI3_CSN0_M2		
4	GPIO4_A4	SPI3_MOSI_M2	I2C4_SCL_M1	UART6_TX_M0
5	GPIO4_A5			
6	GPIO4_A6	SPI3_MISO_M2	I2C4_SDA_M1	UART6_RX_M0
7	GPIO4_A7	SPI3_CLK_M2		

USB-C 5V IN

VCC5V0_SYS_S5

ED1

AZ5825-01F

Ipp=18A

Vpwm=5V

Vclamp=6.5V

Vbvw=6~9V

Vsurge_CL=6~9.5V

30pF

**IF TVS UNMOUNTED,
ESD OR SURGE SHOULD BE
DAMAGE THE PMIC!!!**

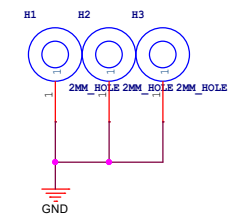
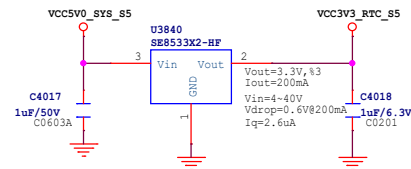
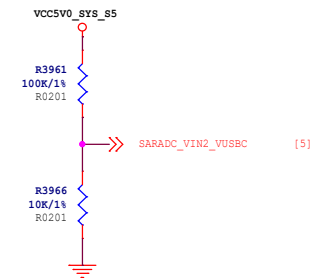
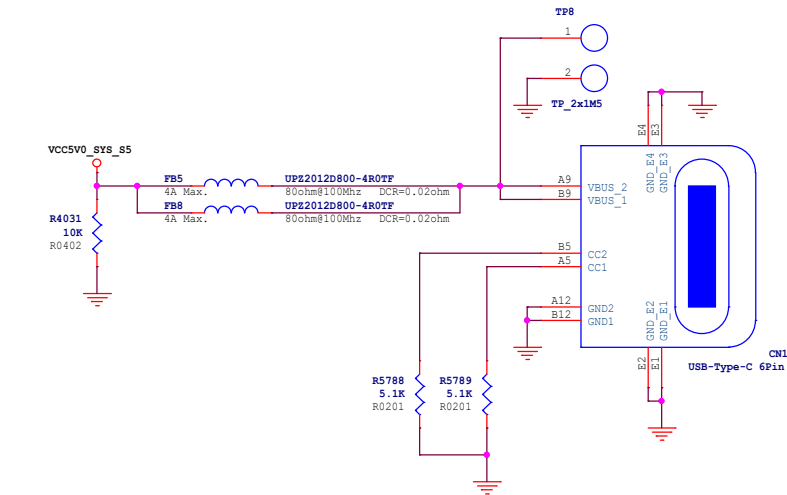
This device must be mounted. Replacing TVS mode is not recommended, if must, please choose the same specifications

Operating Supply Vltage : 5.5V(5.25-6V)

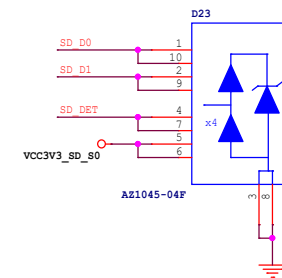
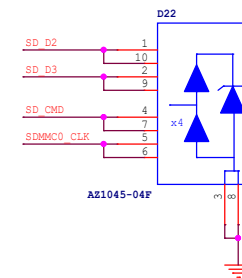
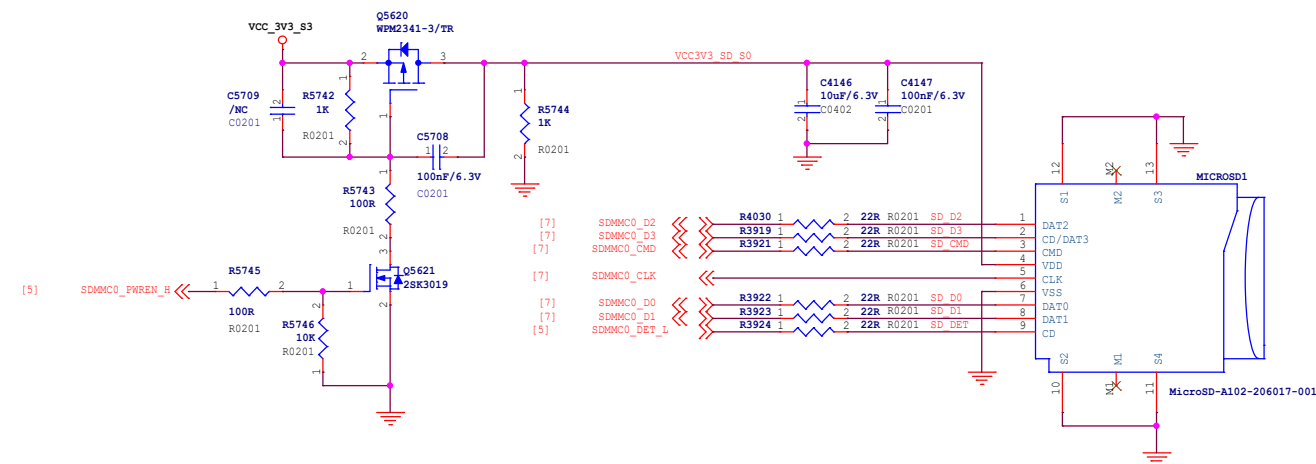
PeakPulse Current: >10A (tpe=8/20uS)

Surge Clamping Voltage: <6.5V

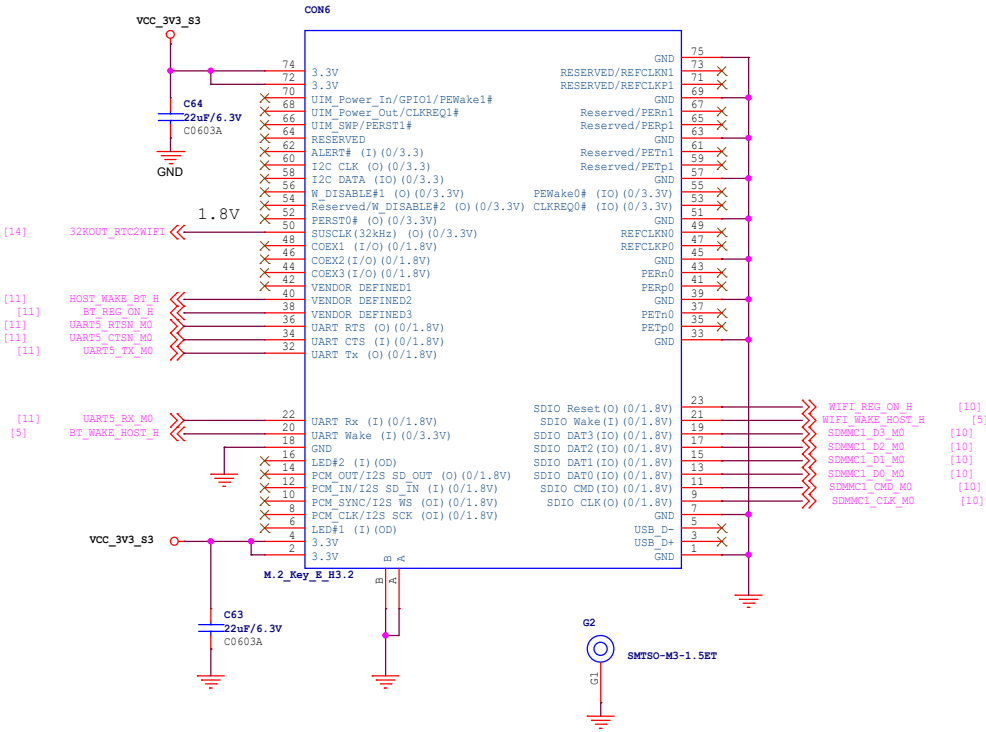
DO NOT DELETE IT!

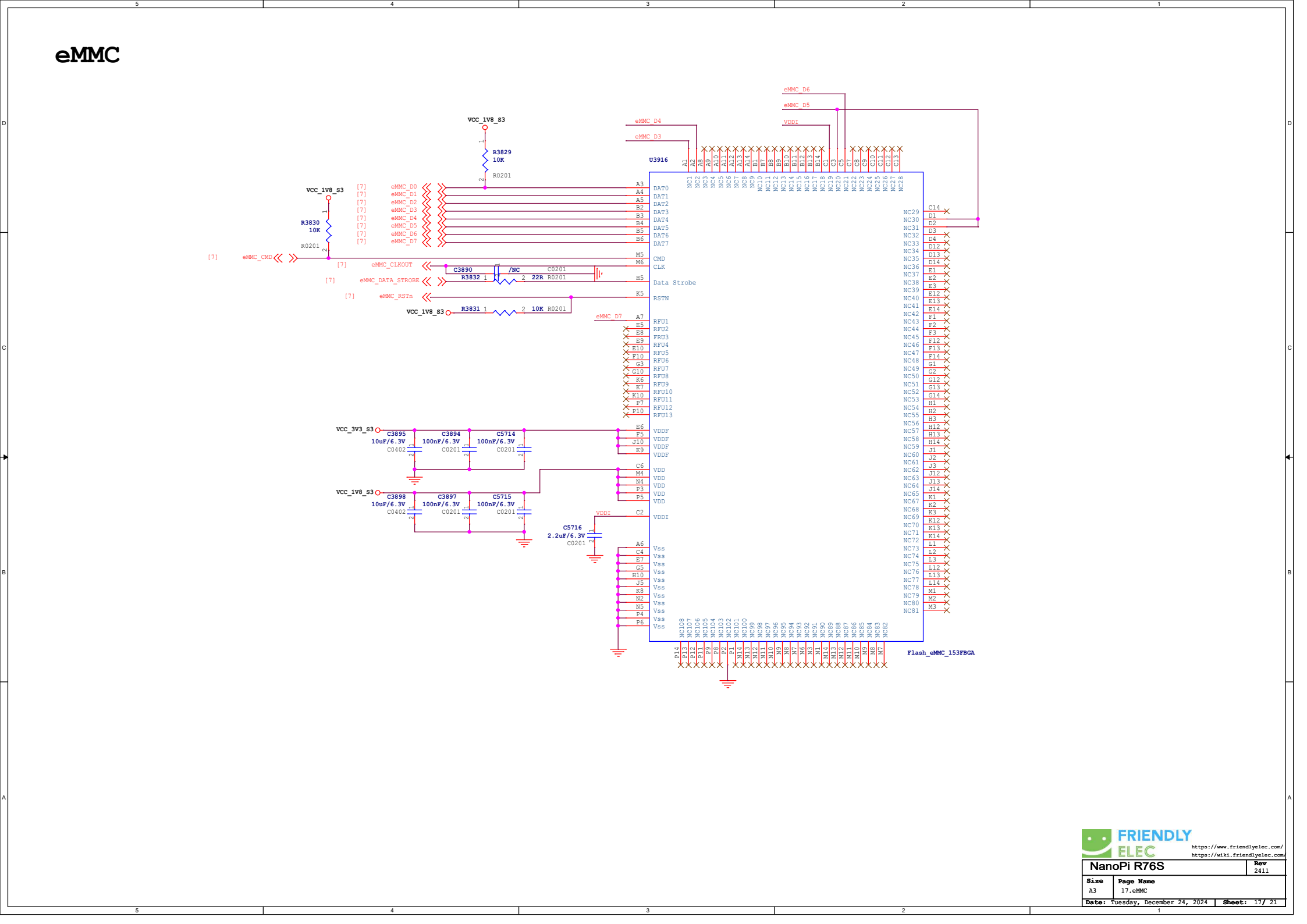


microSD

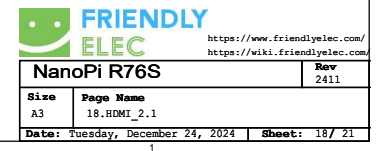
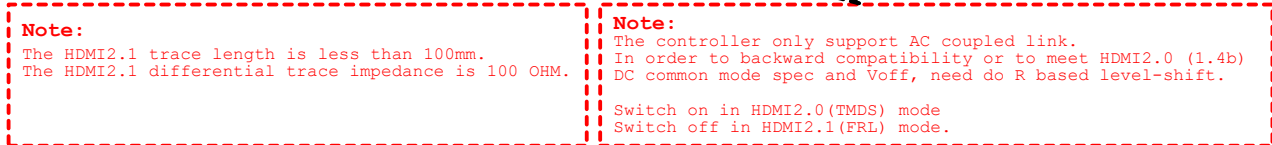


M.2 Key E 2230

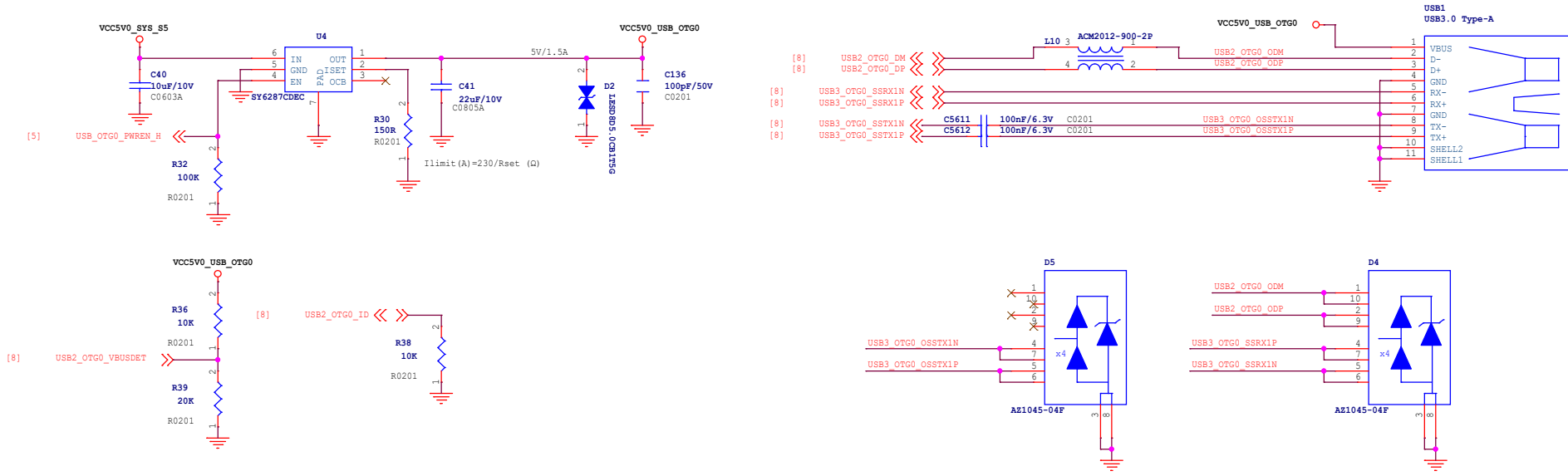




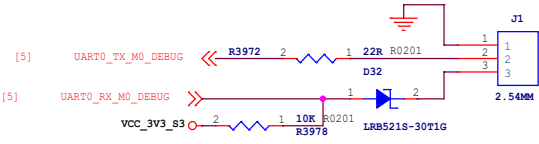
Support video output
up to 4Kx2K@120Hz



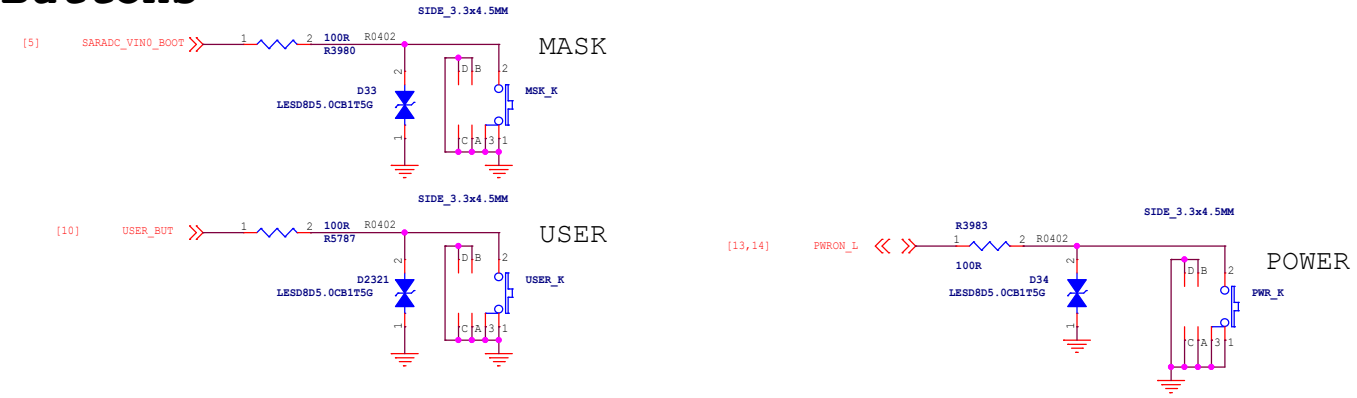
USB3.0



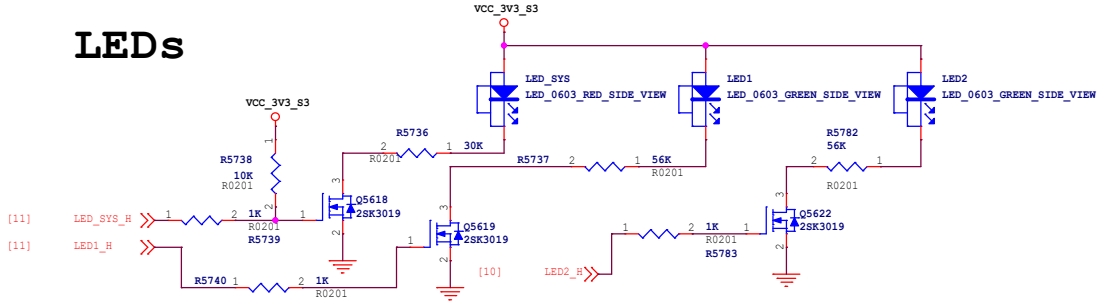
Debug UART



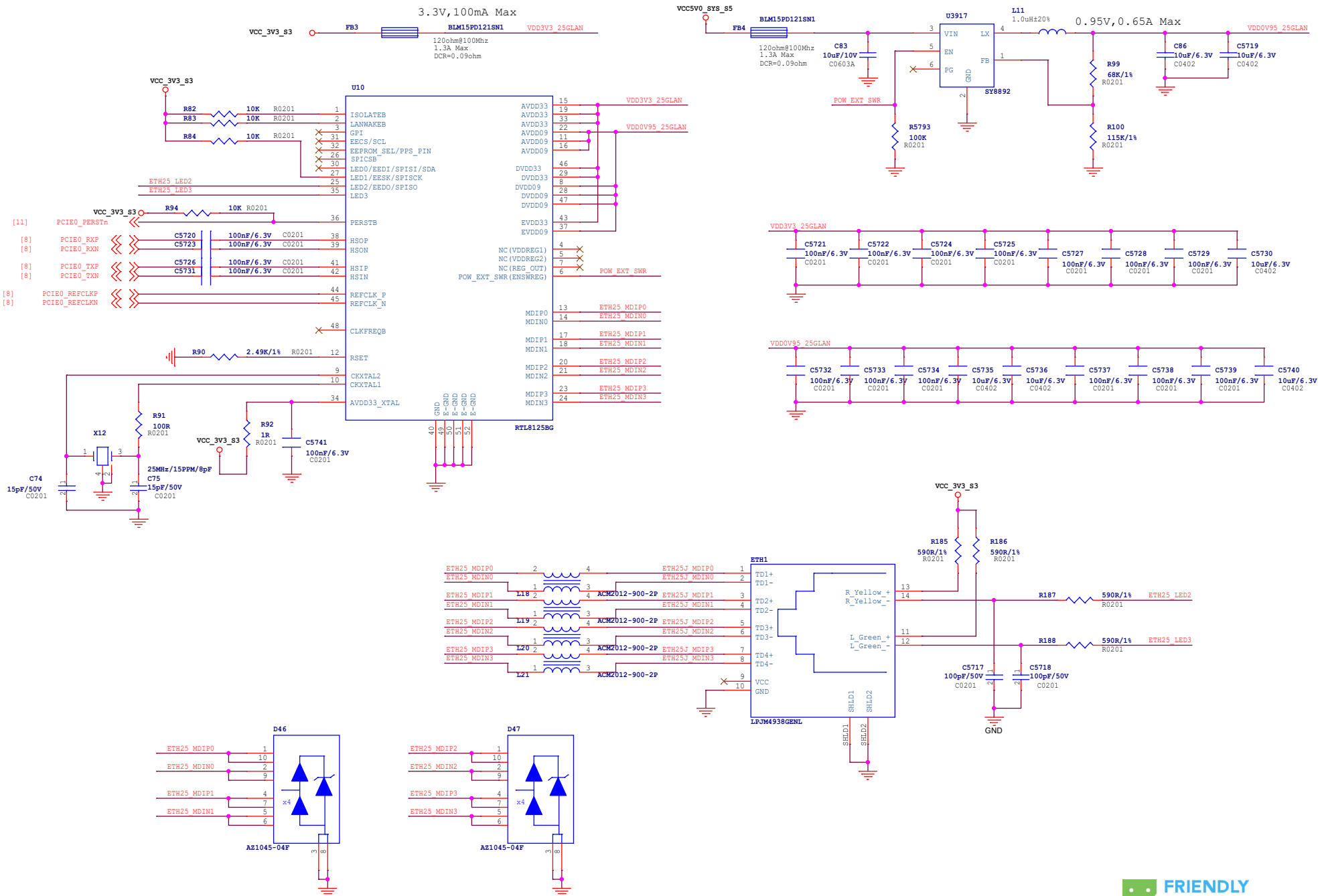
Buttons



LEDs



2.5G Ethernet A



2.5G Ethernet B

