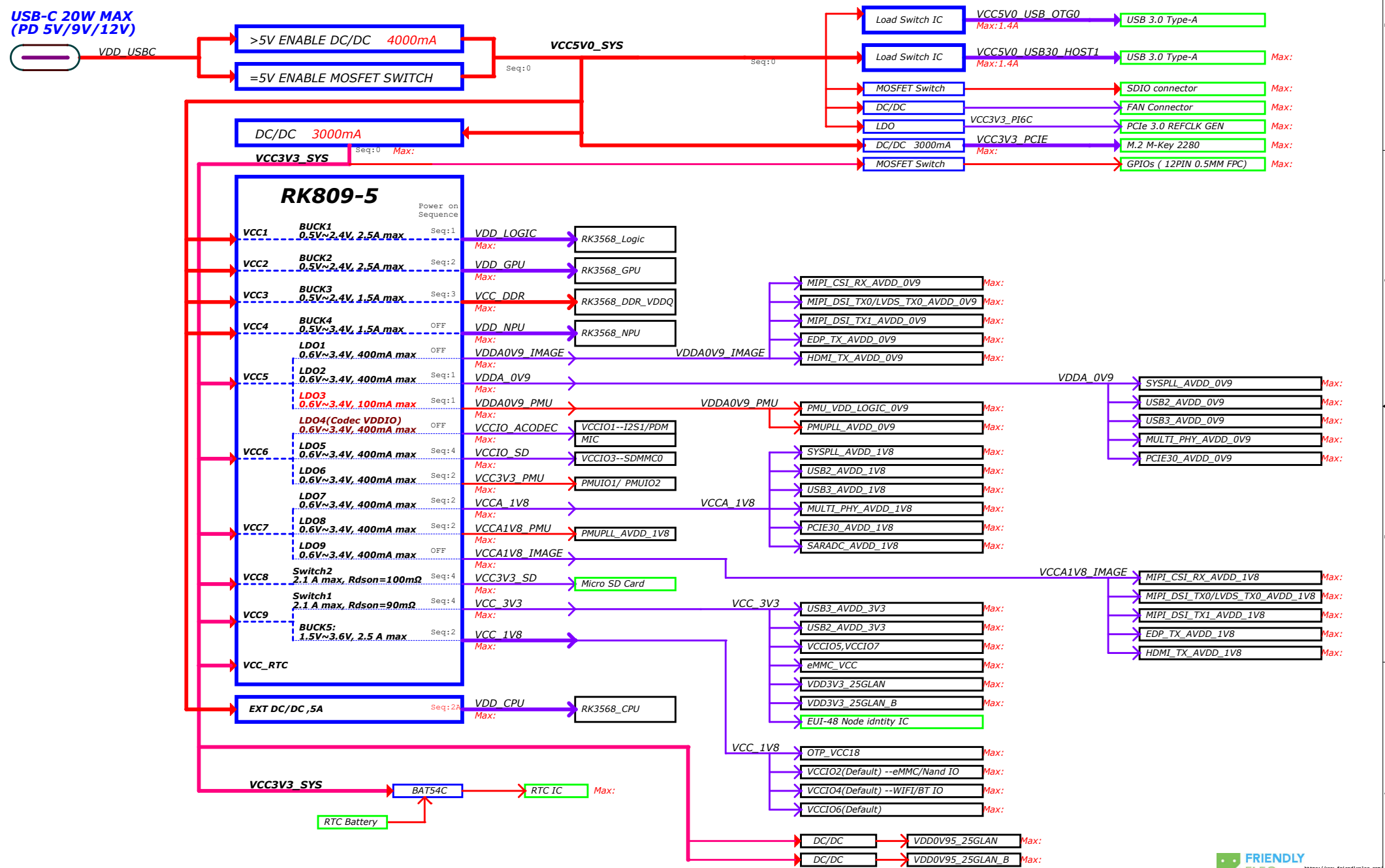
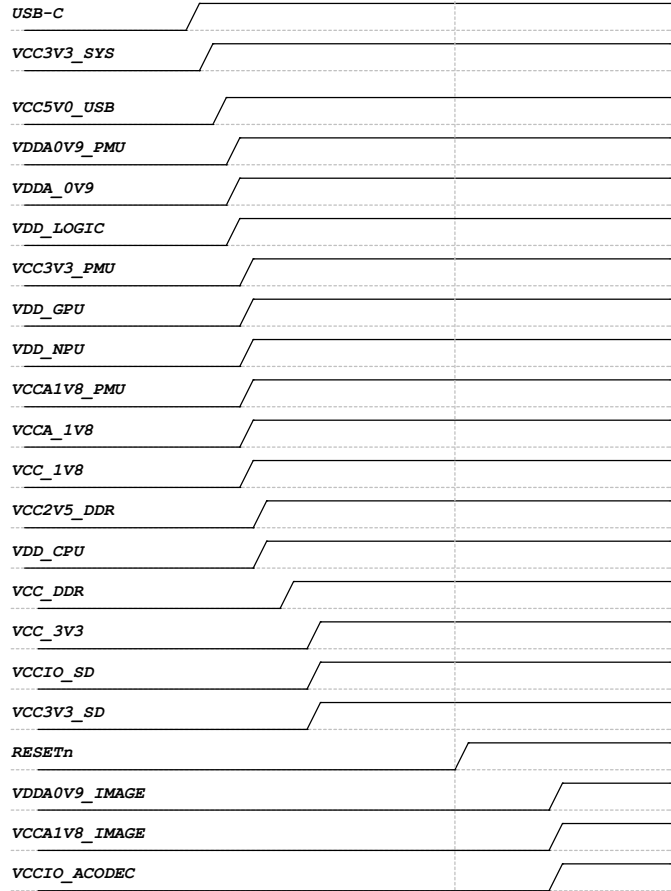


Power Diagram



Power Sequence



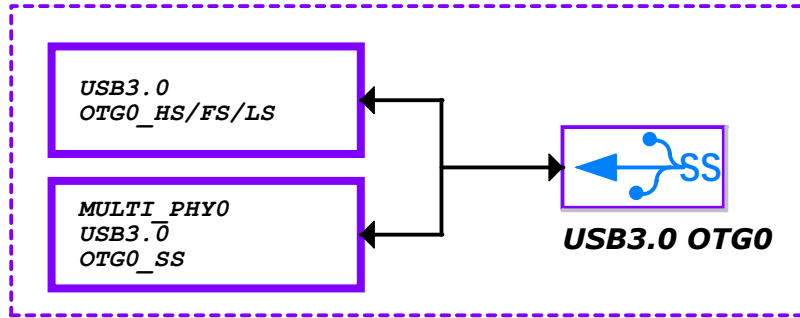
I2C5, 7bit address
- 0x51, HYM8563TS, RTC IC
- 0x53, 24AA025E48T, EUI-48 Node Identity

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0.9V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0.9V	OFF	OFF	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	3.3V	OFF	OFF	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	1.8V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW2	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
VCC3V3_SYS	100mohm RK809_SW1	2.1A	VCC_3V3	Slot:4	3.3V	ON	OFF	TBD	TBD
	90mohm RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_RESETn			Slot:4+5					
VDD_USBC	EXT BUCK	4.0A	VCC3V3_SYS	Slot:0	3.3V	ON	ON	TBD	TBD
VDD_USBC	EXT BUCK	4.0A	VCC3V3_SYSP	Slot:0	3.3V	ON	ON	TBD	TBD
VCC3V3_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF	TBD	TBD

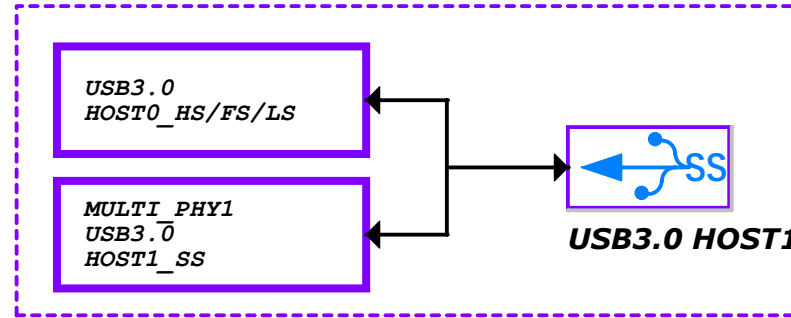
IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V, FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

USB3.0 OTG0



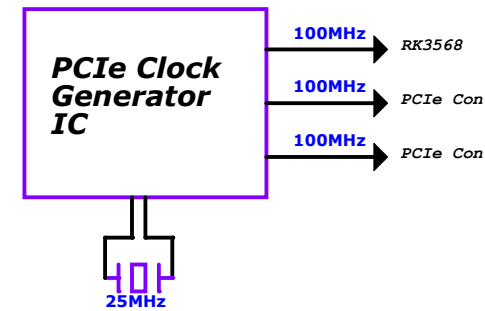
USB3.0 HOST1



PCIe3.0 PHY

Option1	PCIe3.0 x2Lane	PCIe30_REFCLK (RC/EP:input)	PCIe30_TX0 PCIe30_RX0 PCIe30_TX1 PCIe30_RX1	PCIe30X2_CLKREQn PCIe30X2_WAKEn PCIe30X2_PERSTn PCIe30X2_BUTTONRSTn	RC or EP
Option2	PCIe3.0 x1Lane + PCIe3.0 x1Lane	PCIe30_REFCLK (RC:input)	PCIe30_TX0 PCIe30_RX0	PCIe30X2_CLKREQn PCIe30X2_WAKEn PCIe30X2_PERSTn PCIe30X2_BUTTONRSTn	Only RC
			PCIe30_TX1 PCIe30_RX1	PCIe30X1_CLKREQn PCIe30X1_WAKEn PCIe30X1_PERSTn PCIe30X1_BUTTONRSTn	Only RC

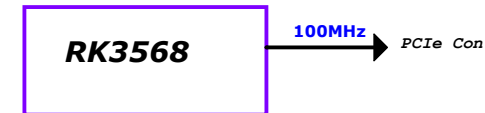
PCIe REFCLK



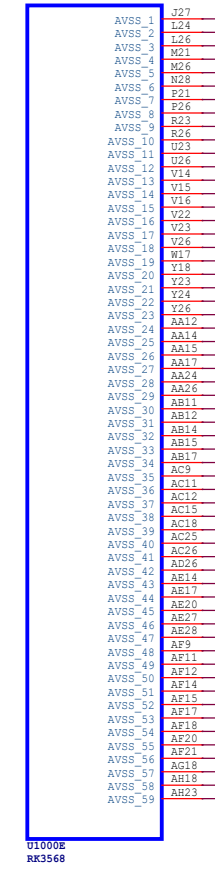
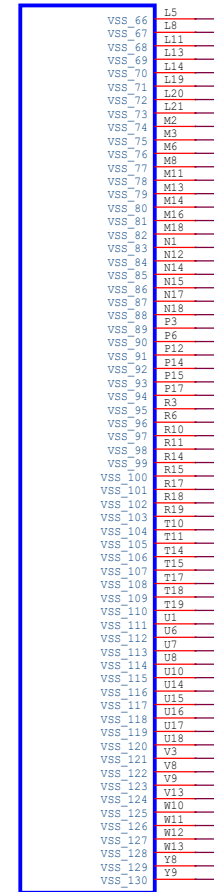
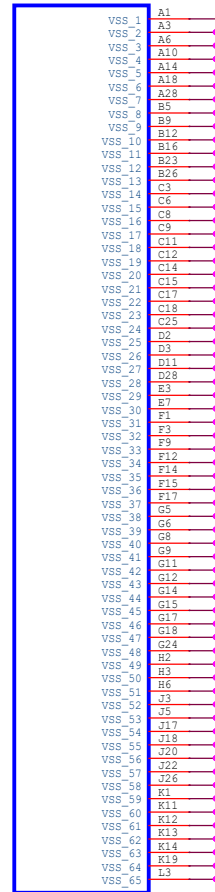
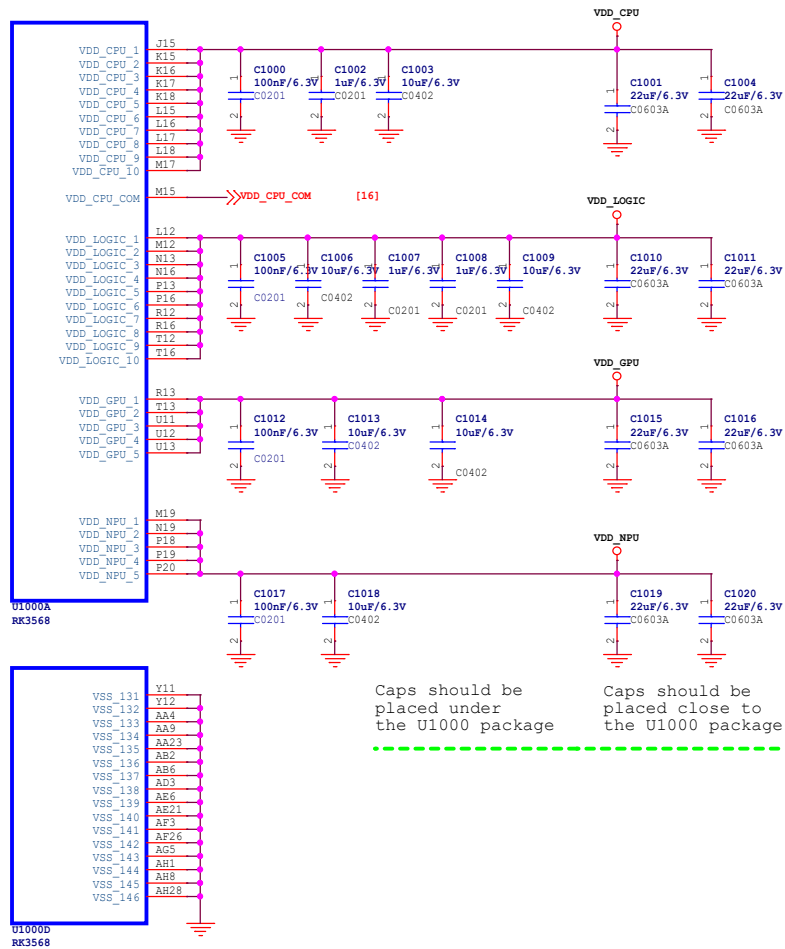
PCIe2.0 PHY

MULTI_PHY2	PCIe2.0 x1Lane	PCIe20_REFCLK (RC:output)	PCIe20_TX PCIe20_RX	PCIe20_CLKREQn PCIe20_WAKEn PCIe20_PERSTn PCIe20_BUTTONRSTn	Only RC
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PCIe2.0 REFCLK



RK3568_ABCDE (Power&Gnd)

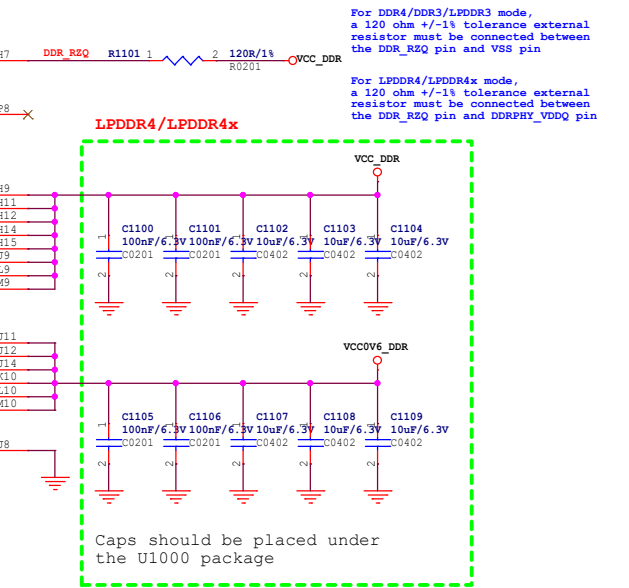


RK3568_F (DDR PHY)

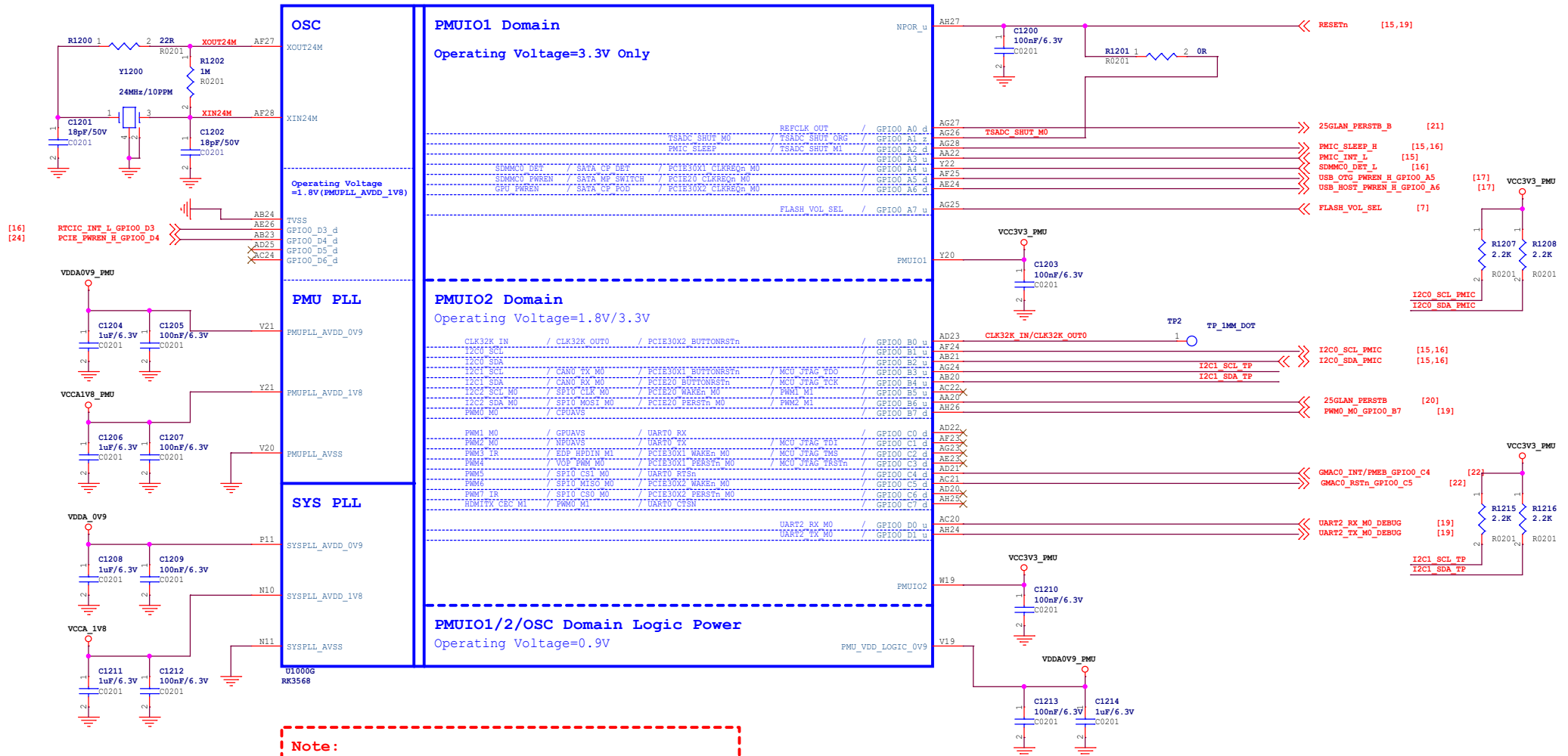
	DDR4	LPDDR4	DDR3	LPDDR3
(14) LPDDR4_DQ0_A	DDR_DQ0_A	F2	DDR_DQ0_A / DDR4_DQ0_A	DDR3_DQ0 / LPDDR3_DQ0
(14) LPDDR4_DQ1_A	DDR_DQ1_A	E1	DDR_DQ1_A / DDR4_DQ1_A	DDR3_DQ1 / LPDDR3_DQ1
(14) LPDDR4_DQ2_A	DDR_DQ2_A	E2	DDR_DQ2_A / DDR4_DQ2_A	DDR3_DQ2 / LPDDR3_DQ2
(14) LPDDR4_DQ3_A	DDR_DQ3_A	D1	DDR_DQ3_A / DDR4_DQ3_A	DDR3_DQ3 / LPDDR3_DQ3
(14) LPDDR4_DQ4_A	DDR_DQ4_A	J1	DDR_DQ4_A / DDR4_DQ4_A	DDR3_DQ4 / LPDDR3_DQ4
(14) LPDDR4_DQ5_A	DDR_DQ5_A	J2	DDR_DQ5_A / DDR4_DQ5_A	DDR3_DQ5 / LPDDR3_DQ5
(14) LPDDR4_DQ6_A	DDR_DQ6_A	H1	DDR_DQ6_A / DDR4_DQ6_A	DDR3_DQ6 / LPDDR3_DQ6
(14) LPDDR4_DQ7_A	DDR_DQ7_A	H4	DDR_DQ7_A / DDR4_DQ7_A	DDR3_DQ7 / LPDDR3_DQ7
(14) LPDDR4_DMO_A	DDR_DMO_A	H5	DDR_DMO_A / DDR4_DMO_A	DDR3_DMO / LPDDR3_DMO
(14) LPDDR4_DQS0P_A	DDR_DQS0P_A	G1	DDR_DQS0P_A / DDR4_DQS0P_A	DDR3_DQS0P / LPDDR3_DQS0P
(14) LPDDR4_DQS0N_A	DDR_DQS0N_A	G2	DDR_DQS0N_A / DDR4_DQS0N_A	DDR3_DQS0N / LPDDR3_DQS0N
(14) LPDDR4_DQ8_A	DDR_DQ8_A	M1	DDR_DQ8_A / DDR4_DQ8_A	DDR3_DQ8 / LPDDR3_DQ8
(14) LPDDR4_DQ9_A	DDR_DQ9_A	N2	DDR_DQ9_A / DDR4_DQ9_A	DDR3_DQ9 / LPDDR3_DQ9
(14) LPDDR4_DQ10_A	DDR_DQ10_A	L7	DDR_DQ10_A / DDR4_DQ10_A	DDR3_DQ10 / LPDDR3_DQ10
(14) LPDDR4_DQ11_A	DDR_DQ11_A	L6	DDR_DQ11_A / DDR4_DQ11_A	DDR3_DQ11 / LPDDR3_DQ11
(14) LPDDR4_DQ12_A	DDR_DQ12_A	K2	DDR_DQ12_A / DDR4_DQ12_A	DDR3_DQ12 / LPDDR3_DQ12
(14) LPDDR4_DQ13_A	DDR_DQ13_A	J6	DDR_DQ13_A / DDR4_DQ13_A	DDR3_DQ13 / LPDDR3_DQ13
(14) LPDDR4_DQ14_A	DDR_DQ14_A	J7	DDR_DQ14_A / DDR4_DQ14_A	DDR3_DQ14 / LPDDR3_DQ14
(14) LPDDR4_DQ15_A	DDR_DQ15_A	L4	DDR_DQ15_A / DDR4_DQ15_A	DDR3_DQ15 / LPDDR3_DQ15
(14) LPDDR4_DMI_A	DDR_DMI_A	J4	DDR_DMI_A / DDR4_DMI_A	DDR3_DMI / LPDDR3_DMI
(14) LPDDR4_DQS1P_A	DDR_DQS1P_A	L2	DDR_DQS1P_A / DDR4_DQS1P_A	DDR3_DQS1P / LPDDR3_DQS1P
(14) LPDDR4_DQS1N_A	DDR_DQS1N_A	L1	DDR_DQS1N_A / DDR4_DQS1N_A	DDR3_DQS1N / LPDDR3_DQS1N
(14) LPDDR4_DQ0_B	DDR_DQ0_B	B10	DDR_DQ0_B / DDR4_DQ0_B	DDR3_DQ0 / LPDDR3_DQ0
(14) LPDDR4_DQ1_B	DDR_DQ1_B	A9	DDR_DQ1_B / DDR4_DQ1_B	DDR3_DQ1 / LPDDR3_DQ1
(14) LPDDR4_DQ2_B	DDR_DQ2_B	D12	DDR_DQ2_B / DDR4_DQ2_B	DDR3_DQ2 / LPDDR3_DQ2
(14) LPDDR4_DQ3_B	DDR_DQ3_B	E12	DDR_DQ3_B / DDR4_DQ3_B	DDR3_DQ3 / LPDDR3_DQ3
(14) LPDDR4_DQ4_B	DDR_DQ4_B	A12	DDR_DQ4_B / DDR4_DQ4_B	DDR3_DQ4 / LPDDR3_DQ4
(14) LPDDR4_DQ5_B	DDR_DQ5_B	D15	DDR_DQ5_B / DDR4_DQ5_B	DDR3_DQ5 / LPDDR3_DQ5
(14) LPDDR4_DQ6_B	DDR_DQ6_B	E15	DDR_DQ6_B / DDR4_DQ6_B	DDR3_DQ6 / LPDDR3_DQ6
(14) LPDDR4_DQ7_B	DDR_DQ7_B	E14	DDR_DQ7_B / DDR4_DQ7_B	DDR3_DQ7 / LPDDR3_DQ7
(14) LPDDR4_DMO_B	DDR_DMO_B	D14	DDR_DMO_B / DDR4_DMO_B	DDR3_DMO / LPDDR3_DMO
(14) LPDDR4_DQS0P_B	DDR_DQS0P_B	A11	DDR_DQS0P_B / DDR4_DQS0P_B	DDR3_DQS0P / LPDDR3_DQS0P
(14) LPDDR4_DQS0N_B	DDR_DQS0N_B	B11	DDR_DQS0N_B / DDR4_DQS0N_B	DDR3_DQS0N / LPDDR3_DQS0N
(14) LPDDR4_DQ8_B	DDR_DQ8_B	A16	DDR_DQ8_B / DDR4_DQ8_B	DDR3_DQ8 / LPDDR3_DQ8
(14) LPDDR4_DQ9_B	DDR_DQ9_B	B17	DDR_DQ9_B / DDR4_DQ9_B	DDR3_DQ9 / LPDDR3_DQ9
(14) LPDDR4_DQ10_B	DDR_DQ10_B	A17	DDR_DQ10_B / DDR4_DQ10_B	DDR3_DQ10 / LPDDR3_DQ10
(14) LPDDR4_DQ11_B	DDR_DQ11_B	B18	DDR_DQ11_B / DDR4_DQ11_B	DDR3_DQ11 / LPDDR3_DQ11
(14) LPDDR4_DQ12_B	DDR_DQ12_B	B13	DDR_DQ12_B / DDR4_DQ12_B	DDR3_DQ12 / LPDDR3_DQ12
(14) LPDDR4_DQ13_B	DDR_DQ13_B	A13	DDR_DQ13_B / DDR4_DQ13_B	DDR3_DQ13 / LPDDR3_DQ13
(14) LPDDR4_DQ14_B	DDR_DQ14_B	D17	DDR_DQ14_B / DDR4_DQ14_B	DDR3_DQ14 / LPDDR3_DQ14
(14) LPDDR4_DQ15_B	DDR_DQ15_B	B14	DDR_DQ15_B / DDR4_DQ15_B	DDR3_DQ15 / LPDDR3_DQ15
(14) LPDDR4_DMI_B	DDR_DMI_B	E17	DDR_DMI_B / DDR4_DMI_B	DDR3_DMI / LPDDR3_DMI
(14) LPDDR4_DQS1P_B	DDR_DQS1P_B	B15	DDR_DQS1P_B / DDR4_DQS1P_B	DDR3_DQS1P / LPDDR3_DQS1P
(14) LPDDR4_DQS1N_B	DDR_DQS1N_B	A15	DDR_DQS1N_B / DDR4_DQS1N_B	DDR3_DQS1N / LPDDR3_DQS1N
(14) LPDDR4_DQ0_P	DDR_DQ0_P	P5	DDR_DQ0_P / DDR4_DQ0_P	DDR3_DQ0_P / LPDDR3_DQ0_P
(14) LPDDR4_DQ1_P	DDR_DQ1_P	M4	DDR_DQ1_P / DDR4_DQ1_P	DDR3_DQ1_P / LPDDR3_DQ1_P
(14) LPDDR4_DQ2_P	DDR_DQ2_P	M5	DDR_DQ2_P / DDR4_DQ2_P	DDR3_DQ2_P / LPDDR3_DQ2_P
(14) LPDDR4_DQ3_P	DDR_DQ3_P	R5	DDR_DQ3_P / DDR4_DQ3_P	DDR3_DQ3_P / LPDDR3_DQ3_P
(14) LPDDR4_DQ4_P	DDR_DQ4_P	M7	DDR_DQ4_P / DDR4_DQ4_P	DDR3_DQ4_P / LPDDR3_DQ4_P
(14) LPDDR4_DQ5_P	DDR_DQ5_P	E7	DDR_DQ5_P / DDR4_DQ5_P	DDR3_DQ5_P / LPDDR3_DQ5_P
(14) LPDDR4_DQ6_P	DDR_DQ6_P	R4	DDR_DQ6_P / DDR4_DQ6_P	DDR3_DQ6_P / LPDDR3_DQ6_P
(14) LPDDR4_DQ7_P	DDR_DQ7_P	R4	DDR_DQ7_P / DDR4_DQ7_P	DDR3_DQ7_P / LPDDR3_DQ7_P
(14) LPDDR4_DQ8_P	DDR_DQ8_P	P7	DDR_DQ8_P / DDR4_DQ8_P	DDR3_DQ8_P / LPDDR3_DQ8_P
(14) LPDDR4_DQ9_P	DDR_DQ9_P	E2	DDR_DQ9_P / DDR4_DQ9_P	DDR3_DQ9_P / LPDDR3_DQ9_P
(14) LPDDR4_DQ10_P	DDR_DQ10_P	E1	DDR_DQ10_P / DDR4_DQ10_P	DDR3_DQ10_P / LPDDR3_DQ10_P
(14) LPDDR4_DQ11_P	DDR_DQ11_P	P1	DDR_DQ11_P / DDR4_DQ11_P	DDR3_DQ11_P / LPDDR3_DQ11_P
(14) LPDDR4_DQ12_P	DDR_DQ12_P	P1	DDR_DQ12_P / DDR4_DQ12_P	DDR3_DQ12_P / LPDDR3_DQ12_P
(14) LPDDR4_DQ13_P	DDR_DQ13_P	P1	DDR_DQ13_P / DDR4_DQ13_P	DDR3_DQ13_P / LPDDR3_DQ13_P
(14) LPDDR4_DQ14_P	DDR_DQ14_P	P1	DDR_DQ14_P / DDR4_DQ14_P	DDR3_DQ14_P / LPDDR3_DQ14_P
(14) LPDDR4_DQ15_P	DDR_DQ15_P	P1	DDR_DQ15_P / DDR4_DQ15_P	DDR3_DQ15_P / LPDDR3_DQ15_P
(14) LPDDR4_DMI_P	DDR_DMI_P	P1	DDR_DMI_P / DDR4_DMI_P	DDR3_DMI_P / LPDDR3_DMI_P
(14) LPDDR4_DQS1P_P	DDR_DQS1P_P	P1	DDR_DQS1P_P / DDR4_DQS1P_P	DDR3_DQS1P_P / LPDDR3_DQS1P_P
(14) LPDDR4_DQS1N_P	DDR_DQS1N_P	P1	DDR_DQS1N_P / DDR4_DQS1N_P	DDR3_DQS1N_P / LPDDR3_DQS1N_P

DDR4	LPDDR4	DDR3	LPDDR3
DDR4_A0	LPDDR4_CLKP_B	DDR3_A9	LPDDR3_DQ15
DDR4_A1	---	DDR3_A2	---
DDR4_A2	LPDDR4_A1_A	DDR3_A4	LPDDR3_A6
DDR4_A3	LPDDR4_CKE1_A	DDR3_A3	---
DDR4_A4	LPDDR4_A3_B	DDR3_BA1	LPDDR3_A3
DDR4_A5	LPDDR4_A5_B	DDR3_A11	LPDDR3_A2
DDR4_A6	LPDDR4_A1_B	DDR3_A13	LPDDR3_A1
DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A8	---
DDR4_A8	LPDDR4_ODT0_CA_A	DDR3_A6	LPDDR3_A9
DDR4_A9	LPDDR4_CLKN_B	DDR3_A5	---
DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	---
DDR4_A11	LPDDR4_A0_A	DDR3_A7	LPDDR3_A8
DDR4_A12	LPDDR4_A3_A	DDR3_BA2	---
DDR4_A13	LPDDR4_A0_B	DDR3_A11	LPDDR3_A0
DDR4_A14	LPDDR4_A1_A	DDR3_A12	LPDDR3_A3
DDR4_A15	LPDDR4_A2_A	DDR3_A12	---
DDR4_A16	RASn	DDR3_A5	LPDDR3_A7
DDR4_A17	LPDDR4_CKE1_B	DDR3_CASn	---
DDR4_A18	LPDDR4_A2_B	DDR3_A12	LPDDR3_A4
DDR4_A19	LPDDR4_A4_B	DDR3_A12	---
DDR4_BG0	LPDDR4_ODT1_CA_B	---	---
DDR4_BG1	LPDDR4_ODT1_CA_A	DDR3_BA0	---
DDR4_CKE	LPDDR4_CKE0_A	DDR3_CKE	LPDDR3_CKE
DDR4_CLKP	LPDDR4_CLKP_A	DDR3_CLKP	LPDDR3_CLKP
DDR4_CLKN	LPDDR4_CLKN_A	DDR3_CLKN	LPDDR3_CLKN
DDR4_CS0n	LPDDR4_CS0n_A	DDR3_ODT1	LPDDR3_ODT0
DDR4_CS1n	LPDDR4_CS1n_A	DDR3_CS1n	LPDDR3_CS0n
DDR4_ODT0	LPDDR4_CS1n_B	DDR3_ODT0	---
DDR4_ODT1	LPDDR4_CS0n_B	DDR3_CS0n	LPDDR3_CS1n
DDR4_RESETh	LPDDR4_RESETh	DDR3_RESETh	---

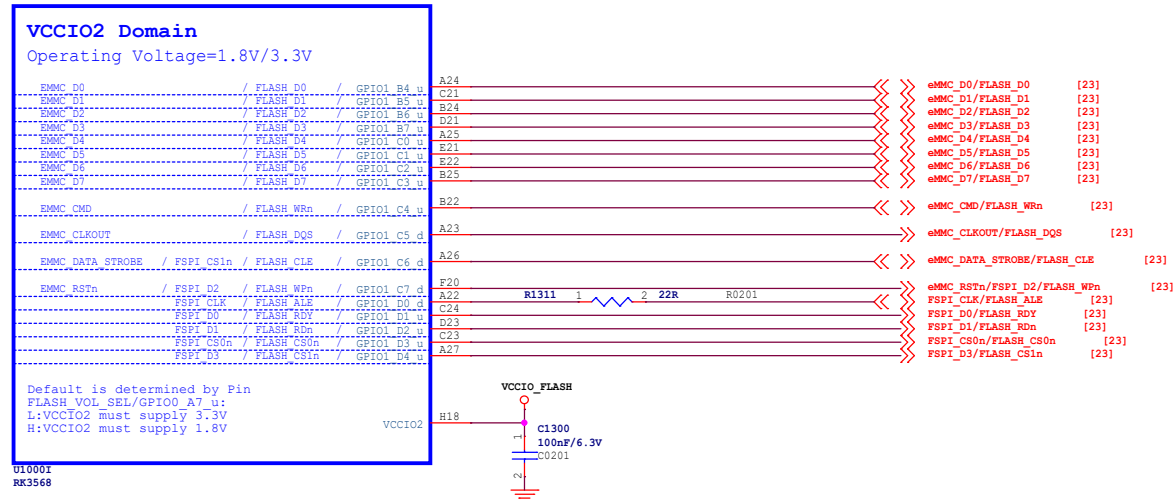
B6	AC0	LPDDR4_CLKP_B	(14)
F5	AC1	---	---
B1	AC2	LPDDR4_A1_A	(14)
F4	AC3	LPDDR4_CKE1_A	(14)
D9	AC4	LPDDR4_A3_B	(14)
D7	AC5	LPDDR4_A5_B	(14)
A7	AC6	LPDDR4_A1_B	(14)
A8	AC7	LPDDR4_ODT0_CA_B	(14)
C1	AC8	LPDDR4_ODT0_CA_A	(14)
A5	AC9	LPDDR4_A0_B	(14)
D6	AC10	LPDDR4_CKE0_B	(14)
C2	AC11	LPDDR4_A0_A	(14)
C4	AC12	LPDDR4_A3_A	(14)
B8	AC13	LPDDR4_A0_B	(14)
C5	AC14	LPDDR4_A4_A	(14)
E4	AC15	LPDDR4_A2_A	(14)
D5	AC16	LPDDR4_A5_A	(14)
E6	AC17	LPDDR4_CKE1_B	(14)
E11	AC18	LPDDR4_A2_B	(14)
E9	AC19	LPDDR4_A4_B	(14)
F8	AC20	---	---
F7	AC21	---	---
B3	AC22	LPDDR4_CKE0_A	(14)
B4	AC23	LPDDR4_CLKP_A	(14)
A4	AC24	LPDDR4_CLKN_A	(14)
A2	AC25	LPDDR4_CS0n_A	(14)
B2	AC26	LPDDR4_CS1n_A	(14)
D8	AC27	LPDDR4_CS0n_B	(14)
E8	AC28	LPDDR4_CS1n_B	(14)
F11	AC29	LPDDR4_RESETh	(14)



RK3568_G (OSC/PLL/PMUIO1/2)

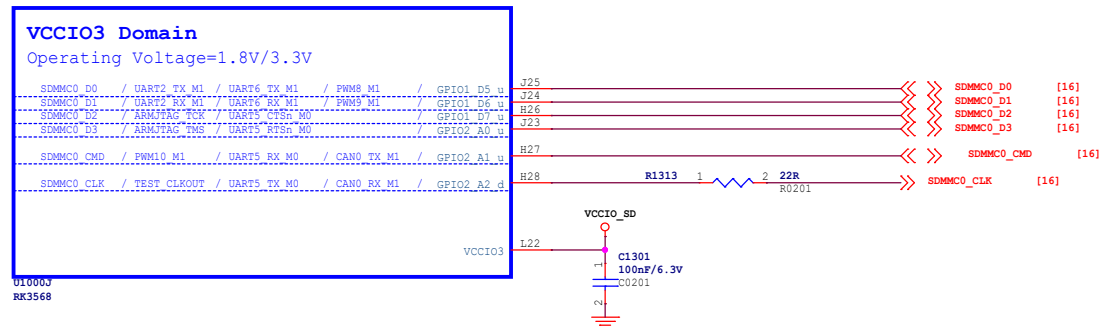


RK3568_I (VCCIO2 Domain)



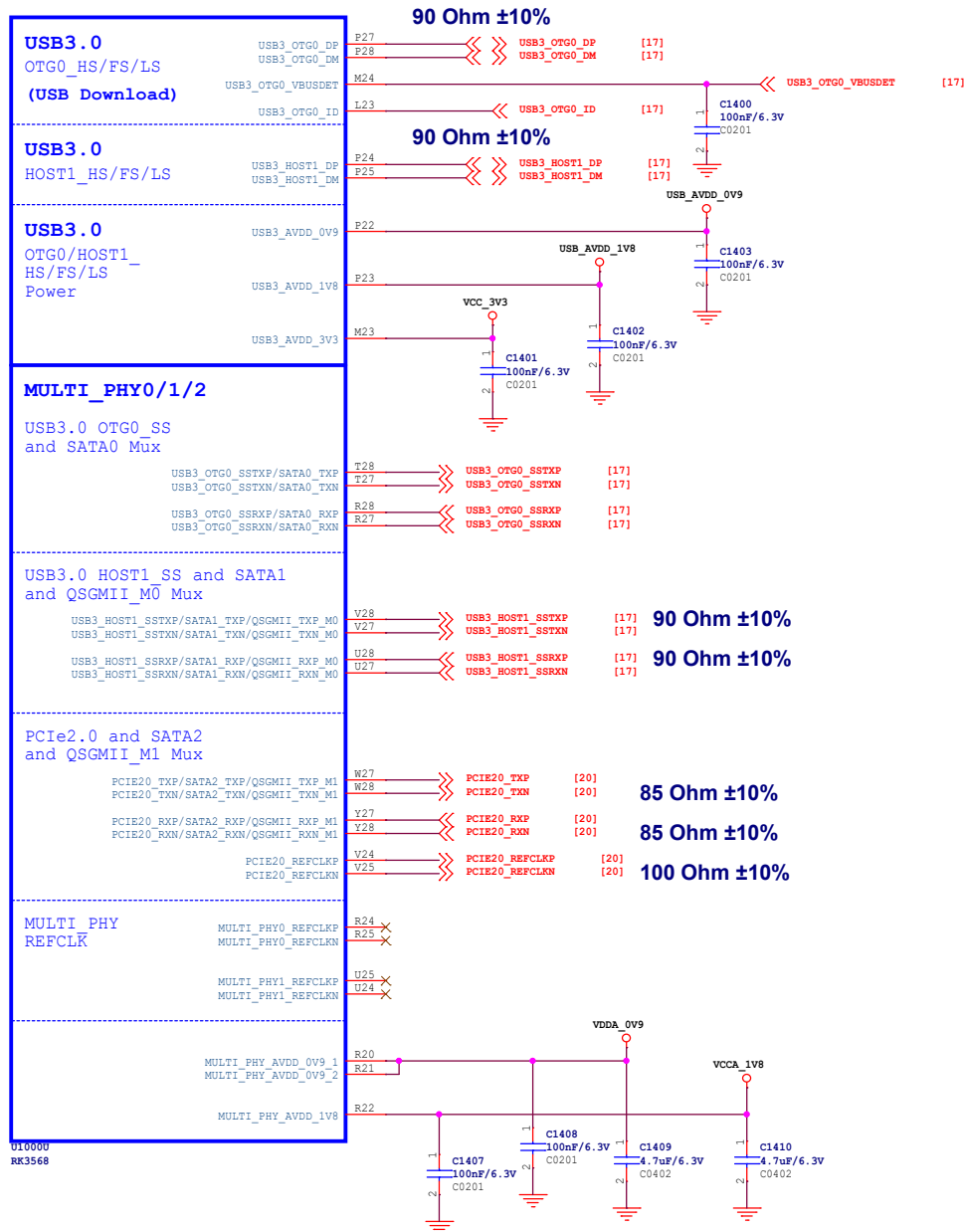
Note:
FLASH VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

RK3568_J (VCCIO3 Domain)



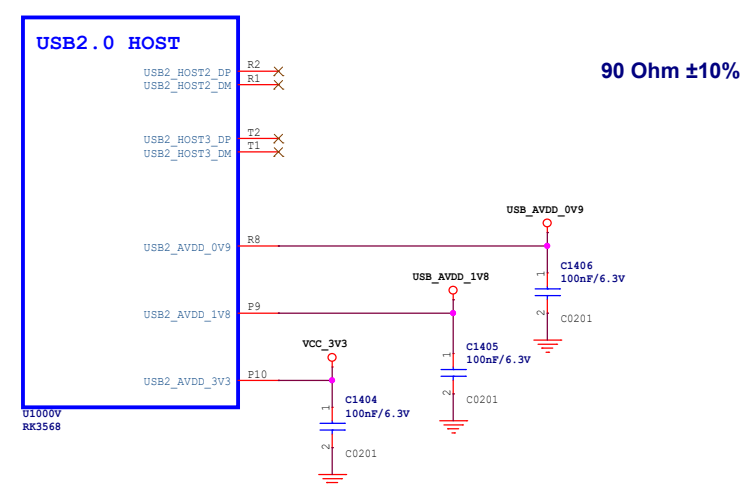
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package

RK3568 V (USB2.0 HOST)

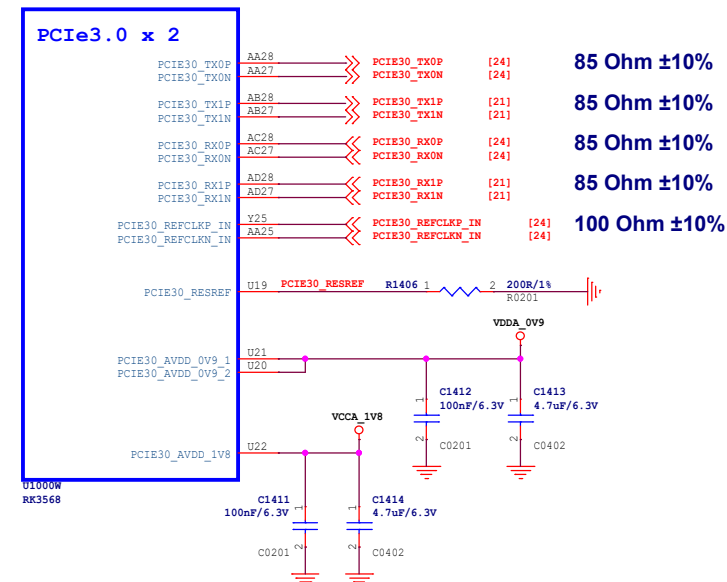


Note:

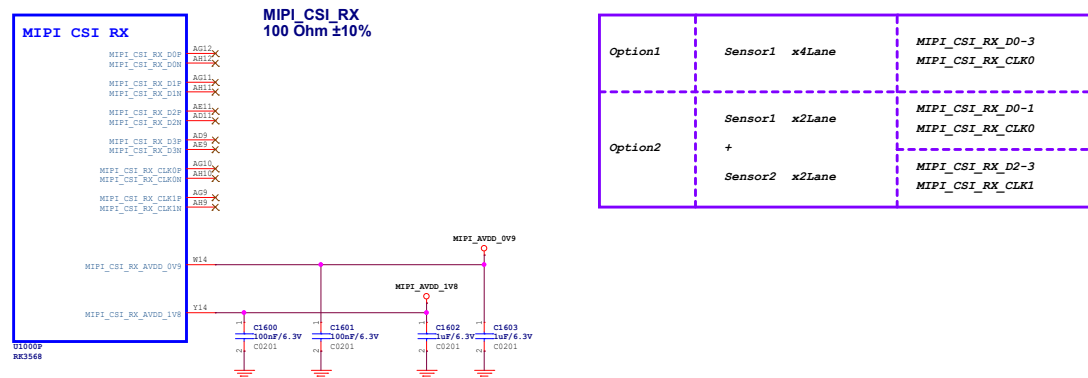
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



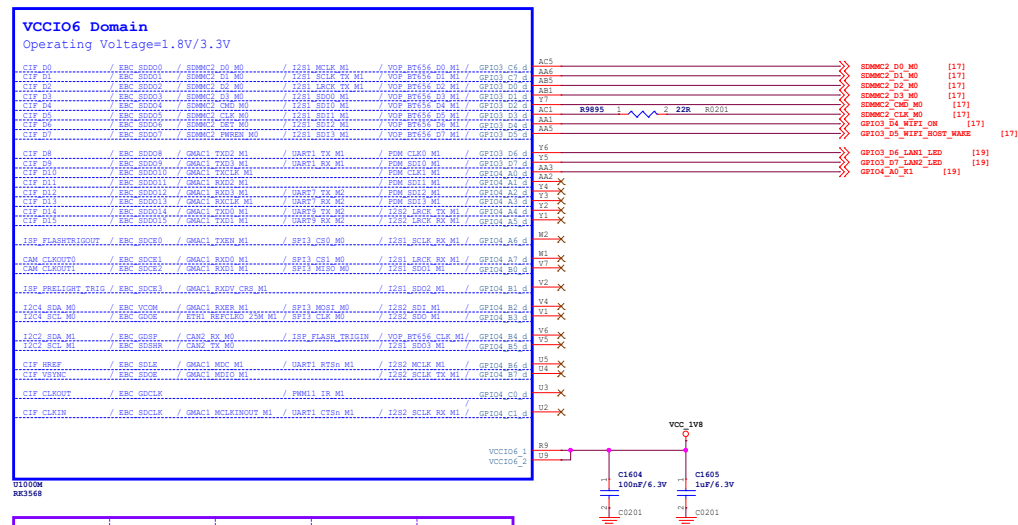
RK3568 W (PCIe3.0 x2)



RK3568_P (MIPI CSI_RX)



RK3568 M(VCCIO6 Domain)



Mode	16bit	12bit	10bit	8bit
<i>CIF_D0</i>	<i>D0</i>	--	--	--
<i>CIF_D1</i>	<i>D1</i>	--	--	--
<i>CIF_D2</i>	<i>D2</i>	--	--	--
<i>CIF_D3</i>	<i>D3</i>	--	--	--
<i>CIF_D4</i>	<i>D4</i>	<i>D0</i>	--	--
<i>CIF_D5</i>	<i>D5</i>	<i>D1</i>	--	--
<i>CIF_D6</i>	<i>D6</i>	<i>D2</i>	<i>D0</i>	--
<i>CIF_D7</i>	<i>D7</i>	<i>D3</i>	<i>D1</i>	--
<i>CIF_D8</i>	<i>D8</i>	<i>D4</i>	<i>D2</i>	<i>D0</i>
<i>CIF_D9</i>	<i>D9</i>	<i>D5</i>	<i>D3</i>	<i>D1</i>
<i>CIF_D10</i>	<i>D10</i>	<i>D6</i>	<i>D4</i>	<i>D2</i>
<i>CIF_D11</i>	<i>D11</i>	<i>D7</i>	<i>D5</i>	<i>D3</i>
<i>CIF_D12</i>	<i>D12</i>	<i>D8</i>	<i>D6</i>	<i>D4</i>
<i>CIF_D13</i>	<i>D13</i>	<i>D9</i>	<i>D7</i>	<i>D5</i>
<i>CIF_D14</i>	<i>D14</i>	<i>D10</i>	<i>D8</i>	<i>D6</i>
<i>CIF_D15</i>	<i>D15</i>	<i>D11</i>	<i>D9</i>	<i>D7</i>

```
Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input
```

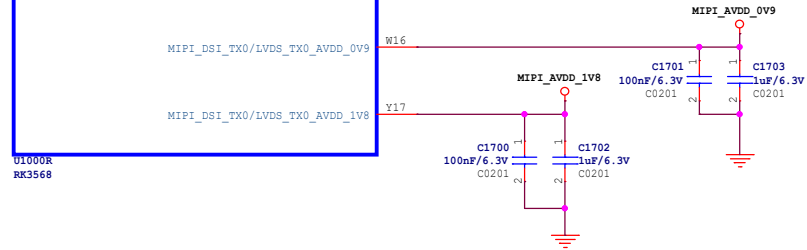
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_R(MIPI_DSI_TX0/LVDS_TX0)

MIPI DSI TX0/LVDS TX0

MIPI_DSI_TX0_D0P/LVDS_TX0_D0P AH17
MIPI_DSI_TX0_D0N/LVDS_TX0_D0N AG17
MIPI_DSI_TX0_D1P/LVDS_TX0_D1P AH16
MIPI_DSI_TX0_D1N/LVDS_TX0_D1N AG16
MIPI_DSI_TX0_D2P/LVDS_TX0_D2P AH14
MIPI_DSI_TX0_D2N/LVDS_TX0_D2N AG14
MIPI_DSI_TX0_D3P/LVDS_TX0_D3P AH13
MIPI_DSI_TX0_D3N/LVDS_TX0_D3N AG13
MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP AH15
MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN AG15

MIPI_DSI_TX0/LVDS_TX0
100 Ohm $\pm 10\%$

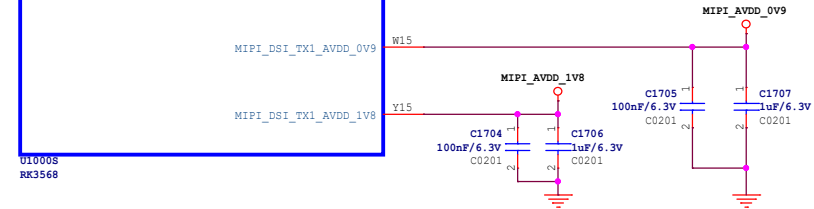


RK3568_S(MIPI_DSI_TX1)

MIPI DSI TX1

MIPI_DSI_TX1_D0P AD18
MIPI_DSI_TX1_D0N AE18
MIPI_DSI_TX1_D1P AD17
MIPI_DSI_TX1_D1N AC17
MIPI_DSI_TX1_D2P AD14
MIPI_DSI_TX1_D2N AC14
MIPI_DSI_TX1_D3P AD12
MIPI_DSI_TX1_D3N AE12
MIPI_DSI_TX1_CLKP AD15
MIPI_DSI_TX1_CLKN AE15

MIPI_DSI_TX1
100 Ohm $\pm 10\%$

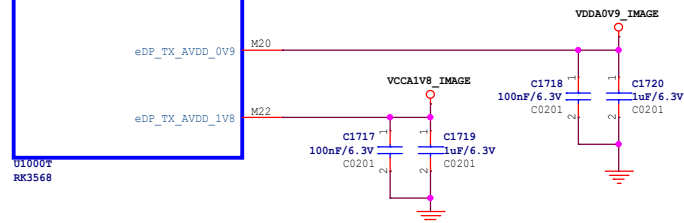


RK3568_T(eDP TX)

eDP_TX

eDP_TX_D0P J28
eDP_TX_D0N K27
eDP_TX_D1P K28
eDP_TX_D1N L27
eDP_TX_D2P L28
eDP_TX_D2N M27
eDP_TX_D3P M28
eDP_TX_D3N N27
eDP_TX_AUXP L25
eDP_TX_AUXN M25

HDMI TMDs trace
100 Ohm $\pm 10\%$



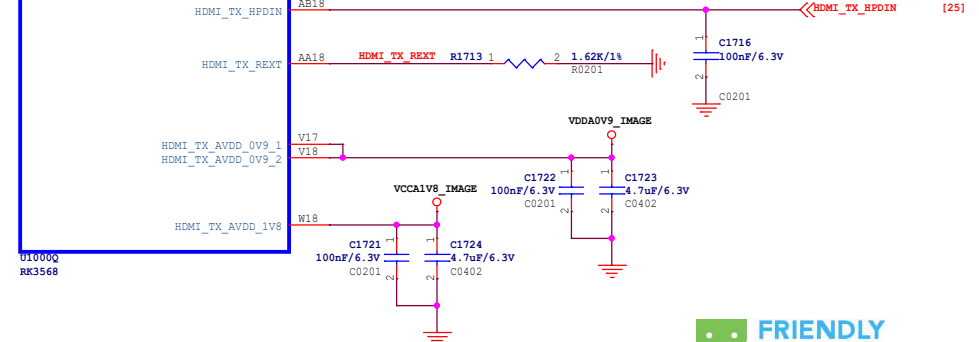
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_Q(HDMI2.0 TX)

HDMI2.0 TX

HDMI_TX_D2P	AG22	HDMI_TX2P	R1708	1	2	2.2R	R0201	HDMI_TX2P_PORT	[25]
HDMI_TX_D2N	AH22	HDMI_TX2N	R1704	1	2	2.2R	R0201	HDMI_TX2N_PORT	[25]
HDMI_TX_D1P	AG21	HDMI_TX1P	R1705	1	2	2.2R	R0201	HDMI_TX1P_PORT	[25]
HDMI_TX_D1N	AH21	HDMI_TX1N	R1706	1	2	2.2R	R0201	HDMI_TX1N_PORT	[25]
HDMI_TX_D0P	AG20	HDMI_TX0P	R1709	1	2	2.2R	R0201	HDMI_TX0P_PORT	[25]
HDMI_TX_D0N	AH20	HDMI_TX0N	R1707	1	2	2.2R	R0201	HDMI_TX0N_PORT	[25]
HDMI_TX_CLKP	AH19	HDMI_TXCLKP	R1710	1	2	2.2R	R0201	HDMI_TXCLKP_PORT	[25]
HDMI_TX_CLKN	AG19	HDMI_TXCLKN	R1711	1	2	2.2R	R0201	HDMI_TXCLKN_PORT	[25]



RK3568_L (VCCIO5 Domain)

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

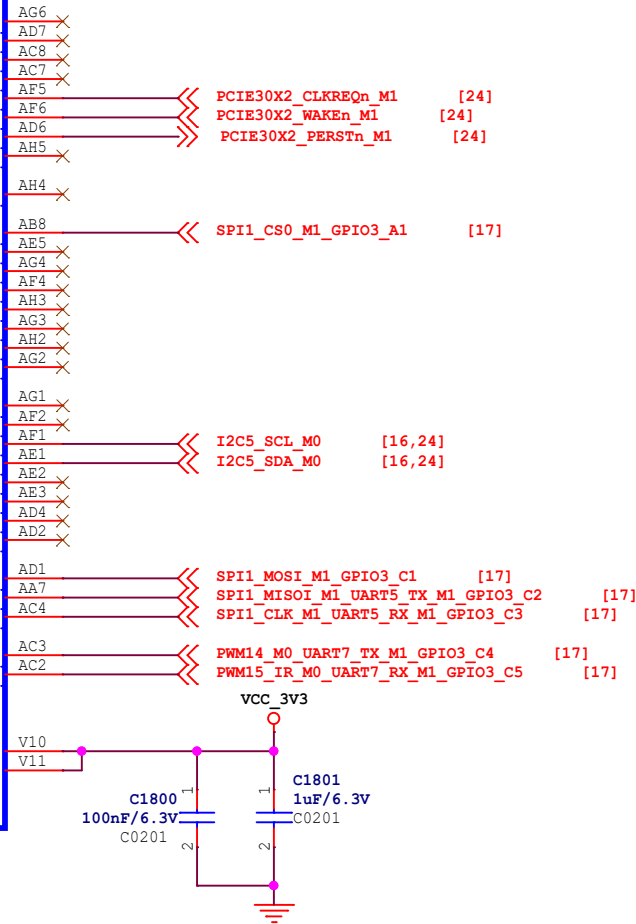
LCDC D0	/ VOP BT656 D0 M0	/ SPI0 MISO M1	/ PCIE20 CLKREQn M1	/ I2S1 MCLK M2	/ GPIO2 D0 d
LCDC D1	/ VOP BT656 D1 M0	/ SPI0 MOSI M1	/ PCIE20 WAKEn M1	/ I2S1 SCLK TX M2	/ GPIO2 D1 d
LCDC D2	/ VOP BT656 D2 M0	/ SPI0 CS0 M1	/ PCIE30X1 CLKREQn M1	/ I2S1 LRCK TX M2	/ GPIO2 D2 d
LCDC D3	/ VOP BT656 D3 M0	/ SPI0 CLK M1	/ PCIE30X1 WAKEn M1	/ I2S1 SDIO M2	/ GPIO2 D3 d
LCDC D4	/ VOP BT656 D4 M0	/ SPI2 CS1 M1	/ PCIE30X2 CLKREQn M1	/ I2S1 SDI1 M2	/ GPIO2 D4 d
LCDC D5	/ VOP BT656 D5 M0	/ SPI2 CS0 M1	/ PCIE30X2 WAKEn M1	/ I2S1 SDI2 M2	/ GPIO2 D5 d
LCDC D6	/ VOP BT656 D6 M0	/ SPI2 MOSI M1	/ PCIE30X2 PERSTn M1	/ I2S1 SDI3 M2	/ GPIO2 D6 d
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART8 TX M1	/ I2S1 SDO0 M2	/ GPIO2 D7 d
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART8 RX M1	/ I2S1 SDO1 M2	/ GPIO3 A0 d
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERSTn M1	/ SDMMC2 D0 M1	/ GPIO3 A1 d
LCDC D9	/ VOP BT1120 D1	/ GMAC1 TXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1	/ GPIO3 A2 d
LCDC D10	/ VOP BT1120 D2	/ GMAC1 TXD3 M0	/ I2S3 SCLK M0	/ SDMMC2 D2 M1	/ GPIO3 A3 d
LCDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0	/ I2S3 LRCK M0	/ SDMMC2 D3 M1	/ GPIO3 A4 d
LCDC D12	/ VOP BT1120 D4	/ GMAC1 RXD3 M0	/ I2S3 SDO M0	/ SDMMC2 CMD M1	/ GPIO3 A5 d
LCDC D13	/ VOP BT1120 CLK	/ GMAC1 TXCLK M0	/ I2S3 SDI M0	/ SDMMC2 CLK M1	/ GPIO3 A6 d
LCDC D14	/ VOP BT1120 D5	/ GMAC1 RXCLK M0	/ SDMMC2 DET M1	/ GPIO3 A7 d	
LCDC D15	/ VOP BT1120 D6	/ ETH1 REFCLK0 25M M0	/ SDMMC2 PWREN M1	/ GPIO3 B0 d	
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ PWM8 M0	/ GPIO3 B1 d
LCDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ PWM9 M0	/ GPIO3 B2 d
LCDC D18	/ VOP BT1120 D9	/ GMAC1 RXDV CRS M0	/ I2C5 SCL M0	/ PDM SDIO M2	/ GPIO3 B3 d
LCDC D19	/ VOP BT1120 D10	/ GMAC1 RXER M0	/ I2C5 SDA M0	/ PDM SDI1 M2	/ GPIO3 B4 d
LCDC D20	/ VOP BT1120 D11	/ GMAC1 TXD0 M0	/ I2C3 SCL M1	/ PWM10 M0	/ GPIO3 B5 d
LCDC D21	/ VOP BT1120 D12	/ GMAC1 TXD1 M0	/ I2C3 SDA M1	/ PWM11 IR M0	/ GPIO3 B6 d
LCDC D22	/ PWM12 M0	/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SDI2 M2	/ GPIO3 B7 d
LCDC D23	/ PWM13 M0	/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SDI3 M2	/ GPIO3 C0 d
LCDC HSYNC	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERSTn M1	/ I2S1 SDO2 M2	/ GPIO3 C1 d
LCDC VSYNC	/ VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ I2S1 SDO3 M2	/ GPIO3 C2 d
LCDC DEN	/ VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ I2S1 SCLK RX M2	/ GPIO3 C3 d
PWM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0	/ UART7 TX M1	/ PDM CLK1 M2	/ GPIO3 C4 d
PWM15 IR M0	/ SPDIF TX M1	/ GMAC1 MDIO M0	/ UART7 RX M1	/ I2S1 LRCK RX M2	/ GPIO3 C5 d

VCCIO5_1
VCCIO5_2

U1000L
RK3568

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package



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NanoPi R5S

Rev
2204

Size Page Name
A4 12.RK3568_VO Interface_2

Date: Thursday, May 05, 2022 Sheet: 12/ 25

RK3568_H (VCCIO1 Domain)

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3 SDA M0	/ UART3 RX M0	/ CAN1 RX M0	/ AUDIOPWM LOUT P	/ ACODEC ADC DATA	/ GPIO1 A0 u
I2C3 SCL M0	/ UART3 TX M0	/ CAN1 TX M0	/ AUDIOPWM LOUT N	/ ACODEC ADC CLK	/ GPIO1 A1 u
I2S1 MCLK M0	/ UART3 RTSn M0	/ SCR CLK	/ PCIE30X1 PERSTn M2		/ GPIO1 A2 d
I2S1 SCLK TX M0	/ UART3 CTSn M0	/ SCR IO	/ PCIE30X1 WAKEn M2	/ ACODEC DAC CLK	/ GPIO1 A3 d
I2S1 SCLK RX M0	/ UART4 RX M0	/ PDM CLK1 M0	/ SPDIF TX M0		/ GPIO1 A4 d
I2S1 LRCK TX M0	/ UART4 RTSn M0	/ SCR RST	/ PCIE30X1 CLKREOn M2	/ ACODEC DAC SYNC	/ GPIO1 A5 d
I2S1 LRCK RX M0	/ UART4 TX M0	/ PDM CLK0 M0	/ AUDIOPWM ROUT P		/ GPIO1 A6 d
I2S1 SDO0 M0	/ UART4 CTSn M0	/ SCR DET	/ AUDIOPWM ROUT N	/ ACODEC DAC DATAL	/ GPIO1 A7 d
I2S1 SDO1 M0	/ I2S1 SDI3 M0	/ PDM SDI3 M0	/ PCIE20 CLKREOn M2	/ ACODEC DAC DATAR	/ GPIO1 B0 d
I2S1 SDO2 M0	/ I2S1 SDI2 M0	/ PDM SDI2 M0	/ PCIE20 WAKEn M2	/ ACODEC ADC SYNC	/ GPIO1 B1 d
I2S1 SDO3 M0	/ I2S1 SDI1 M0	/ PDM SDI1 M0	/ PCIE20 PERSTn M2		/ GPIO1 B2 d
	/ I2S1 SDI0 M0	/ PDM SDI0 M0			/ GPIO1 B3 d

U1000H
RK3568

VCCIO1

D18 I2C3 SDA M0
E18 I2C3 SCL M0

A19 ✕

B19 ✕

F18 ✕

A20 ✕

C20 ✕

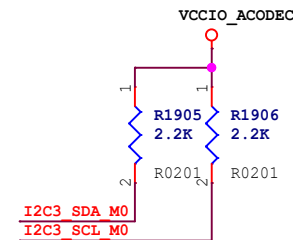
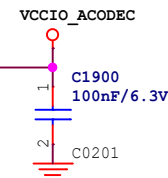
B20 ✕

D20 ✕

E20 ✕

A21 ✕

B21 ✕



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package



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NanoPi R5S

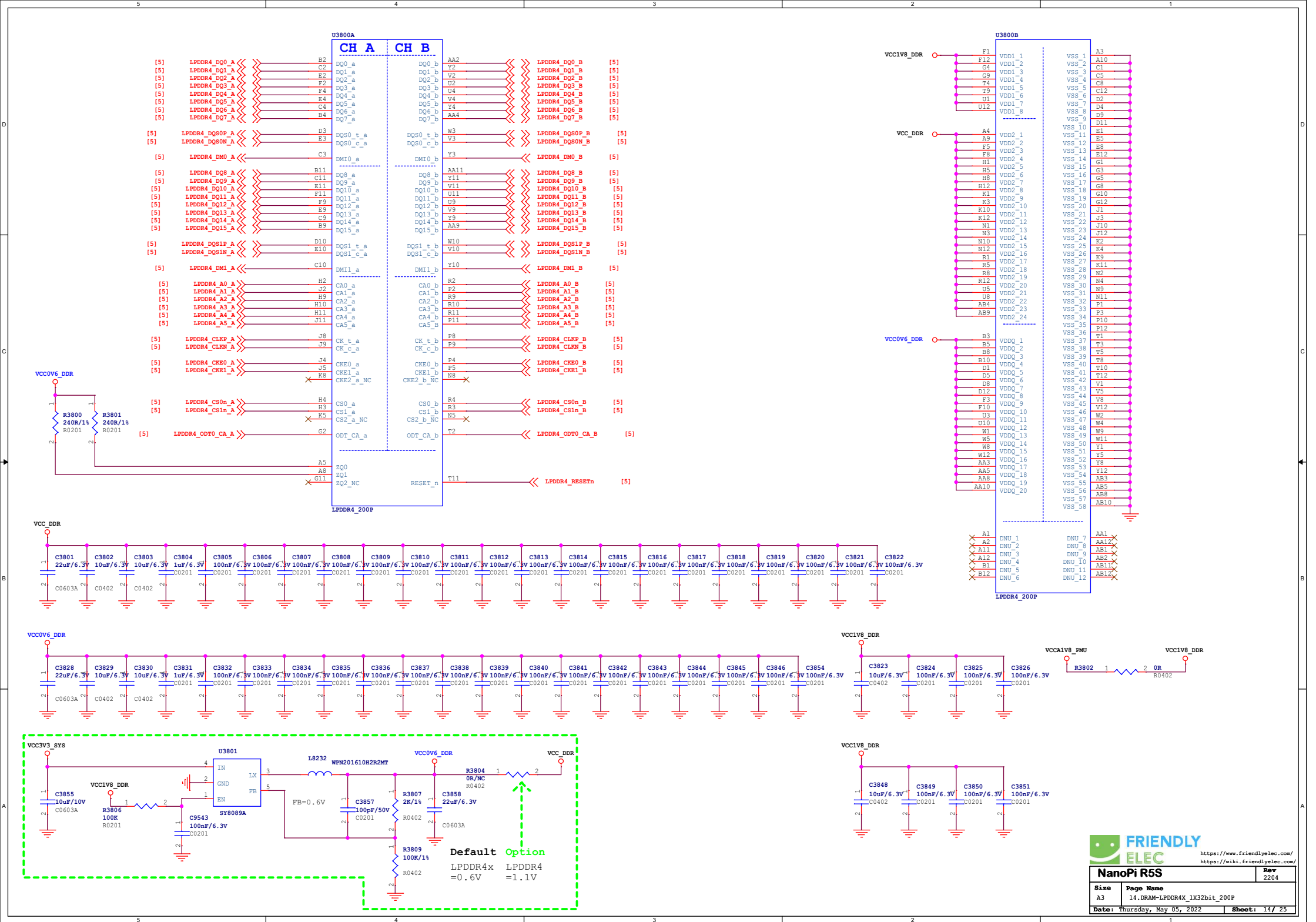
Rev
2204

Size
A4

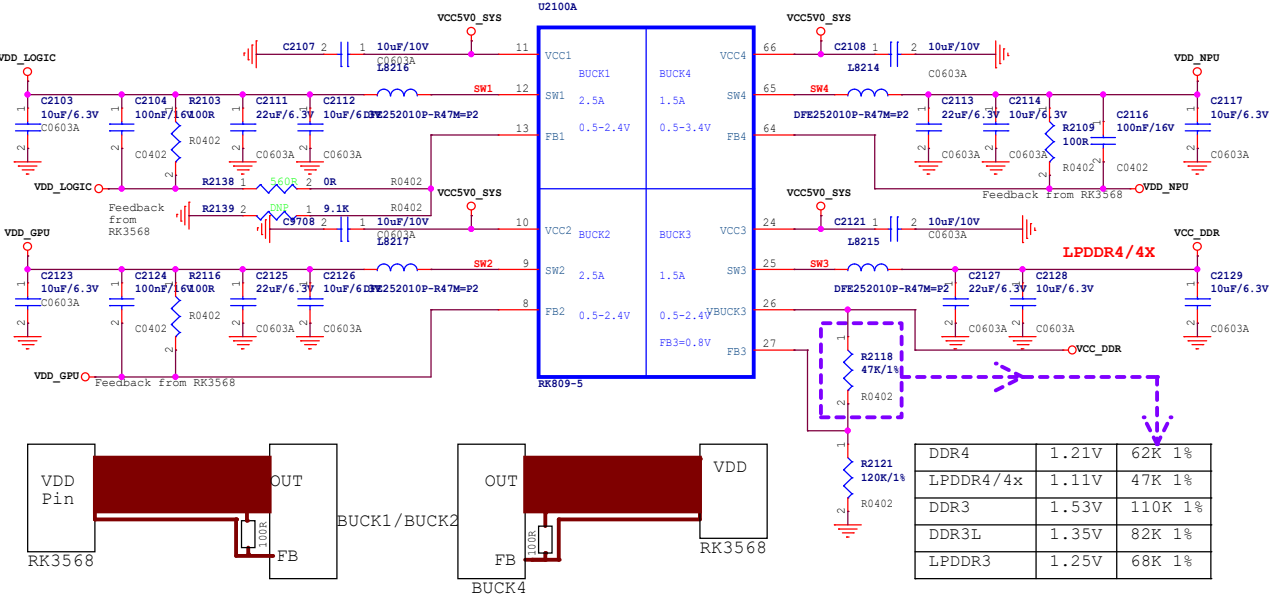
Page Name
13.RK3568 Audio Interface

Date: Thursday, May 05, 2022

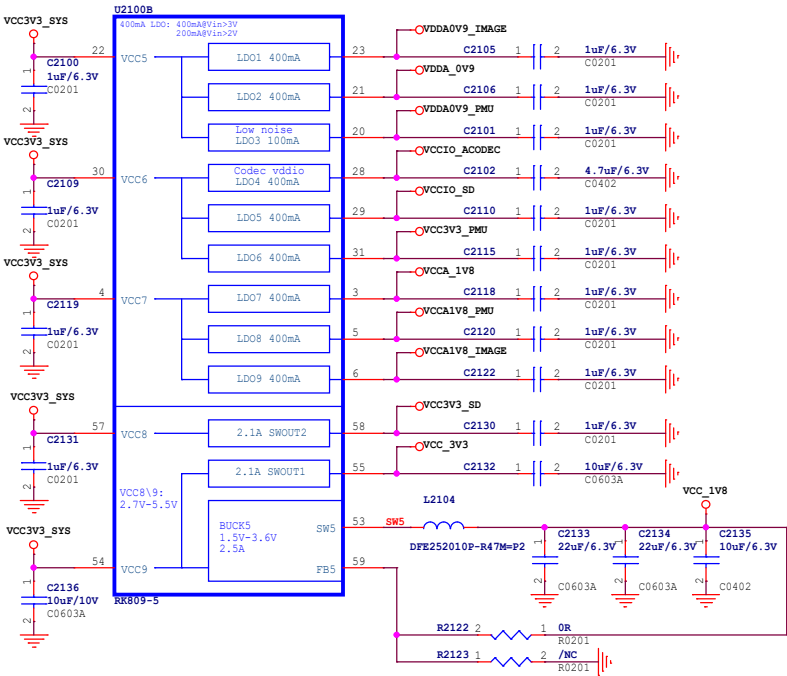
Sheet: 13/ 25



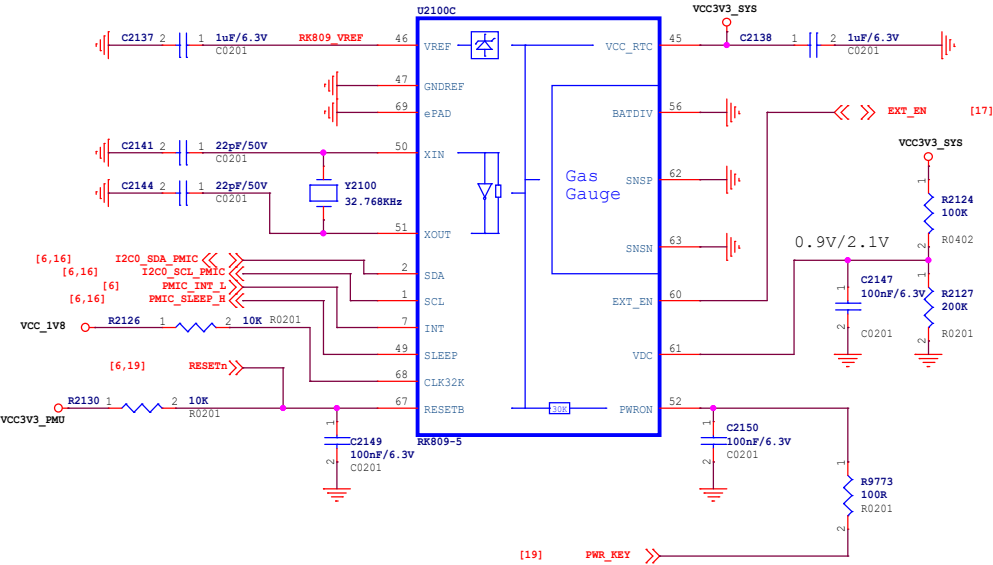
PMIC RK809 DCDC



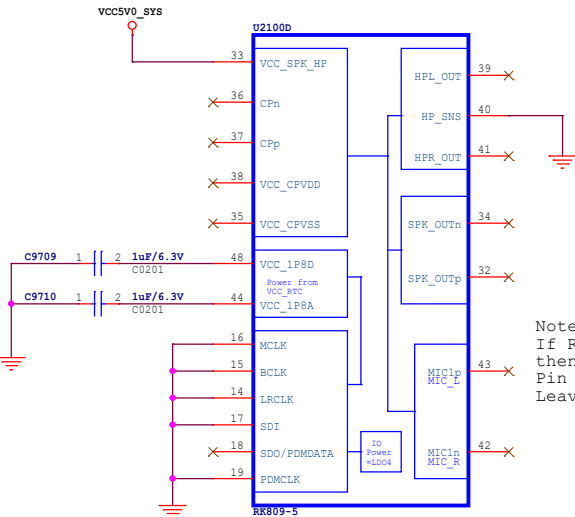
PMIC RK809 LDO



PMIC RK809 Management

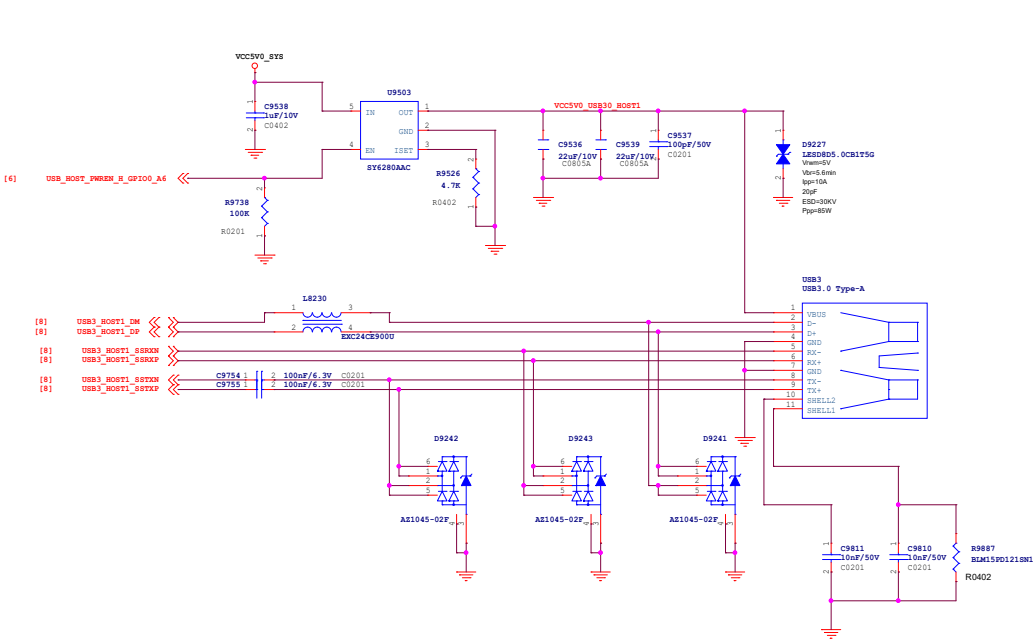


PMIC RK809 CODEC

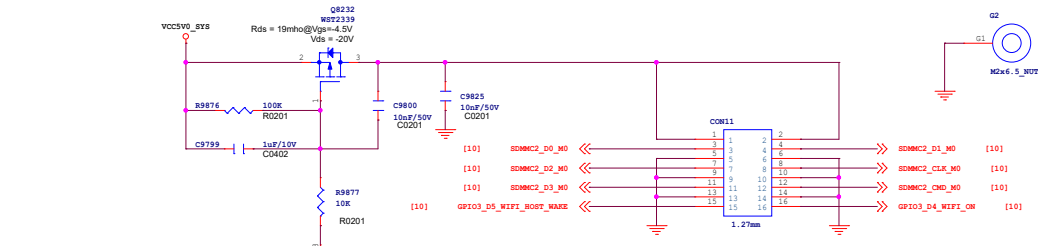


Note:
If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

USB 3.0

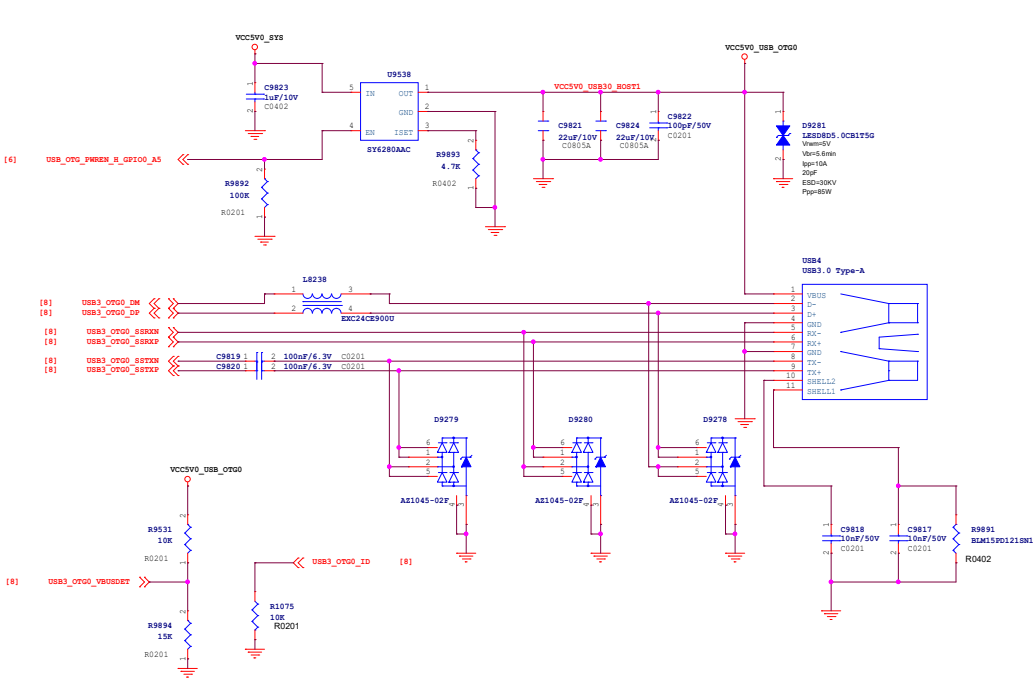


SDIO/I2S

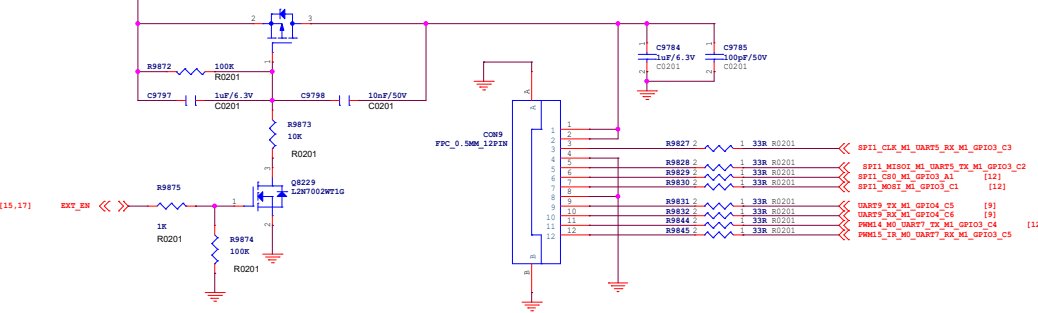


Pin#	GPIO	SD/MMC/SDIO	I2S	POWER	Description
1				VCCSV0_SYS	5V power output
2				VCCSV0_SYS	5V power output
3	GPIO3_C6	SDMMC2_D0_M0	I2S1_MCLK_M1		1.8V level
4	GPIO3_C7	SDMMC2_D1_M0	I2S1_SCLK_TX_M1		1.8V level
5				GND	
6				GND	
7	GPIO3_D0	SDMMC2_D2_M0	I2S1_LRCK_TX_M1		1.8V level
8	GPIO3_D3	SDMMC2_CLK_M0	I2S1_DI1_M1		1.8V level
9				GND	
10				GND	
11	GPIO3_D1	SDMMC2_D3_M0	I2S1_SDO0_M1		1.8V level
12	GPIO3_D2	SDMMC2_CMD_M0	I2S1_SDIO_M1		1.8V level
13				GND	
14				GND	
15	GPIO3_D5	SDMMC2_PWREN_M0	I2S1_DI3_M1		1.8V level
16	GPIO3_D4	SDMMC2_DET_M0	I2S1_DI2_M1		1.8V level

USB 3.0/ADB/MASK

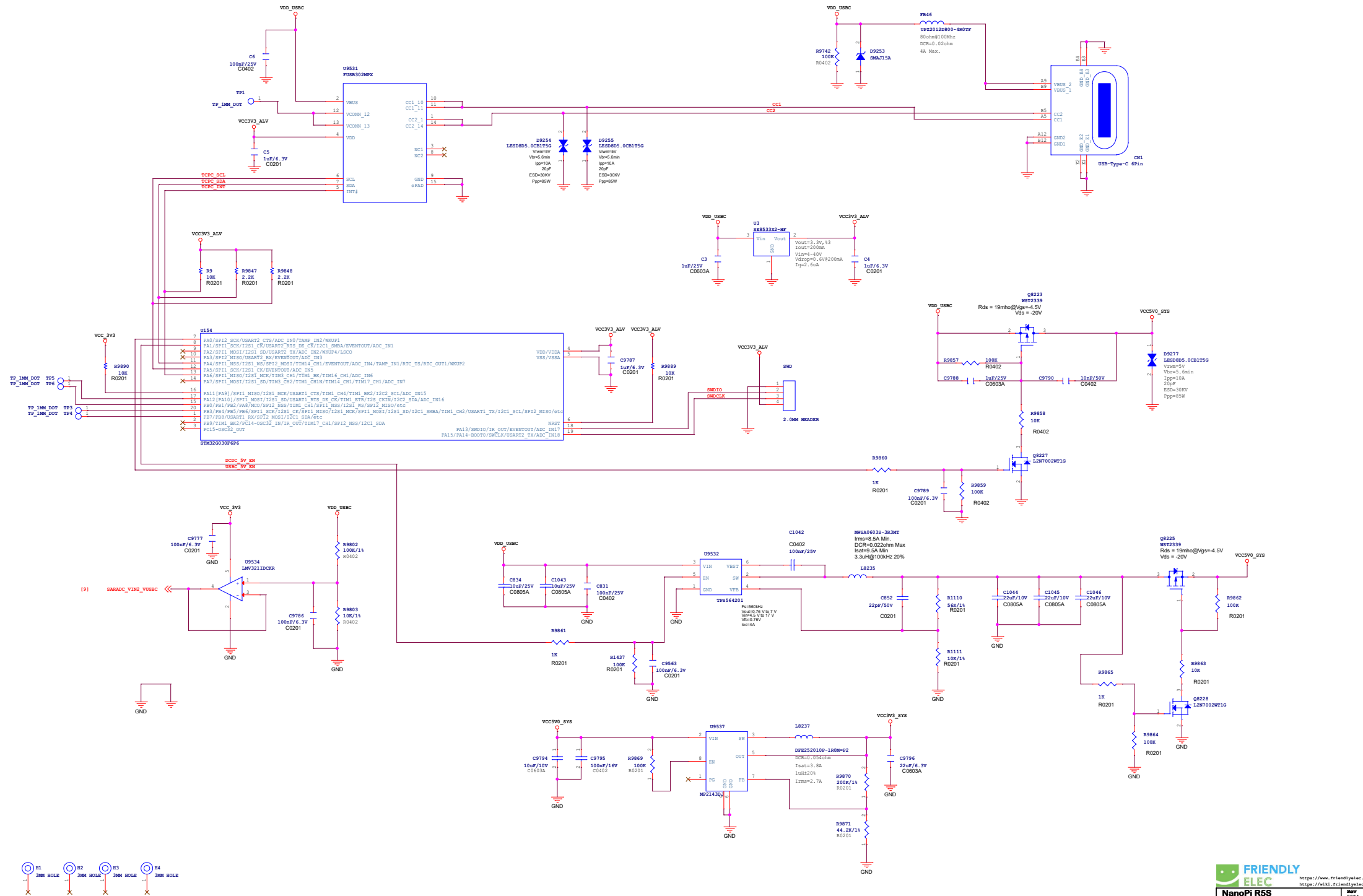


GPIO

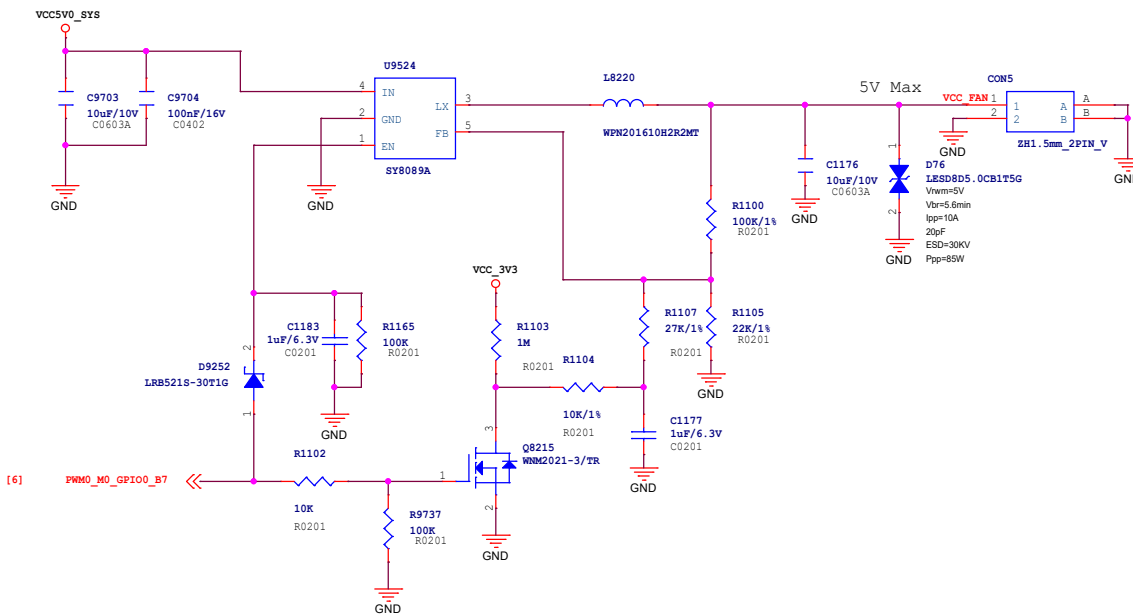


Pin#	GPIO	SPI	UART	PWM	POWER	Description
1					VCCSV3_SYS	3.3V power output
2					VCCSV3_SYS	3.3V power output
3	GPIO3_C3	SPI1_CLK_M1	UART5_RX_M1			3.3V level
4					GND	
5	GPIO3_C2	SPI1_MISO1_M1	UART5_TX_M1			3.3V level
6	GPIO3_A1	SPI1_CS0_M1				3.3V level
7	GPIO3_C1	SPI1_MOSI_M1				3.3V level
8					GND	
9	GPIO4_C5		UART9_TX_M1	PWM12_M1		3.3V level
10	GPIO4_C6		UART9_RX_M1	PWM13_M1		3.3V level
11	GPIO3_C4		UART7_TX_M1	PWM14_M0		3.3V level
12	GPIO3_C5		UART7_RX_M1	PWM15_IR_M0		3.3V level

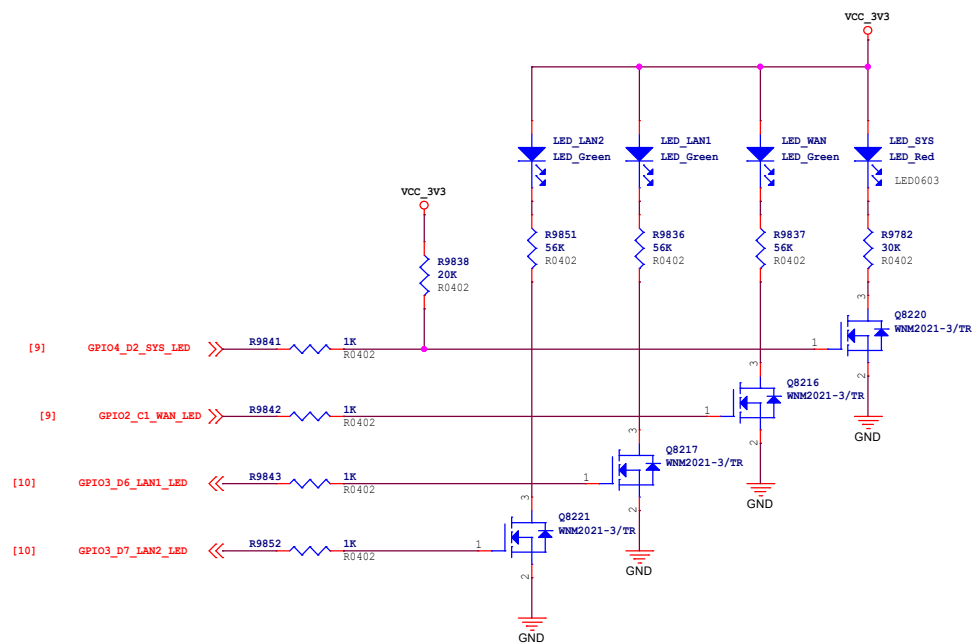
USB PD



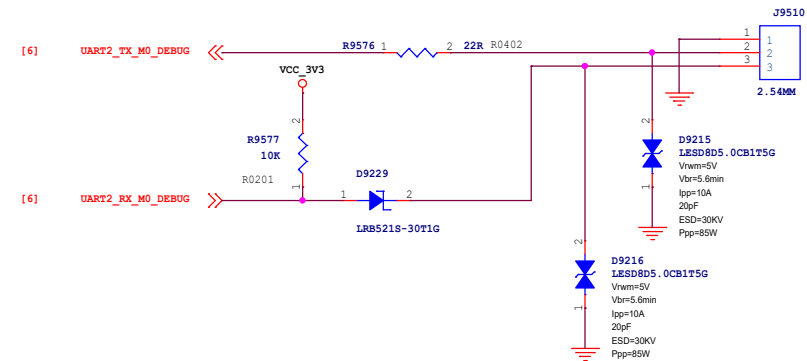
Cooling Fan



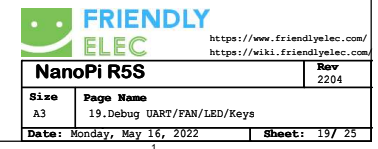
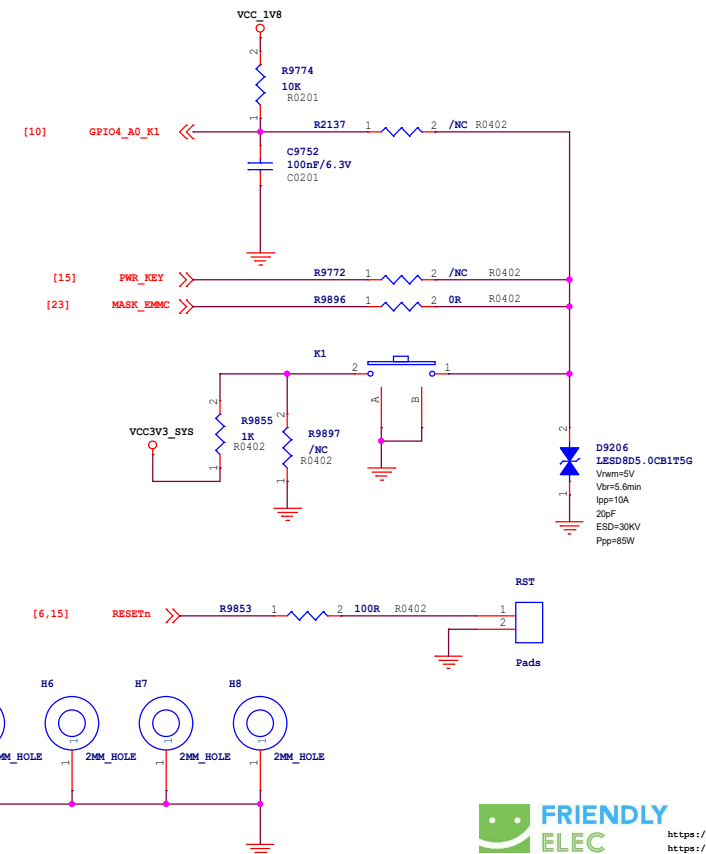
LED



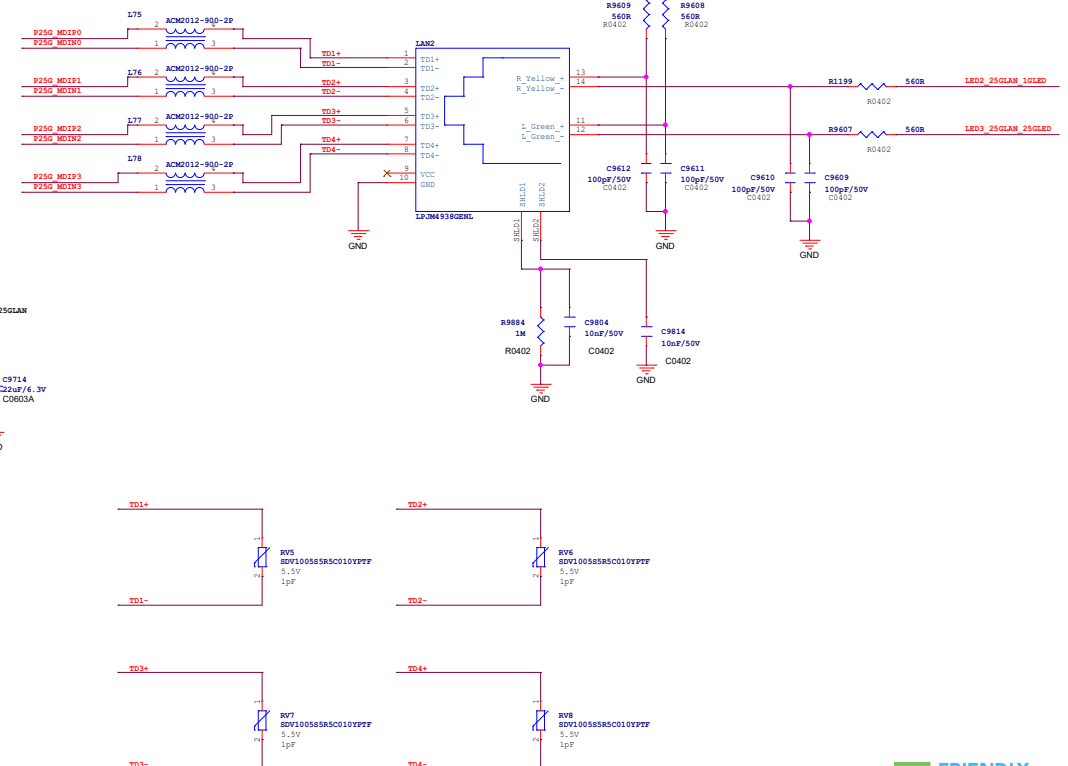
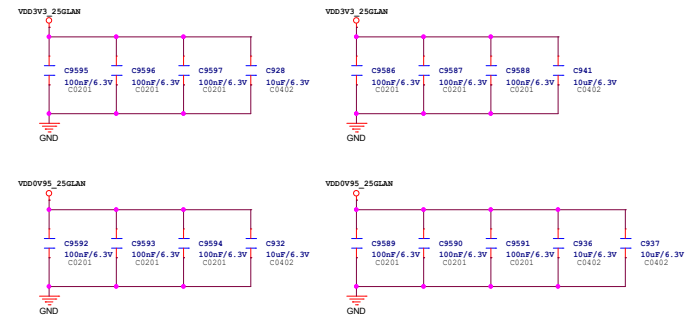
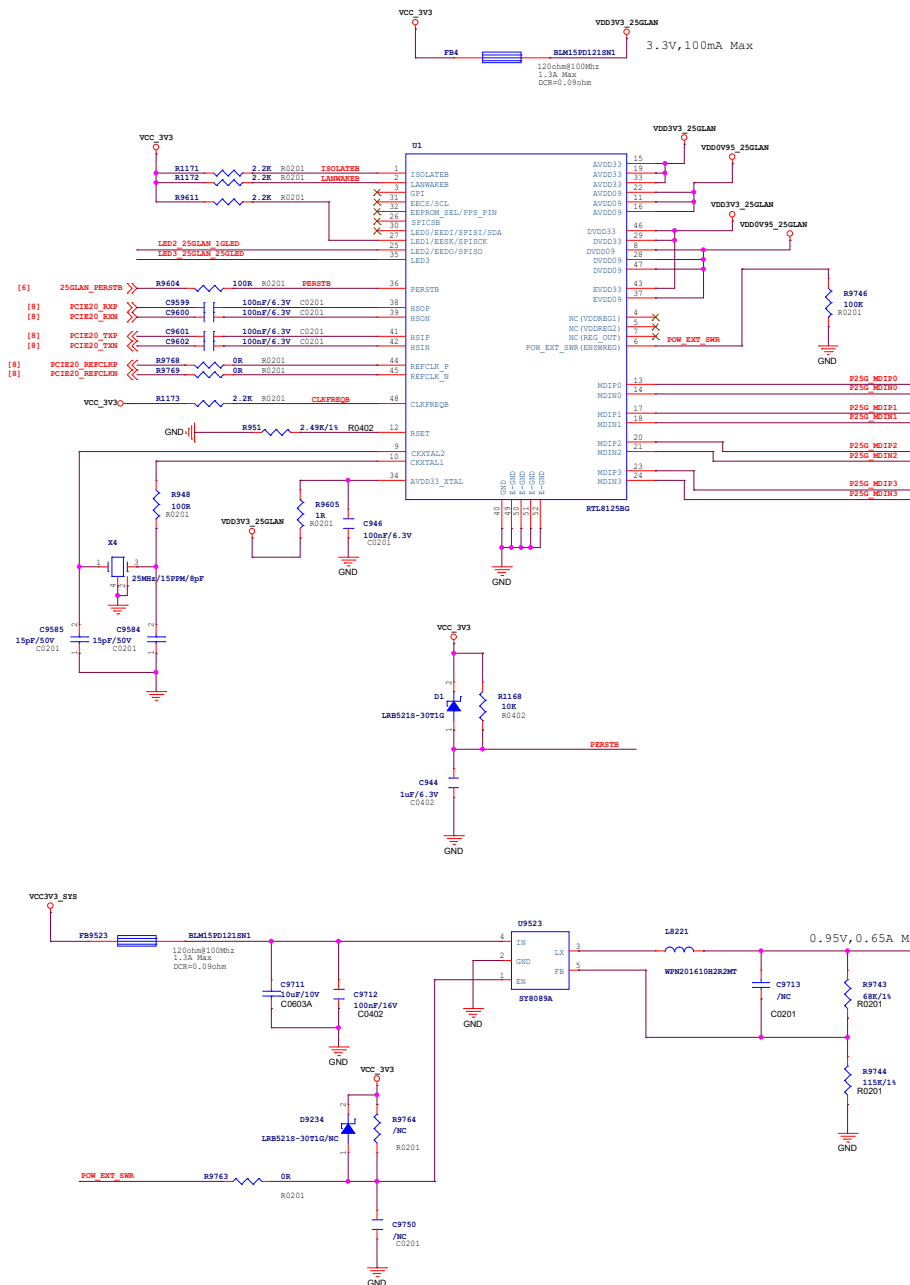
Debug UART



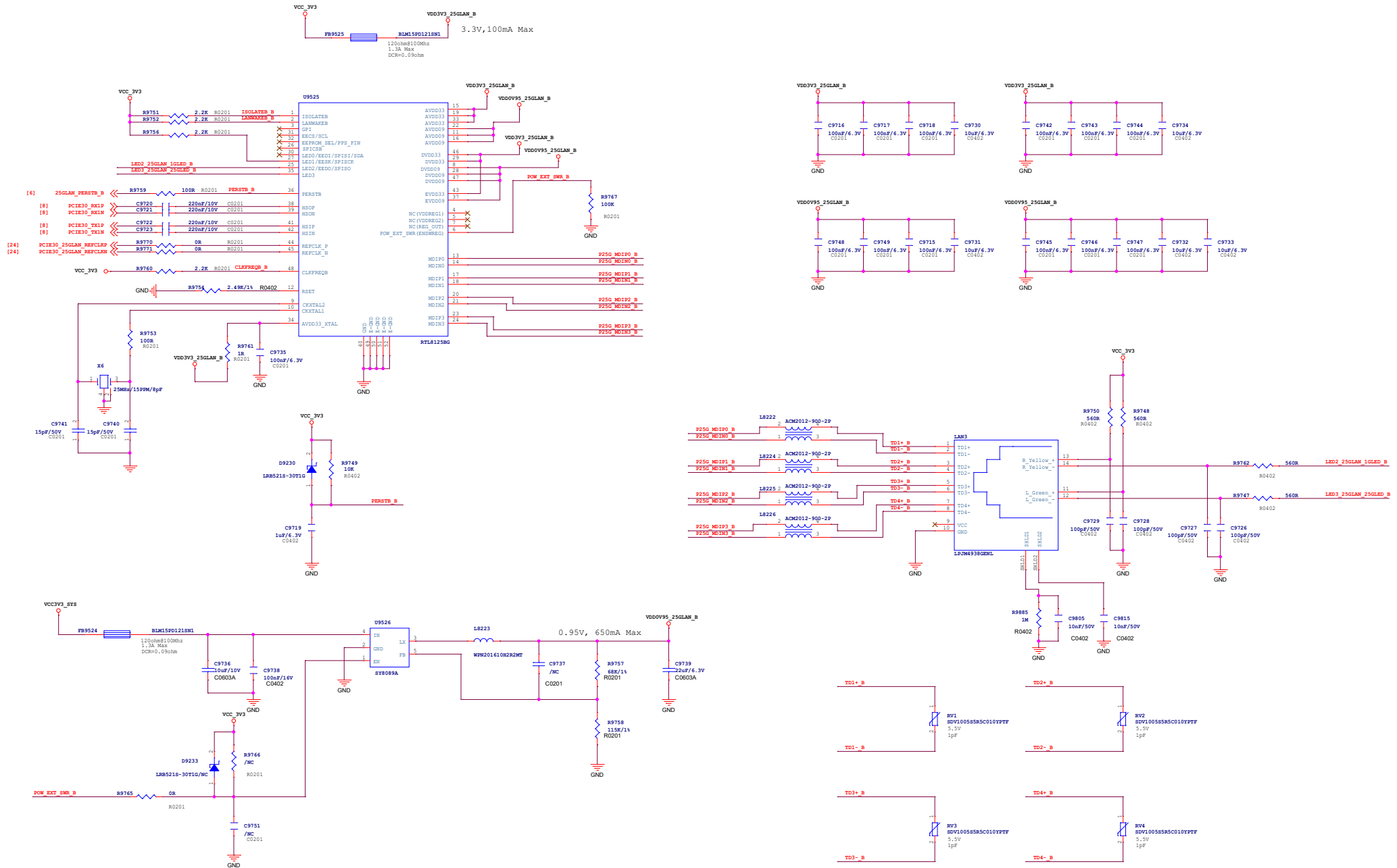
Button



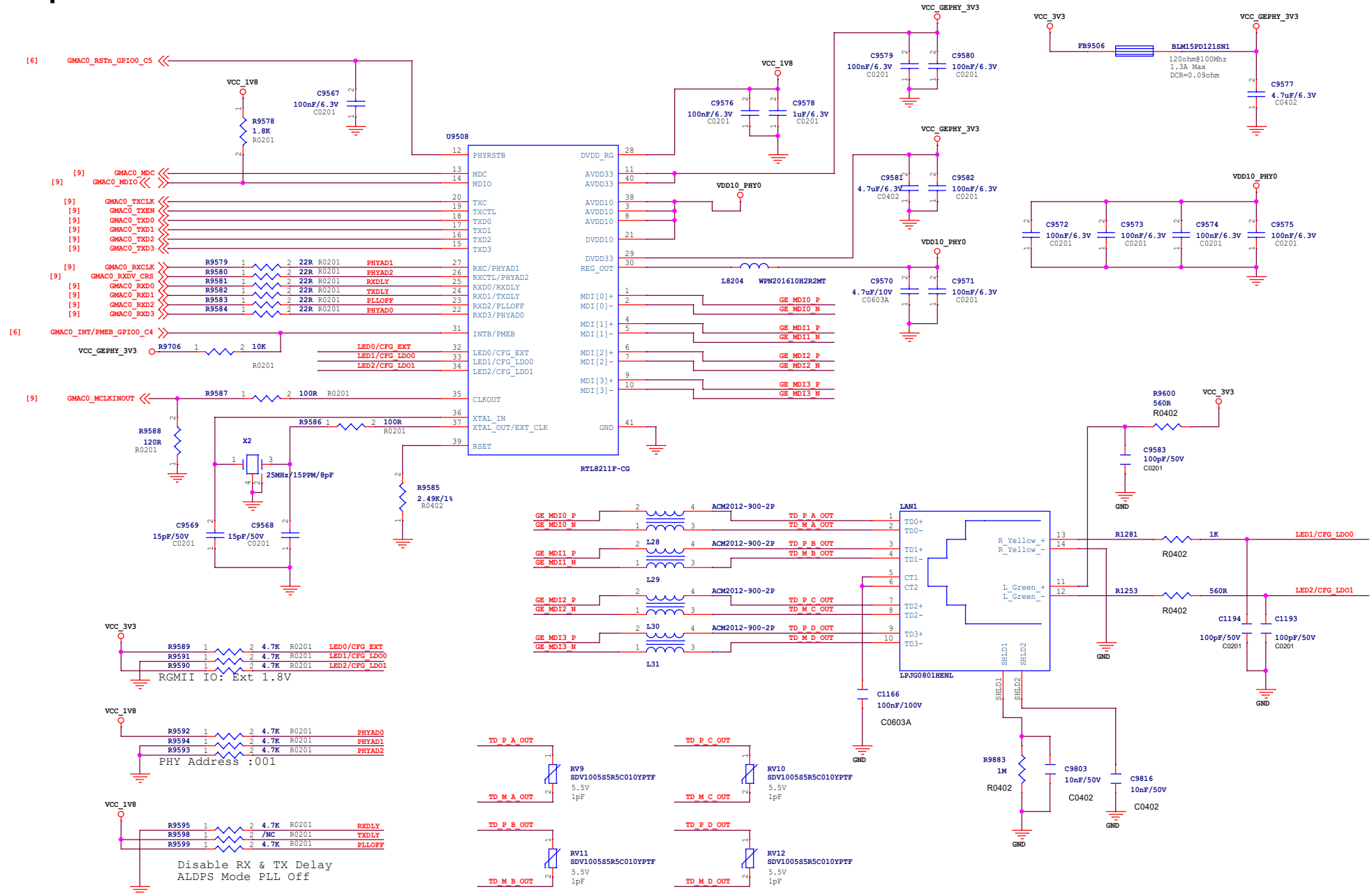
2.5Gbps Ethernet



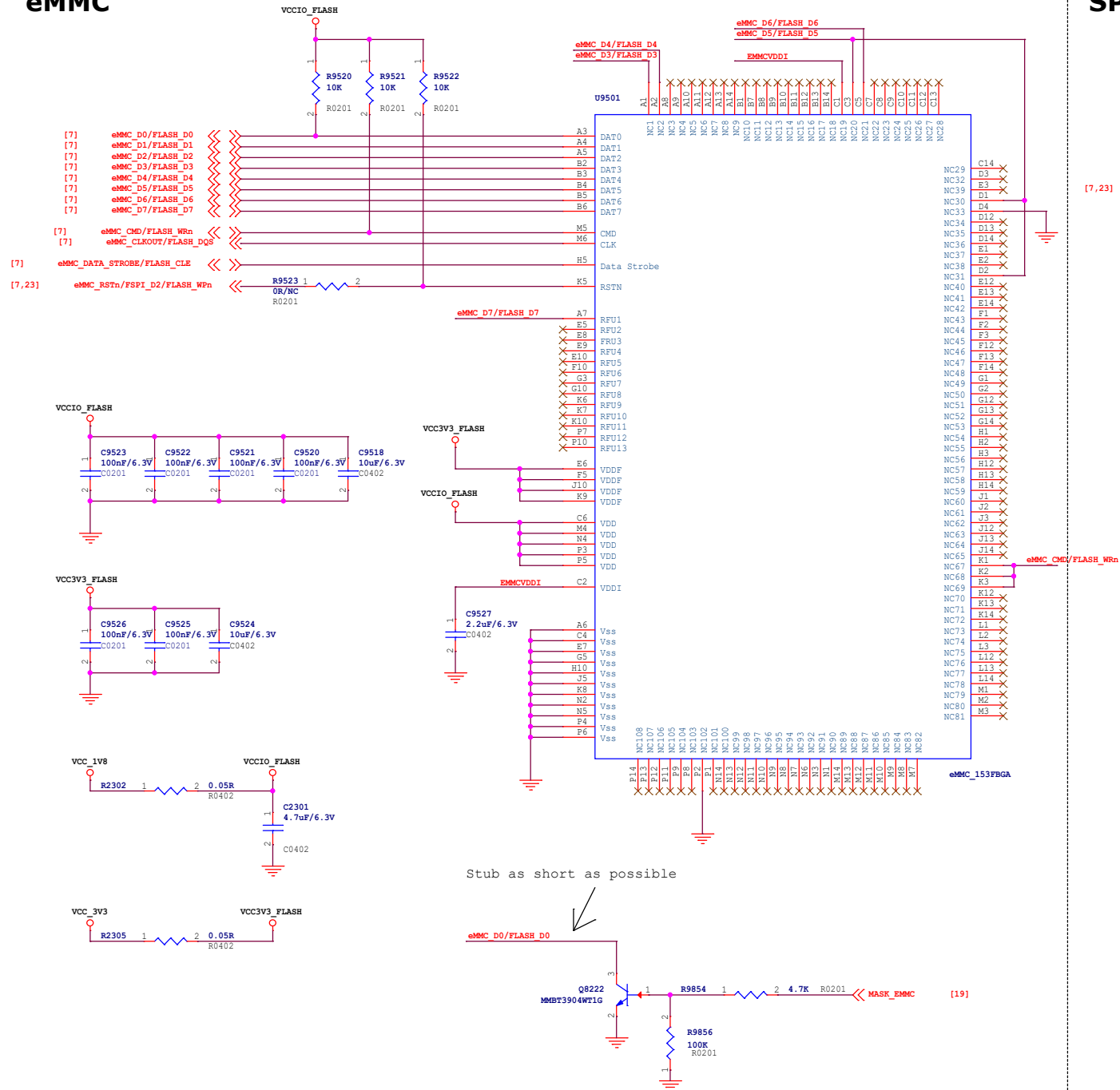
2.5Gbps Ethernet



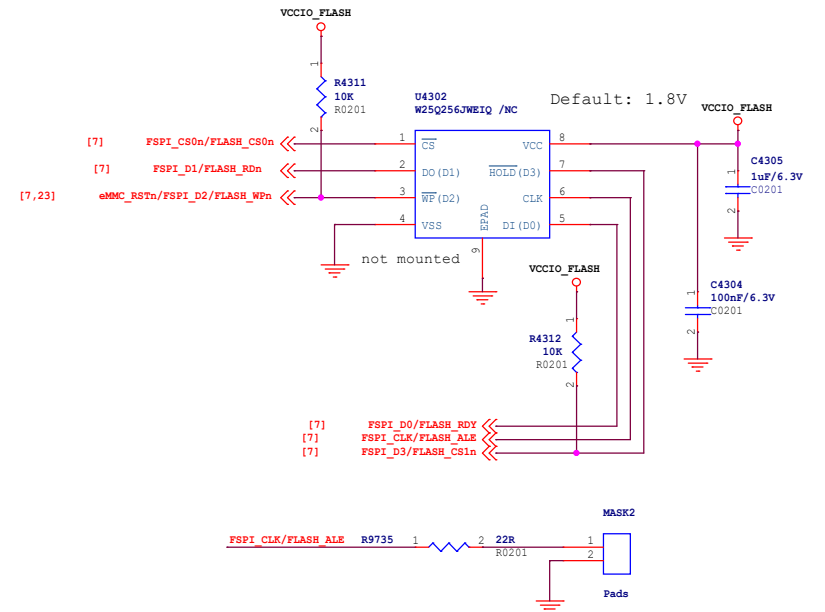
1Gbps Ethernet



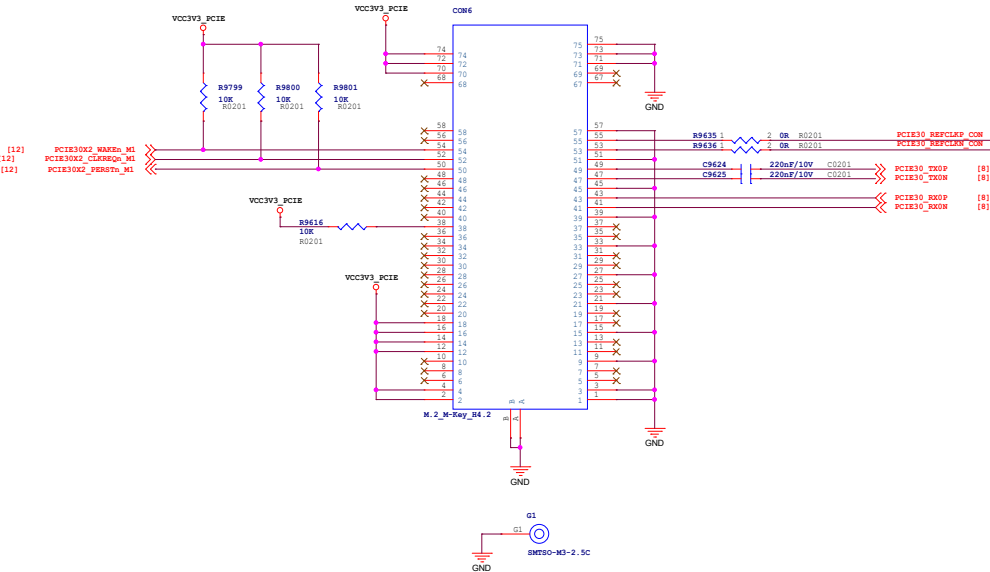
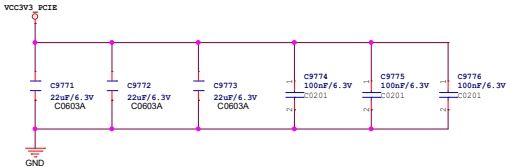
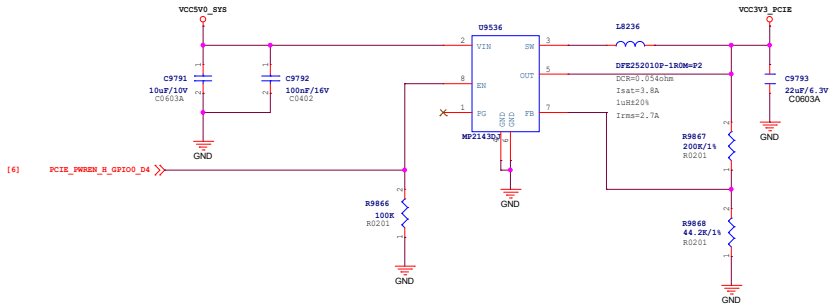
eMMC



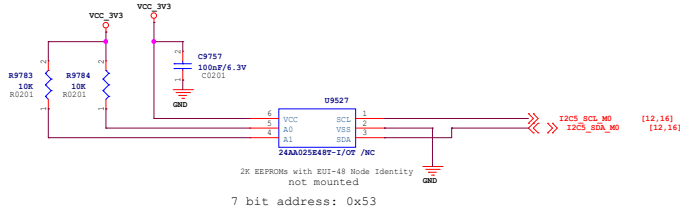
SPI Flash



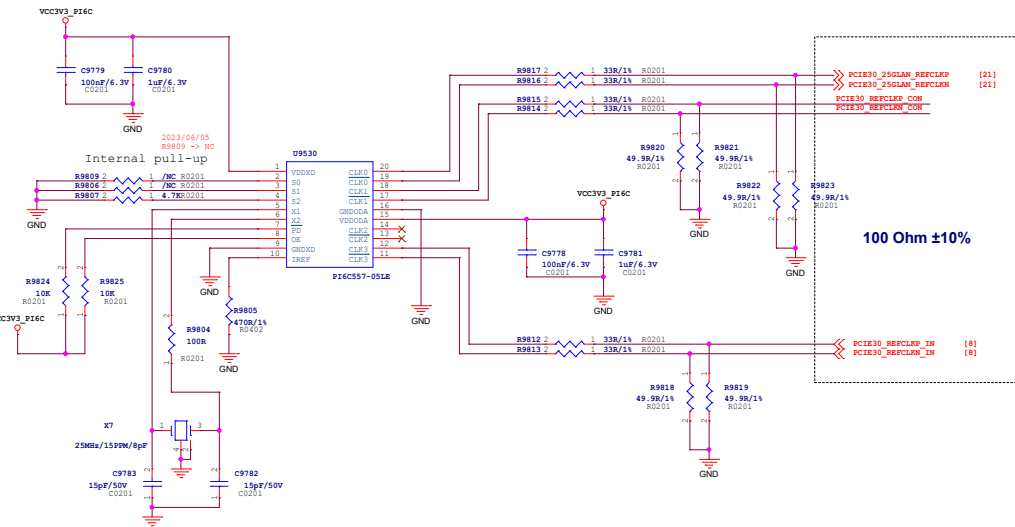
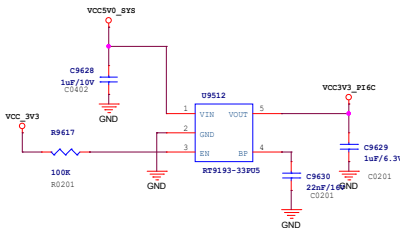
M.2 NVME



EUI-48 Node Identity



PCIe REFCLK



HDMI 2.0 TX

