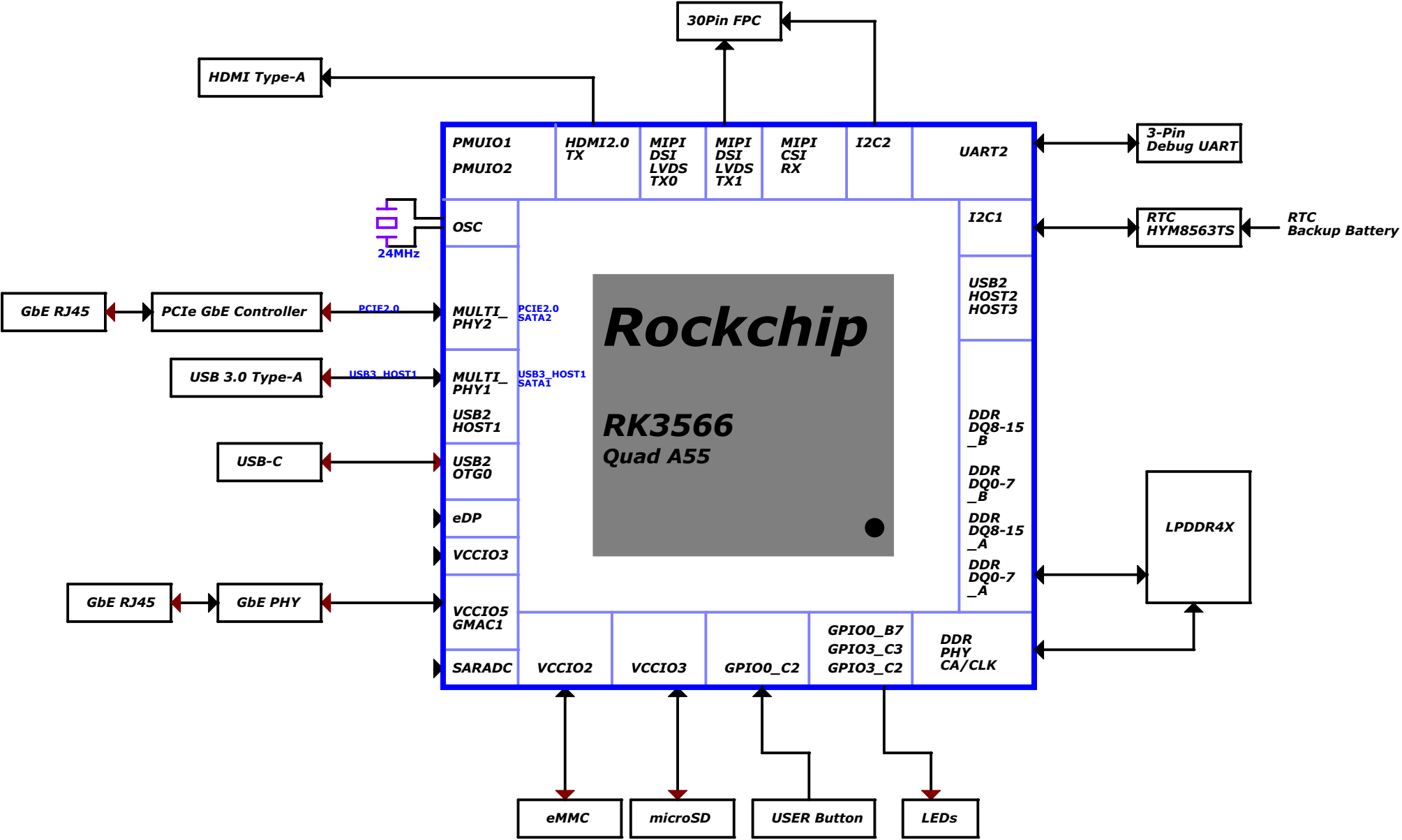
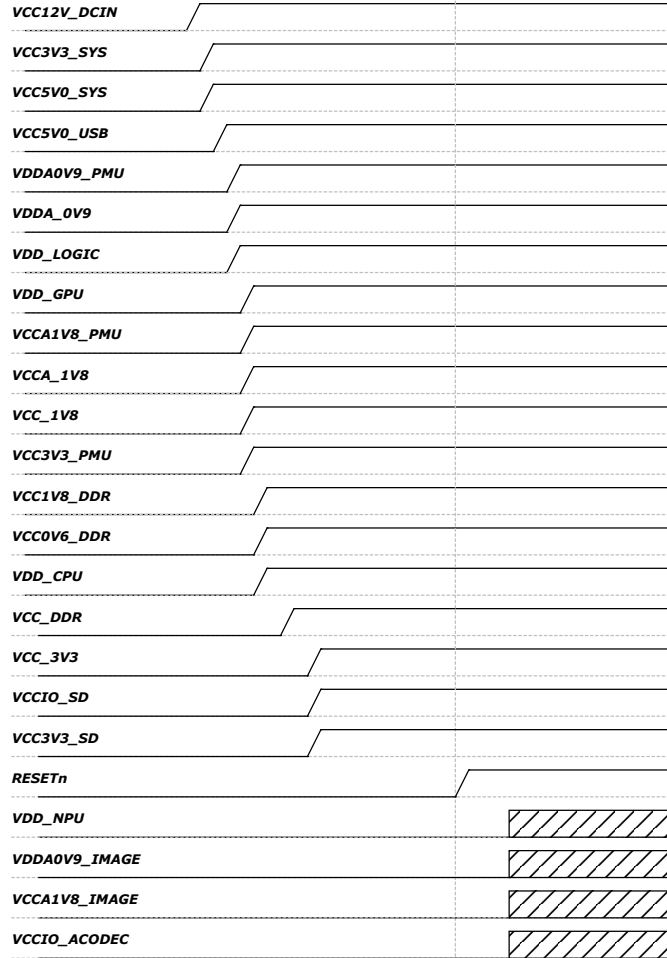


NanoPi R3S LTS



Power Sequence

&Power Path assignment



Power Source	PMIC Channel	Supply Limit	Power Supply Name	Time Slot	Default Voltage	Work Status	Sleep Status
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	OFF
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	--/0.9V	OFF	OFF
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	--/0.9V	OFF	OFF
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	--/3.3V	OFF	OFF
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	OFF
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	--/1.8V	OFF	OFF
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	OFF
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	OFF
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	OFF
	RK809_RESETh			Slot:4+5			
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	ON
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	ON
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF

IO Power Domain Map

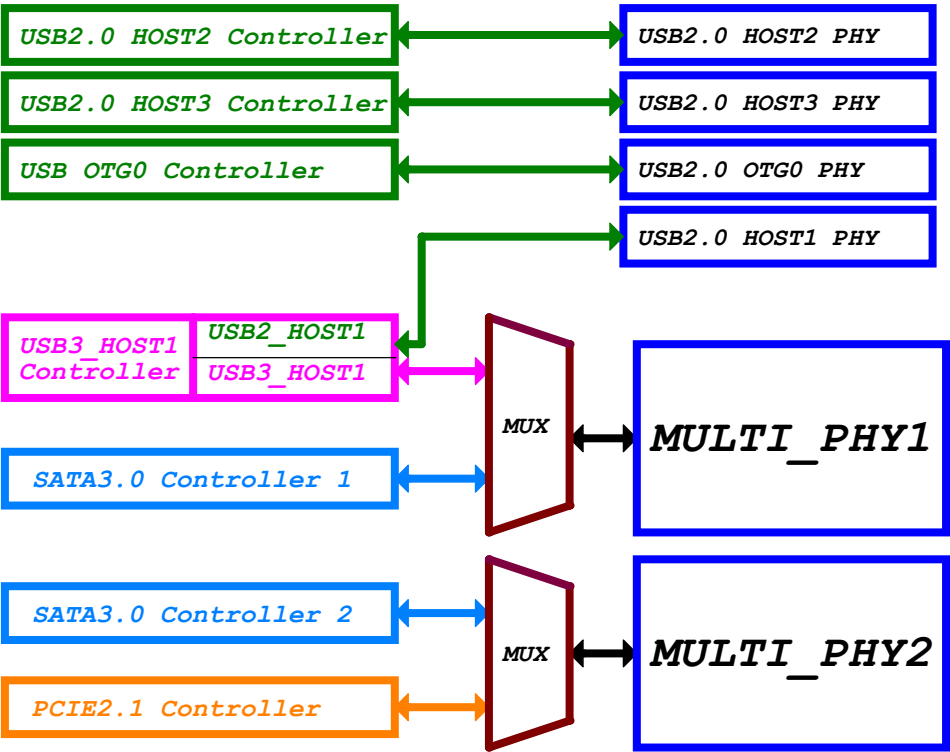
Refer to the actual design!

IO Domain	Pin Num	Support IO Voltage		Assignment IO Domain Voltage		Voltage	Notes
		3.3V	1.8V	Supply Power Net Name	Power Source		
PMUIO1	1P16	YES	NO	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	1N15	YES	YES	VCC3V3_PMU	VCC3V3_PMU	3.3V	3.3V as default, dts config should follow the HW design
VCCIO1	1D13	YES	YES	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	1C13	YES	YES	VCCIO_FLASH	VCC_1V8	1.8V	FLASH_VOL_SEL = 1 --> VCCIO_FLASH = 1.8V
VCCIO3	1F17	YES	YES	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	1E16	YES	YES	VCCIO_WL	VCC_1V8	1.8V	
VCCIO5	1N5 1N6	YES	YES	VCCIO5	VCC_1V8	1.8V	VCC_1V8 as default, VCC_3V3 optional
VCCIO6	1L4 1L5	YES	YES	VCCIO6	VCC1V8_DVP	1.8V	VCC1V8_DVP as default, VCC_1V8 optional
VCCIO7	1N8	YES	YES	VCCIO7	VCC_3V3	3.3V	

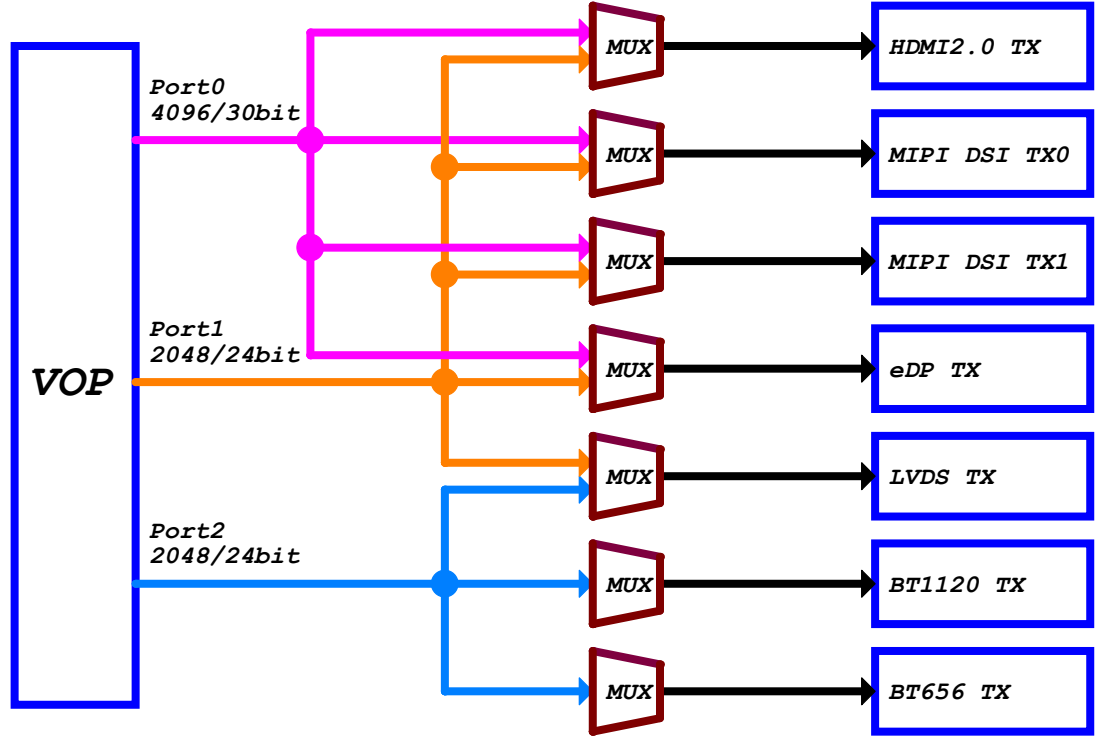
软件dts的电压配置严格与硬件设计保持一致！
Check the software configuration(dts)
of voltage level, which must be
keep the same as hardware design.

!!! Attention
注意

MULTI_PHY1/2 Path Map

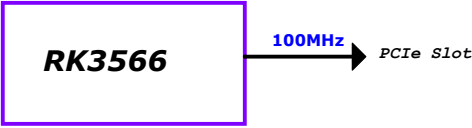


VOP Path Map



RK3566 support max to 2 output display ports ! !

PCIE2.1 REFCLK-RC Mode

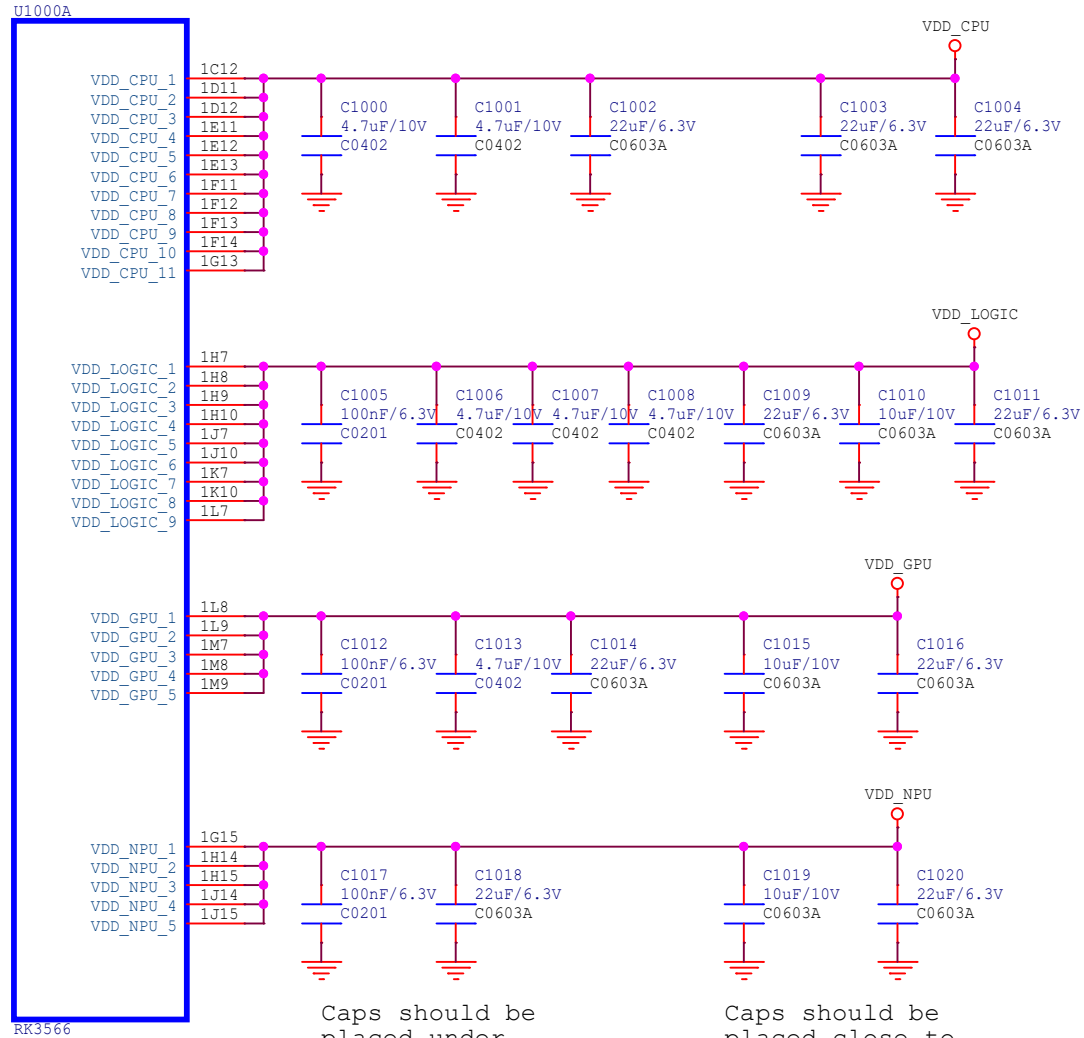


PCIE2.1 PHY

MULTI_PHY2	PCIE2.1 x1Lane	PCIE20_REFCLK (RC:output)	PCIE20_TX PCIE20_RX	PCIE20_CLKREQn PCIE20_WAKEn PCIE20_PERSTn PCIE20_BUTTONRSTn	Only RC
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RK3566_ABCDE

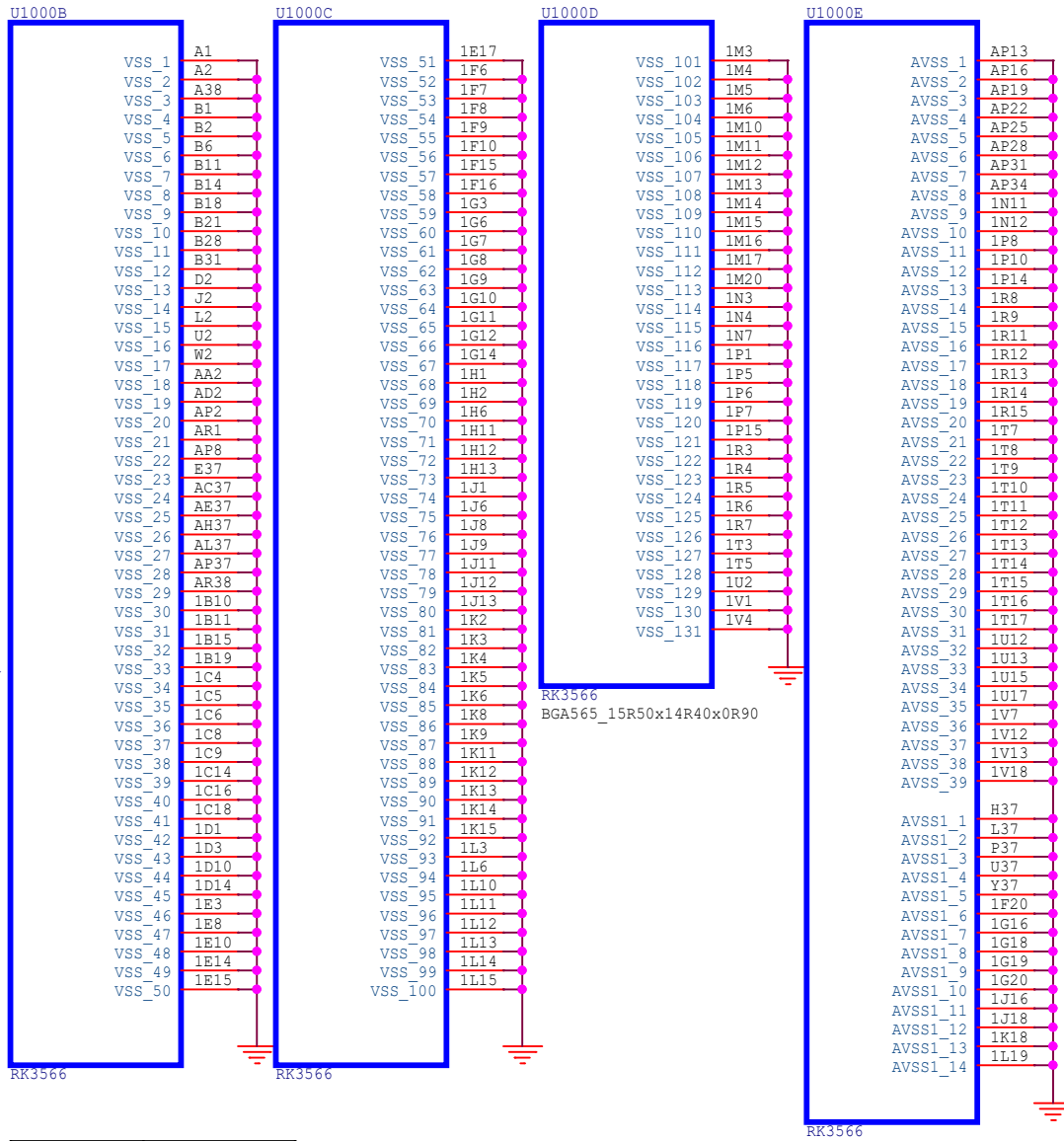
(Power&GND)



Caps should be placed under the U1000 package

Caps should be placed close to the U1000 package

VDD_CPU	3000mA
VDD_GPU	1200mA
VDD_NPU	1000mA
VDD_LOG	1200mA



<https://www.friendlyelec.com>
<https://wiki.friendlyelec.com>

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Size	Page Name	2411
A4	05.RK3566_Power/GND	
Date: Tuesday, October 29, 2024	Sheet: 5 / 21	

RK3566_F (DDR PHY)

U1000F

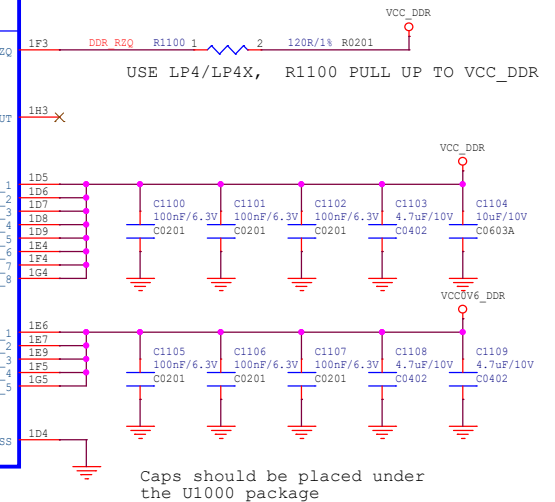
	DDR4	LPDDR4	DDR3	LPDDR3
[7] LPDDR4_DQ0_A	DDR DQ0 A G2	DDR DQ0 A / DDR4 DQ10 A / LPDDR4 DQ0 A / DDR3 DQ0 / LPDDR3 DQ15		
[7] LPDDR4_DQ1_A	DDR DQ1 A P2	DDR DQ1 A / DDR4 DQ12 A / LPDDR4 DQ1 A / DDR3 DQ1 / LPDDR3 DQ17		
[7] LPDDR4_DQ2_A	DDR DQ2 A P1	DDR DQ2 A / DDR4 DQ14 A / LPDDR4 DQ2 A / DDR3 DQ2 / LPDDR3 DQ19		
[7] LPDDR4_DQ3_A	DDR DQ3 A E1	DDR DQ3 A / DDR4 DQ16 A / LPDDR4 DQ3 A / DDR3 DQ3 / LPDDR3 DQ21		
[7] LPDDR4_DQ4_A	DDR DQ4 A M2	DDR DQ4 A / DDR4 DQ18 A / LPDDR4 DQ4 A / DDR3 DQ4 / LPDDR3 DQ23		
[7] LPDDR4_DQ5_A	DDR DQ5 A K1	DDR DQ5 A / DDR4 DQ20 A / LPDDR4 DQ5 A / DDR3 DQ5 / LPDDR3 DQ25		
[7] LPDDR4_DQ6_A	DDR DQ6 A K2	DDR DQ6 A / DDR4 DQ22 A / LPDDR4 DQ6 A / DDR3 DQ6 / LPDDR3 DQ27		
[7] LPDDR4_DQ7_A	DDR DQ7 A 1E1	DDR DQ7 A / DDR4 DQ24 A / LPDDR4 DQ7 A / DDR3 DQ7 / LPDDR3 DQ29		
[7] LPDDR4_DM0_A	DDR DM0 A 1E2	DDR DM0 A / DDR4 DM1 A / LPDDR4 DM0 A / DDR3 DM0 / LPDDR3 DM1		
[7] LPDDR4_DQS0P_A	DDR DQS0P A H2	DDR DQS0P A / DDR4 DQSL P A / LPDDR4 DQS0P A / DDR3 DQS0P / LPDDR3 DQS1P		
[7] LPDDR4_DQS0N_A	DDR DQS0N A H1	DDR DQS0N A / DDR4 DQSL N A / LPDDR4 DQS0N A / DDR3 DQS0N / LPDDR3 DQS1N		
[7] LPDDR4_DQ8_A	DDR DQ8 A P2	DDR DQ8 A / DDR4 DQ03 A / LPDDR4 DQ8 A / DDR3 DQ8 / LPDDR3 DQ25		
[7] LPDDR4_DQ9_A	DDR DQ9 A R1	DDR DQ9 A / DDR4 DQ01 A / LPDDR4 DQ9 A / DDR3 DQ9 / LPDDR3 DQ27		
[7] LPDDR4_DQ10_A	DDR DQ10 A R2	DDR DQ10 A / DDR4 DQ07 A / LPDDR4 DQ10 A / DDR3 DQ10 / LPDDR3 DQ29		
[7] LPDDR4_DQ11_A	DDR DQ11 A T2	DDR DQ11 A / DDR4 DQ05 A / LPDDR4 DQ11 A / DDR3 DQ11 / LPDDR3 DQ31		
[7] LPDDR4_DQ12_A	DDR DQ12 A M1	DDR DQ12 A / DDR4 DQ02 A / LPDDR4 DQ12 A / DDR3 DQ12 / LPDDR3 DQ33		
[7] LPDDR4_DQ13_A	DDR DQ13 A 1F1	DDR DQ13 A / DDR4 DQ04 A / LPDDR4 DQ13 A / DDR3 DQ13 / LPDDR3 DQ35		
[7] LPDDR4_DQ14_A	DDR DQ14 A 1F2	DDR DQ14 A / DDR4 DQ06 A / LPDDR4 DQ14 A / DDR3 DQ14 / LPDDR3 DQ37		
[7] LPDDR4_DQ15_A	DDR DQ15 A 1G2	DDR DQ15 A / DDR4 DQ08 A / LPDDR4 DQ15 A / DDR3 DQ15 / LPDDR3 DQ39		
[7] LPDDR4_DM1_A	DDR DM1 A 1G1	DDR DM1 A / DDR4 DM0 A / LPDDR4 DM1 A / DDR3 DM1 / LPDDR3 DM3		
[7] LPDDR4_DQS1P_A	DDR DQS1P A N1	DDR DQS1P A / DDR4 DQSU P A / LPDDR4 DQS1P A / DDR3 DQS1P / LPDDR3 DQS3P		
[7] LPDDR4_DQS1N_A	DDR DQS1N A N2	DDR DQS1N A / DDR4 DQSU N A / LPDDR4 DQS1N A / DDR3 DQS1N / LPDDR3 DQS3N		
[7] LPDDR4_DQ0_B	DDR DQ0 B B12	DDR DQ0 B / DDR4 DQ07 B / LPDDR4 DQ0 B / DDR3 DQ16 / LPDDR3 DQ1		
[7] LPDDR4_DQ1_B	DDR DQ1 B B10	DDR DQ1 B / DDR4 DQ09 B / LPDDR4 DQ1 B / DDR3 DQ17 / LPDDR3 DQ3		
[7] LPDDR4_DQ2_B	DDR DQ2 B 1A8	DDR DQ2 B / DDR4 DQ03 B / LPDDR4 DQ2 B / DDR3 DQ18 / LPDDR3 DQ5		
[7] LPDDR4_DQ3_B	DDR DQ3 B 1A7	DDR DQ3 B / DDR4 DQ01 B / LPDDR4 DQ3 B / DDR3 DQ19 / LPDDR3 DQ7		
[7] LPDDR4_DQ4_B	DDR DQ4 B B13	DDR DQ4 B / DDR4 DQ05 B / LPDDR4 DQ4 B / DDR3 DQ20 / LPDDR3 DQ9		
[7] LPDDR4_DQ5_B	DDR DQ5 B 1A10	DDR DQ5 B / DDR4 DQ02 B / LPDDR4 DQ5 B / DDR3 DQ21 / LPDDR3 DQ11		
[7] LPDDR4_DQ6_B	DDR DQ6 B 1B9	DDR DQ6 B / DDR4 DQ04 B / LPDDR4 DQ6 B / DDR3 DQ22 / LPDDR3 DQ13		
[7] LPDDR4_DQ7_B	DDR DQ7 B 1A9	DDR DQ7 B / DDR4 DQ06 B / LPDDR4 DQ7 B / DDR3 DQ23 / LPDDR3 DQ15		
[7] LPDDR4_DM0_B	DDR DM0 B 1B8	DDR DM0 B / DDR4 DM0 B / LPDDR4 DM0 B / DDR3 DM2 / LPDDR3 DM0		
[7] LPDDR4_DQS0P_B	DDR DQS0P B A13	DDR DQS0P B / DDR4 DQSU P B / LPDDR4 DQS0P B / DDR3 DQS2P / LPDDR3 DQS0P		
[7] LPDDR4_DQS0N_B	DDR DQS0N B A12	DDR DQS0N B / DDR4 DQSU N B / LPDDR4 DQS0N B / DDR3 DQS2N / LPDDR3 DQS0N		
[7] LPDDR4_DQ8_B	DDR DQ8 B B19	DDR DQ8 B / DDR4 DQ10 B / LPDDR4 DQ8 B / DDR3 DQ24 / LPDDR3 DQ18 D2		
[7] LPDDR4_DQ9_B	DDR DQ9 B A19	DDR DQ9 B / DDR4 DQ12 B / LPDDR4 DQ9 B / DDR3 DQ25 / LPDDR3 DQ19 D3		
[7] LPDDR4_DQ10_B	DDR DQ10 B A20	DDR DQ10 B / DDR4 DQ14 B / LPDDR4 DQ10 B / DDR3 DQ26 / LPDDR3 DQ21 D6		
[7] LPDDR4_DQ11_B	DDR DQ11 B B20	DDR DQ11 B / DDR4 DQ16 B / LPDDR4 DQ11 B / DDR3 DQ27 / LPDDR3 DQ23 D9		
[7] LPDDR4_DQ12_B	DDR DQ12 B A15	DDR DQ12 B / DDR4 DQ18 B / LPDDR4 DQ12 B / DDR3 DQ28 / LPDDR3 DQ25 D4		
[7] LPDDR4_DQ13_B	DDR DQ13 B B15	DDR DQ13 B / DDR4 DQ20 B / LPDDR4 DQ13 B / DDR3 DQ29 / LPDDR3 DQ27 D6		
[7] LPDDR4_DQ14_B	DDR DQ14 B 1C10	DDR DQ14 B / DDR4 DQ03 B / LPDDR4 DQ14 B / DDR3 DQ30 / LPDDR3 DQ29 D8		
[7] LPDDR4_DQ15_B	DDR DQ15 B B16	DDR DQ15 B / DDR4 DQ05 B / LPDDR4 DQ15 B / DDR3 DQ31 / LPDDR3 DQ31 D5		
[7] LPDDR4_DM1_B	DDR DM1 B 1A11	DDR DM1 B / DDR4 DM1 B / LPDDR4 DM1 B / DDR3 DM3 / LPDDR3 DM2		
[7] LPDDR4_DQS1P_B	DDR DQS1P B A17	DDR DQS1P B / DDR4 DQSL P B / LPDDR4 DQS1P B / DDR3 DQS3P / LPDDR3 DQS2P		
[7] LPDDR4_DQS1N_B	DDR DQS1N B B17	DDR DQS1N B / DDR4 DQSL N B / LPDDR4 DQS1N B / DDR3 DQS3N / LPDDR3 DQS2N		

Note:
Except DDR3, other DQ sequences
can not be swap

DDR4	LPDDR4	DDR3	LPDDR3
DDR4 A0	LPDDR4 CLKP_B	DDR3 A9	---
DDR4 A1	---	DDR3 A2	---
DDR4 A2	LPDDR4 A1_A	DDR3 A6	---
DDR4 A3	LPDDR4 CKE1_A	DDR3 A3	---
DDR4 A4	LPDDR4 A3_B	DDR3 BA1	---
DDR4 A5	LPDDR4 A5_B	DDR3 A11	---
DDR4 A6	LPDDR4 A1_B	DDR3 A13	---
DDR4 A7	LPDDR4 OD70_CA_B	DDR3 A5	---
DDR4 A8	LPDDR4 OD70_CA_A	DDR3 A6	---
DDR4 A9	LPDDR4 CLKN_B	DDR3 A9	---
DDR4 A10	LPDDR4 CKE0_B	DDR3 A8	---
DDR4 A11	LPDDR4 A0_A	DDR3 A8	---
DDR4 A12	LPDDR4 A3_A	DDR3 BA2	---
DDR4 A13	LPDDR4 A0_B	DDR3 A14	---
DDR4 A14	LPDDR4 A4_A	DDR3 A15	---
DDR4 A15 CASn	LPDDR4 A2_A	DDR3 A2	---
DDR4 A16 RASn	LPDDR4 A5_A	DDR3 RASn	---
DDR4 ACTn	LPDDR4 CKE1_B	DDR3 CASn	---
DDR4 BA0	LPDDR4 A7_B	DDR3 A1	---
DDR4 BA1	LPDDR4 A4_B	DDR3 A12	---
DDR4 BG0	LPDDR4 OD71_CA_B	---	---
DDR4 BG1	LPDDR4 OD71_CA_A	---	---
DDR4 CKE	LPDDR4 CKE0_A	---	---
DDR4 CLKP	LPDDR4 CLKP_A	DDR3 CLKP	---
DDR4 CLKN	LPDDR4 CLKN_A	DDR3 CLKN	---
DDR4 CS0n	LPDDR4 CS0n_A	DDR3 OD71	---
DDR4 CS1n	LPDDR4 CS1n_A	DDR3 CS1n	---
DDR4 OD70	LPDDR4 CS1n_B	DDR3 OD70	---
DDR4 OD71	LPDDR4 CS0n_B	DDR3 CS0n	---
DDR4 RESETn	LPDDR4 RESETn	DDR3 RESETn	---

Note: Sequences can not be swap

A7	LPDDR4_CLKP_B	[7]
1D2	LPDDR4_A1_A	[7]
C1	LPDDR4_CKE1_A	[7]
1C3	LPDDR4_A3_B	[7]
1B6	LPDDR4_A5_B	[7]
B8	LPDDR4_A1_B	[7]
B9	LPDDR4_OD70_CA_B	[7]
A10	LPDDR4_OD70_CA_A	[7]
E2	LPDDR4_CLKN_B	[7]
B7	LPDDR4_CKE0_B	[7]
1A3	LPDDR4_A0_A	[7]
C2	LPDDR4_A3_A	[7]
1B3	LPDDR4_A0_B	[7]
A9	LPDDR4_A4_A	[7]
1B1	LPDDR4_A2_A	[7]
1C1	LPDDR4_A5_A	[7]
1A1	LPDDR4_CKE1_B	[7]
1A2	LPDDR4_A2_B	[7]
1A6	LPDDR4_A4_B	[7]
1A4	LPDDR4_CLKP_A	[7]
1C2	LPDDR4_CLKN_A	[7]
B4	LPDDR4_CS0n_A	[7]
A5	LPDDR4_CS1n_A	[7]
B5	LPDDR4_CS1n_B	[7]
B3	LPDDR4_CS0n_B	[7]
A3	LPDDR4_RESETn	[7]
1B5	LPDDR4_RESETn	[7]
1C7	LPDDR4_RESETn	[7]



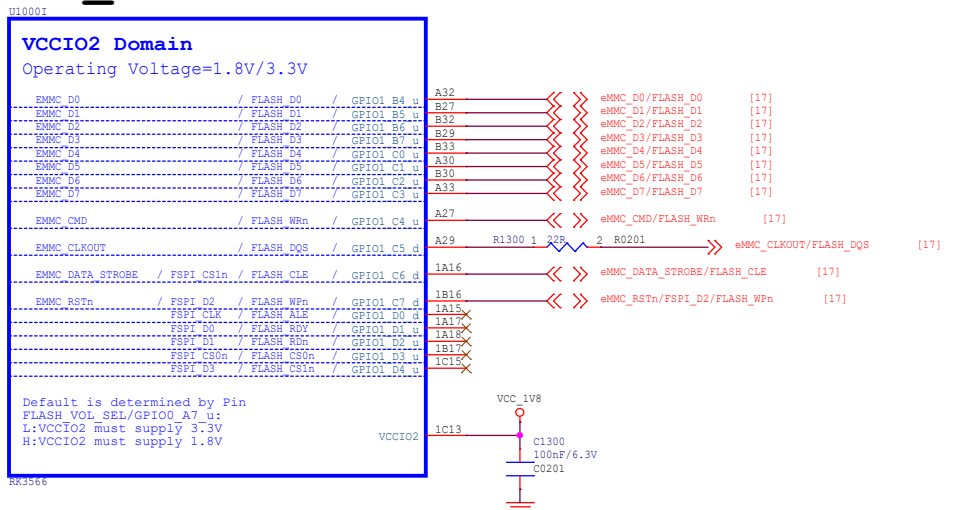
Caps should be placed under the U1000 package

PMUI01/2/OSC Domain Logic Power
Operating Voltage=0.9V

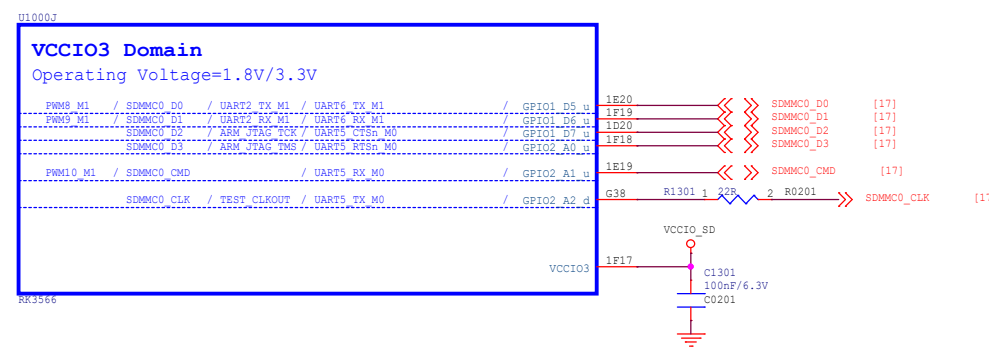
Caps should be placed under the U1000 package

Caps should be placed close to the U1000 package

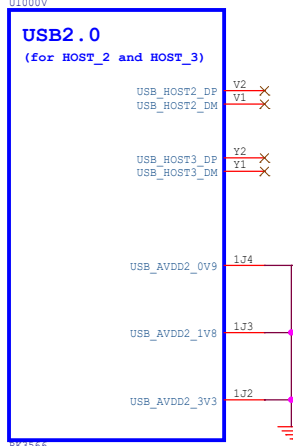
5
RK3566_1 (VCCIO2 Domain)⁴



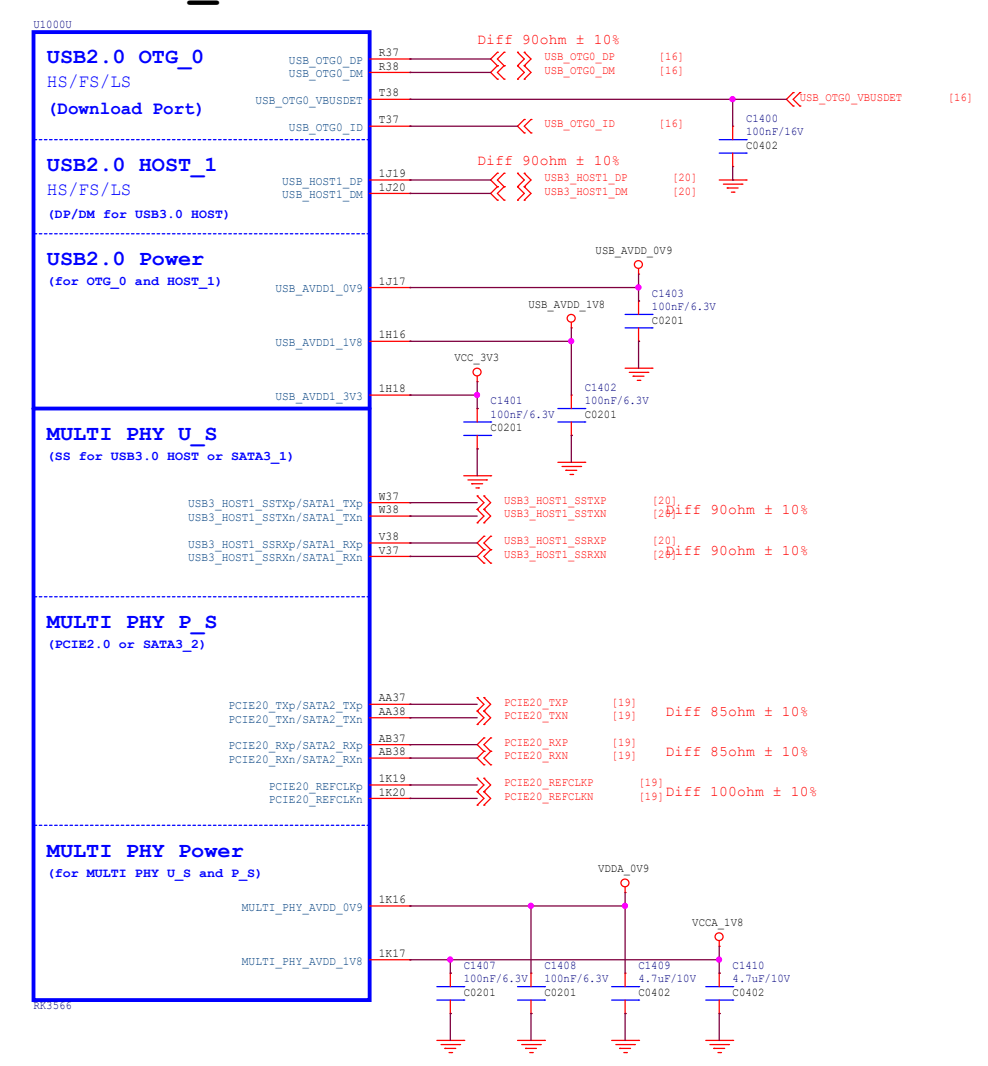
CRK3566_J (VCCIO3 Domain)

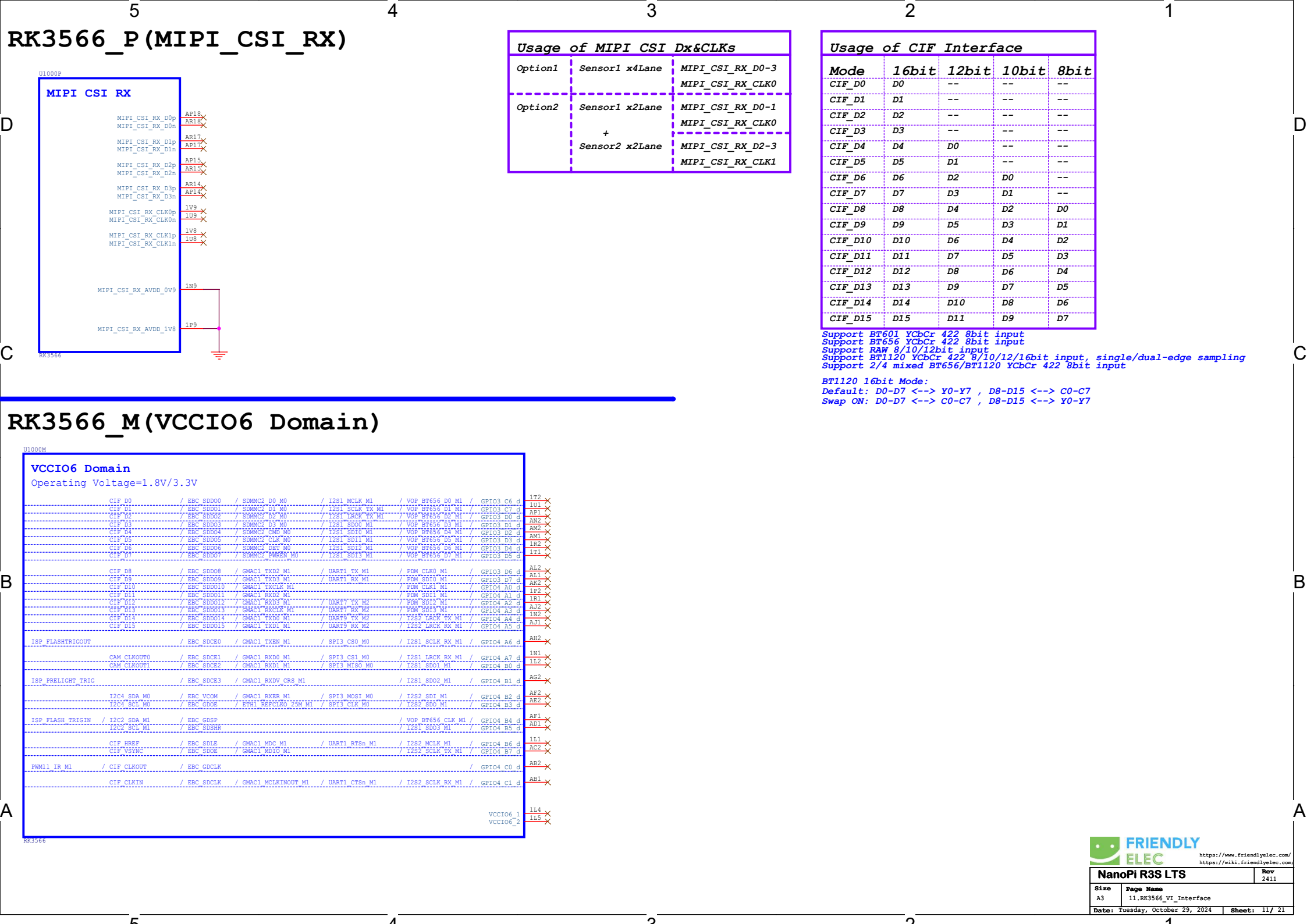


B
RK3566_V (USB2.0 HOST)



1
RK3566_U (USB3.0/PCIE2.0x1/SATA)¹

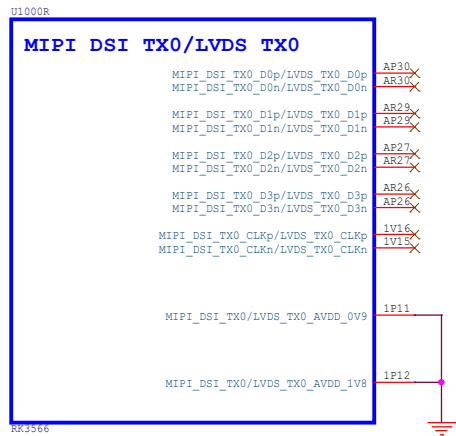




5 4

RK3566_R (MIPI_DSI_TX0/LVDS_TX0)

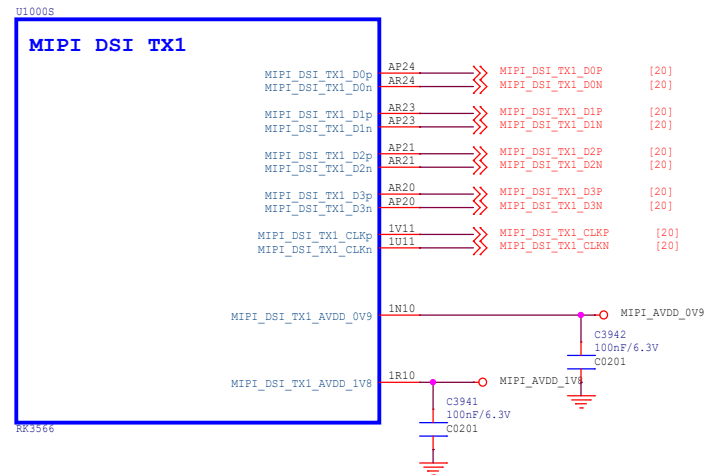
D



3 2 1

RK3566_S (MIPI_DSI_TX1)

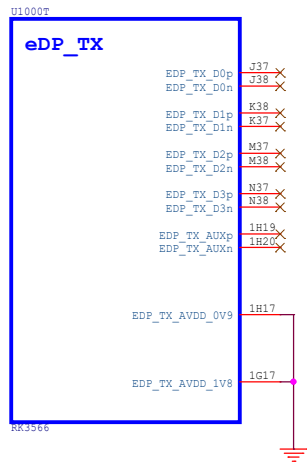
D



C

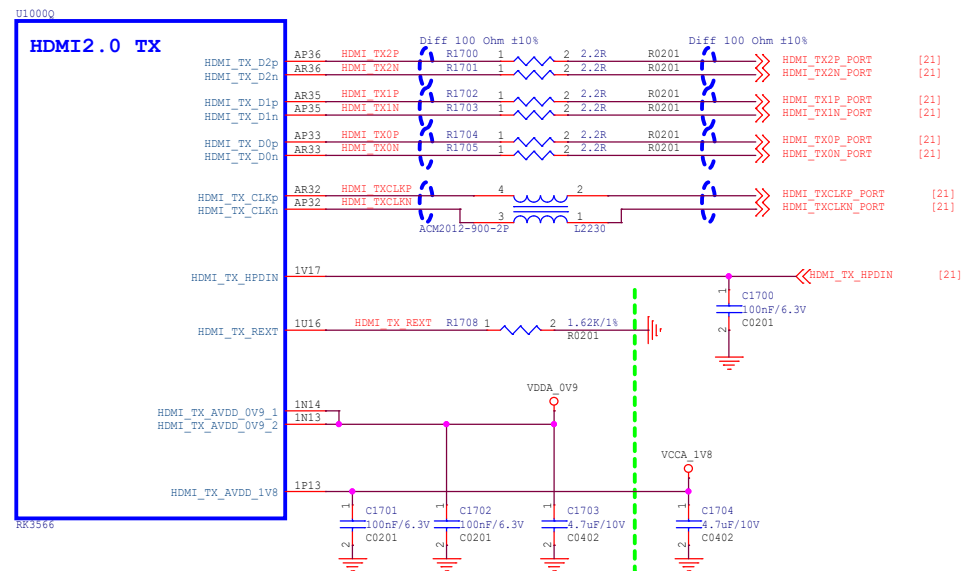
RK3566_T (eDP TX)

B

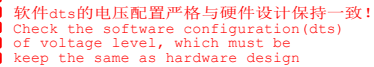


RK3566_Q (HDMI2.0 TX)

B

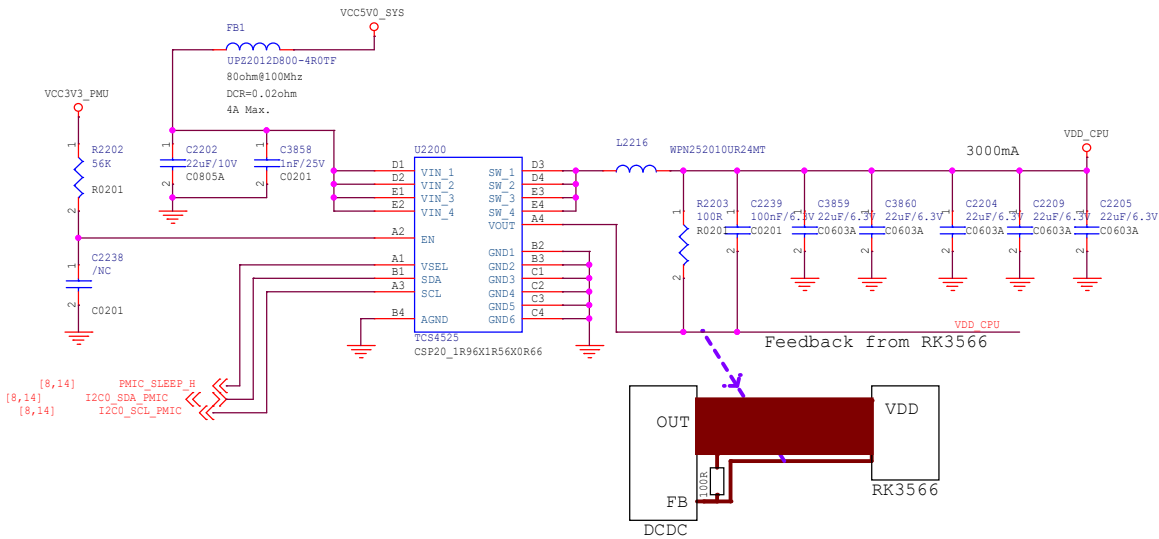


A

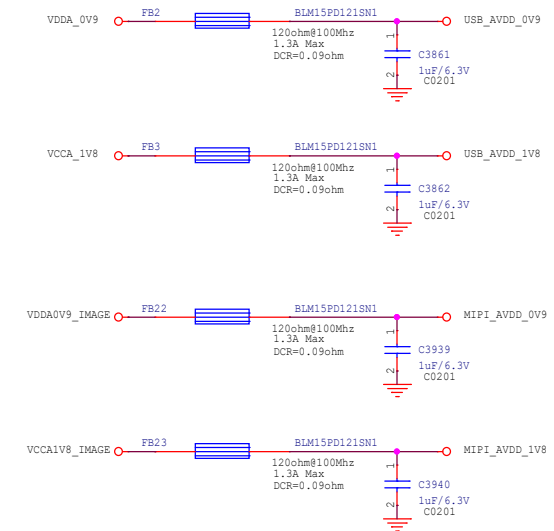


<i>GMAC</i>	<i>Direction</i>	<i>GEPHY</i>	<i>GMAC</i>	<i>Direction</i>	<i>FEPHY</i>
<i>GMACx_TXD0</i>	<i>-----></i>	<i>PHYx_TXD0</i>	<i>GMACx_TXD0</i>	<i>-----></i>	<i>PHYx_TXD0</i>
<i>GMACx_TXD1</i>	<i>-----></i>	<i>PHYx_TXD1</i>	<i>GMACx_TXD1</i>	<i>-----></i>	<i>PHYx_TXD1</i>
<i>GMACx_TXD2</i>	<i>-----></i>	<i>PHYx_TXD2</i>			
<i>GMACx_TXD3</i>	<i>-----></i>	<i>PHYx_TXD3</i>			
<i>GMACx_TXEN</i>	<i>-----></i>	<i>PHYx_TXEN</i>	<i>GMACx_TXEN</i>	<i>-----></i>	<i>PHYx_TXEN</i>
<i>GMACx_TXCLK</i>	<i>-----></i>	<i>PHYx_TXCLK</i>			
<i>GMACx_RXD0</i>	<i><-----</i>	<i>PHYx_RXD0</i>	<i>GMACx_RXD0</i>	<i><-----</i>	<i>PHYx_RXD0</i>
<i>GMACx_RXD1</i>	<i><-----</i>	<i>PHYx_RXD1</i>	<i>GMACx_RXD1</i>	<i><-----</i>	<i>PHYx_RXD1</i>
<i>GMACx_RXD2</i>	<i><-----</i>	<i>PHYx_RXD2</i>			
<i>GMACx_RXD3</i>	<i><-----</i>	<i>PHYx_RXD3</i>			
<i>GMACx_RXDV</i>	<i><-----</i>	<i>PHYx_RXDV</i>	<i>GMACx_RXDV</i>	<i><-----</i>	<i>PHYx_CRS_DV</i>
<i>GMACx_RXCLK</i>	<i><-----</i>	<i>PHYx_RXCLK</i>			
<i>GMACx_RXER</i>			<i>GMACx_RXER</i>	<i><-----</i>	<i>PHYx_RXER</i>
<i>GMACx_MDC</i>	<i>-----></i>	<i>PHYx_MDC</i>	<i>GMACx_MDC</i>	<i>-----></i>	<i>PHYx_MDC</i>
<i>GMACx_MDIO</i>	<i><-----></i>	<i>PHYx_MDIO</i>	<i>GMACx_MDIO</i>	<i><-----></i>	<i>PHYx_MDIO</i>
<i>ETHx_REFCLK0_25M</i>	<i>-----></i>	<i>PHYx_XTALIN</i>			
<i>GMACx_MCLKINOUT</i>	<i><-----</i>	<i>PHYx_CLKOUT125 (Option)</i>	<i>GMACx_MCLKINOUT</i>	<i>-----></i>	<i>PHYx_XTALIN/REFCLK</i>
<i>GPIO</i>	<i>-----></i>	<i>PHYx_RSTn</i>	<i>GPIO</i>	<i>-----></i>	<i>PHYx_RSTn</i>
<i>GPIO</i>	<i><-----</i>	<i>PHYx_INT/PMEB</i>	<i>GPIO</i>	<i><-----</i>	<i>PHYx_INT/PMEB</i>

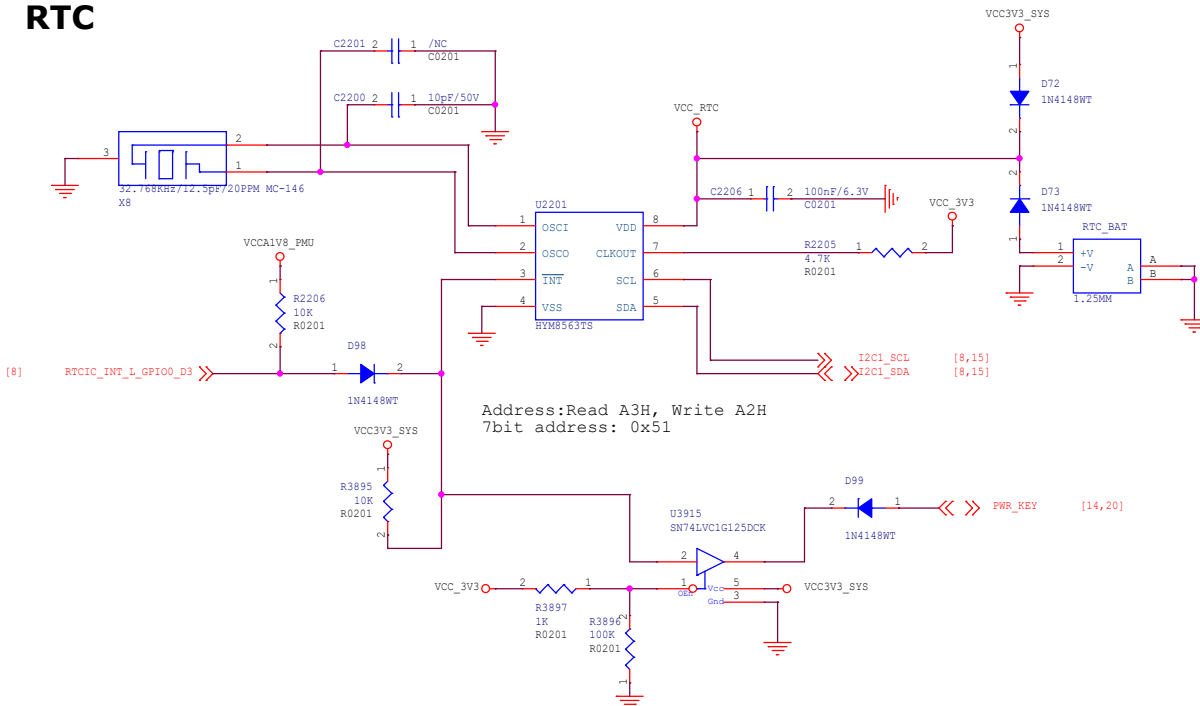
VDD_CPU



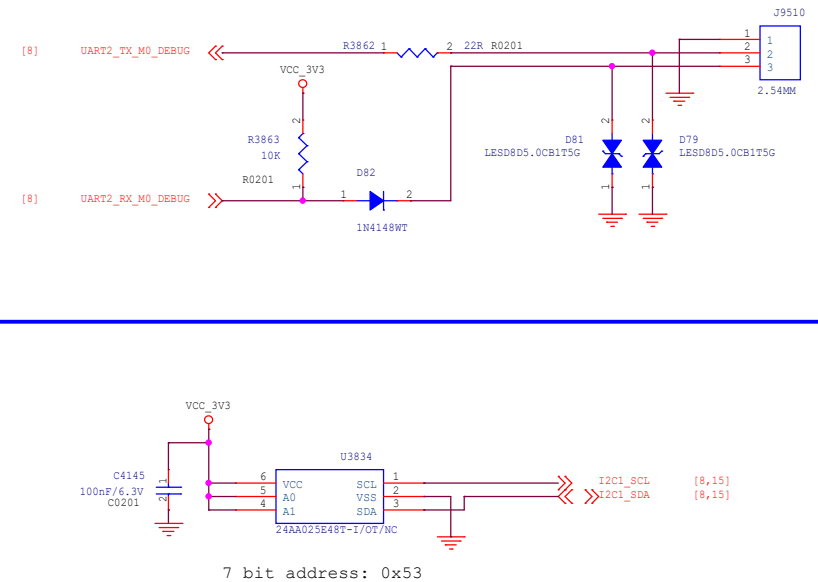
VDD_USB



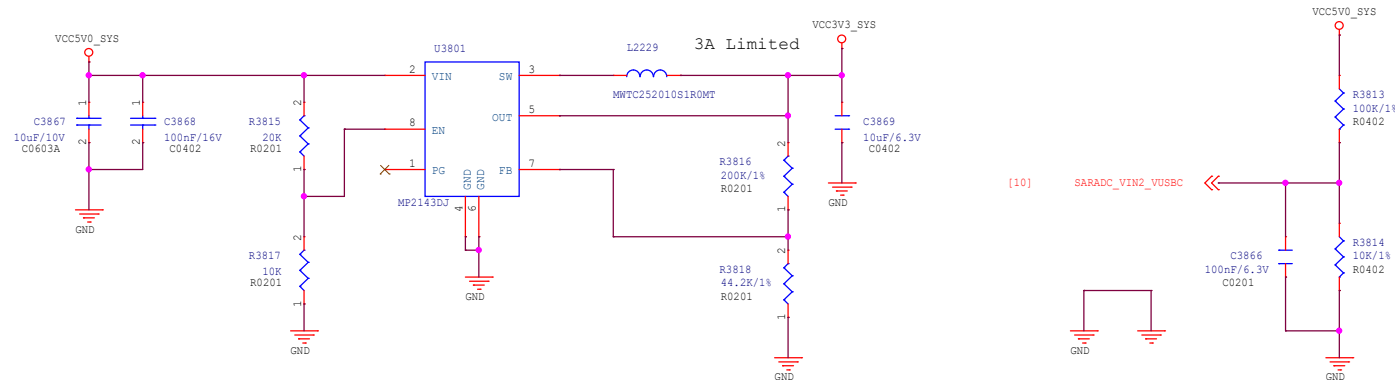
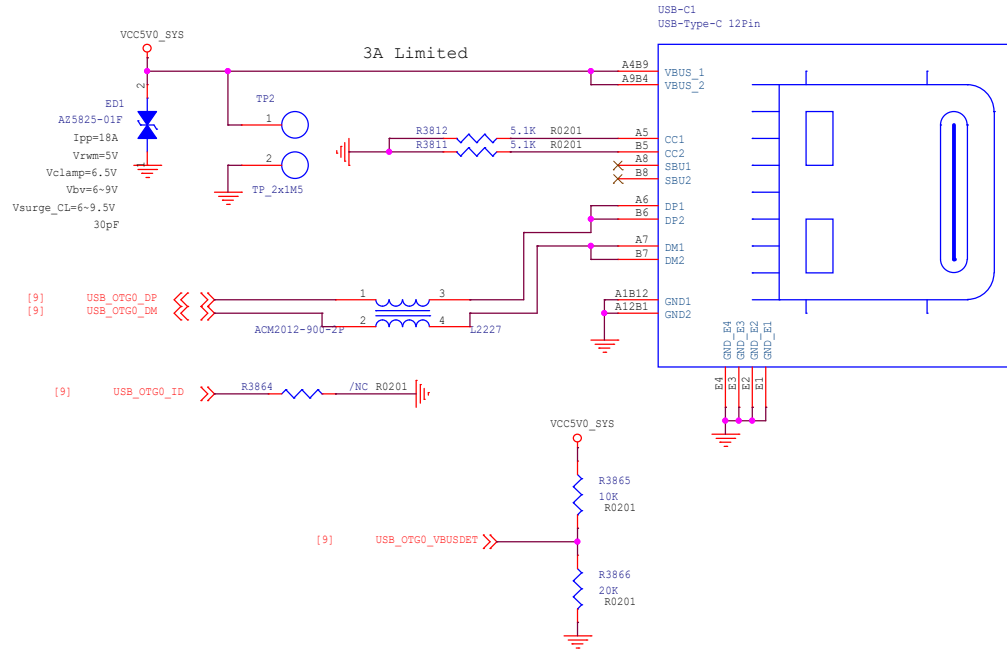
RTC



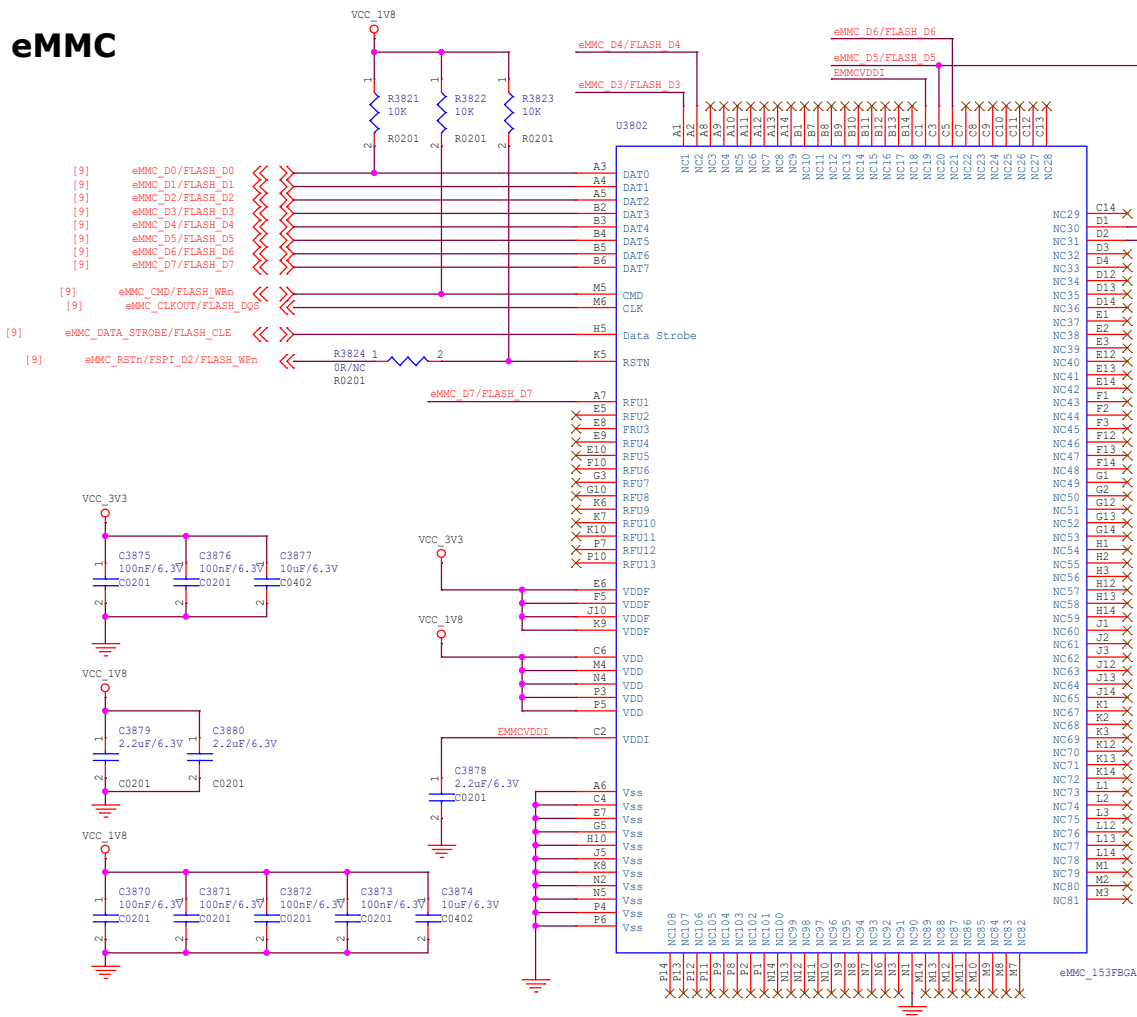
Debug UART



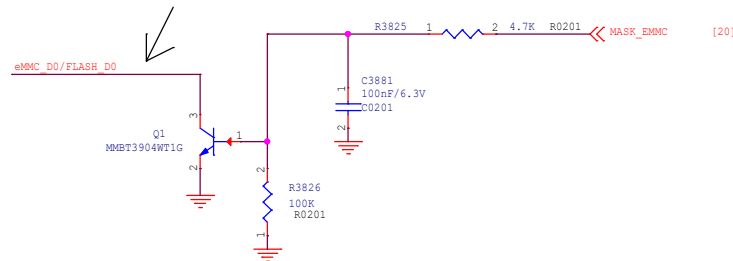
Power IN



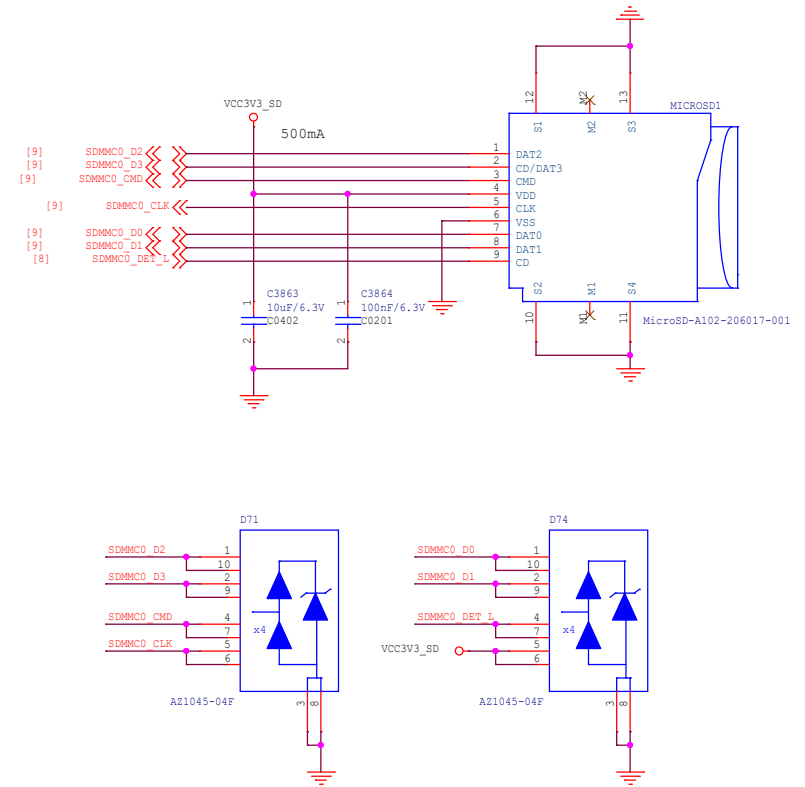
eMMC



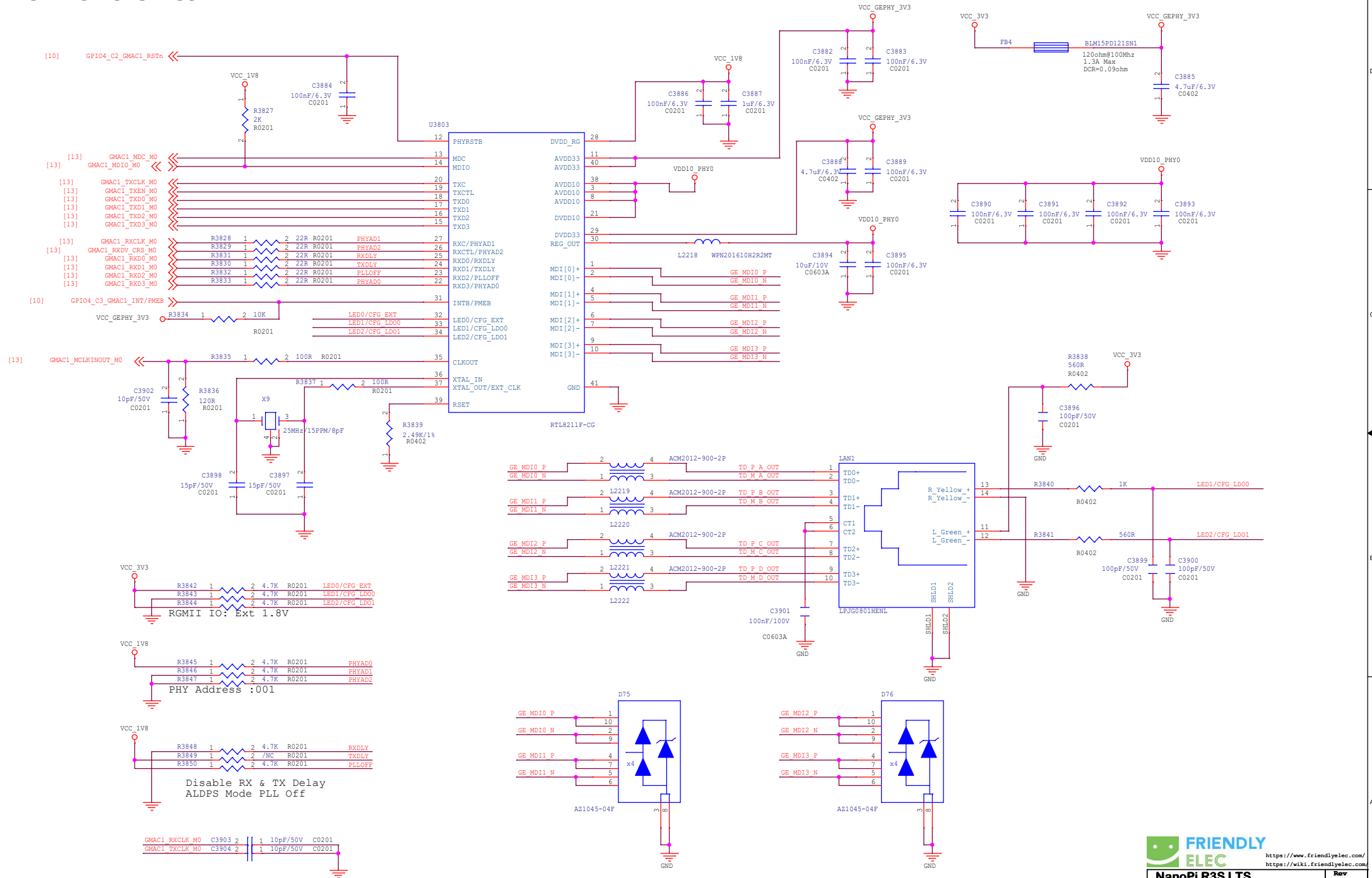
Stub as short as possible



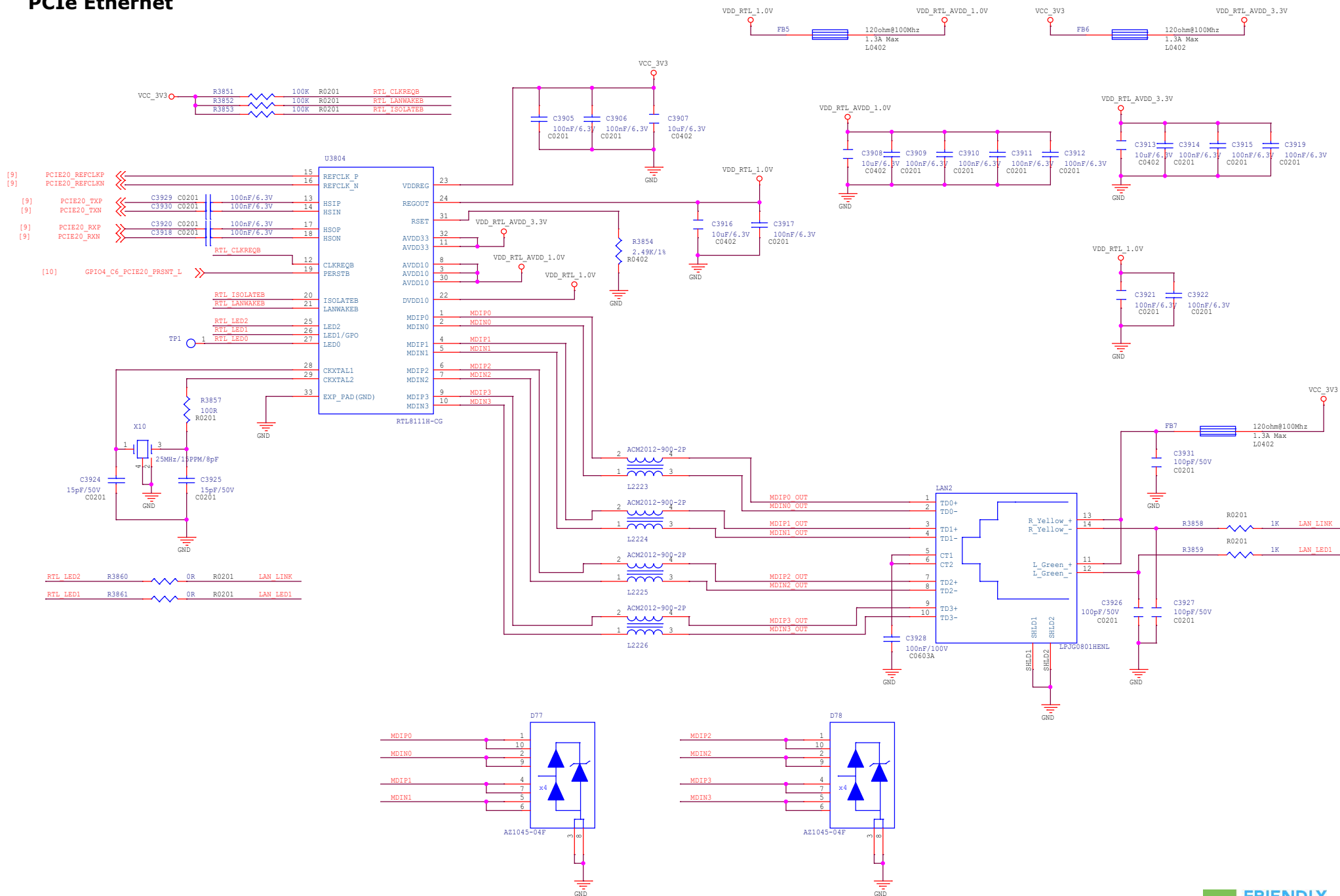
microSD



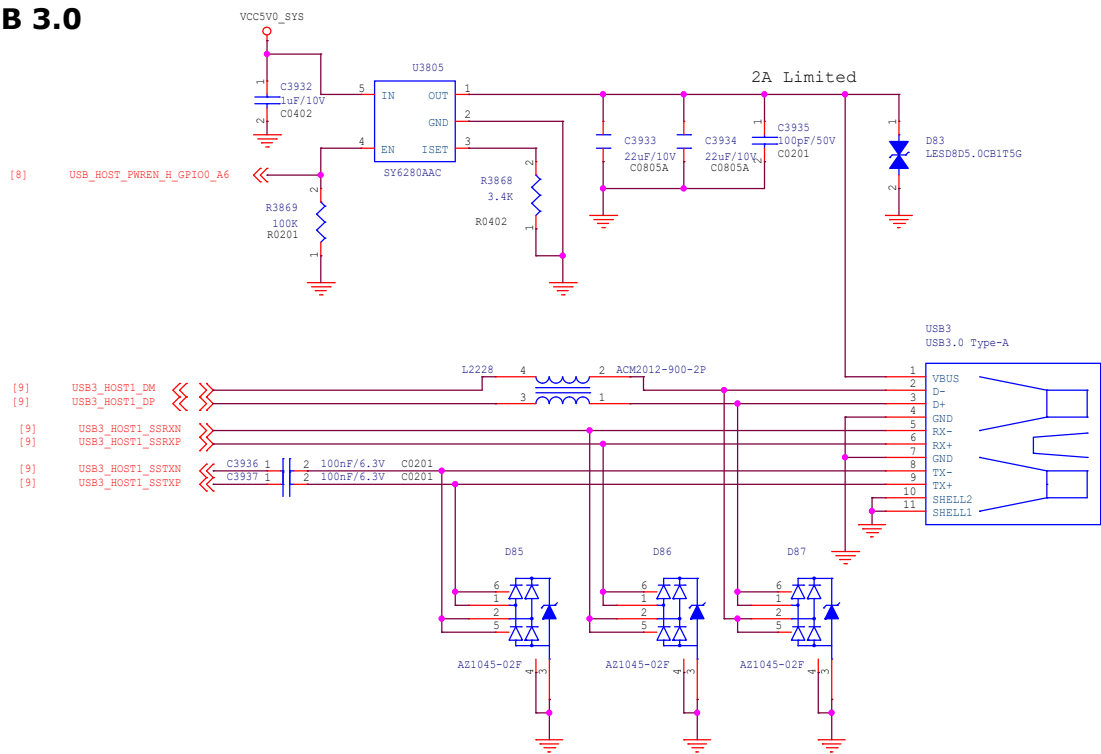
GMAC Ethernet



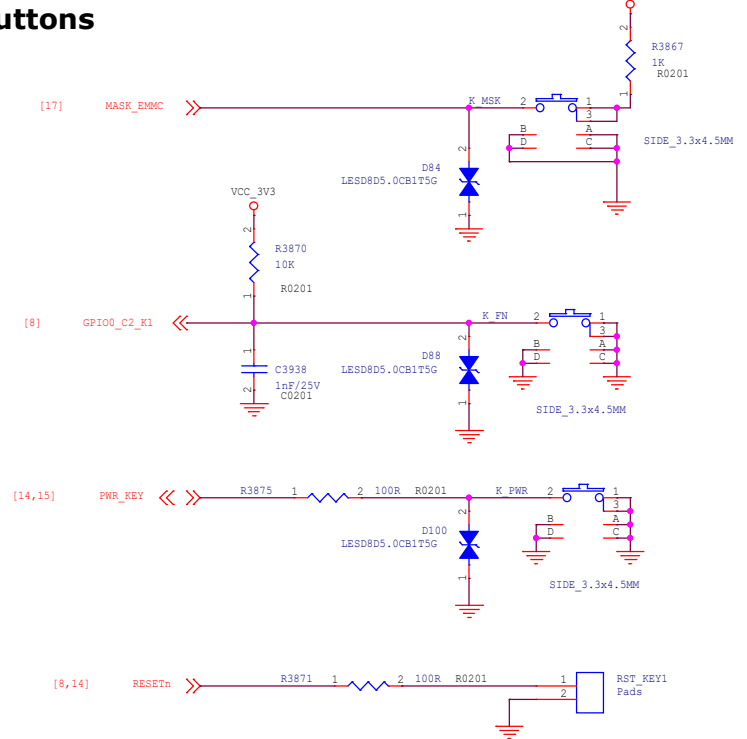
PCIe Ethernet



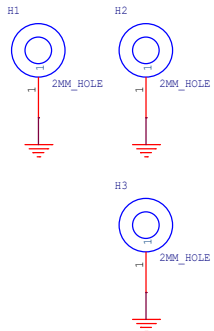
USB 3.0



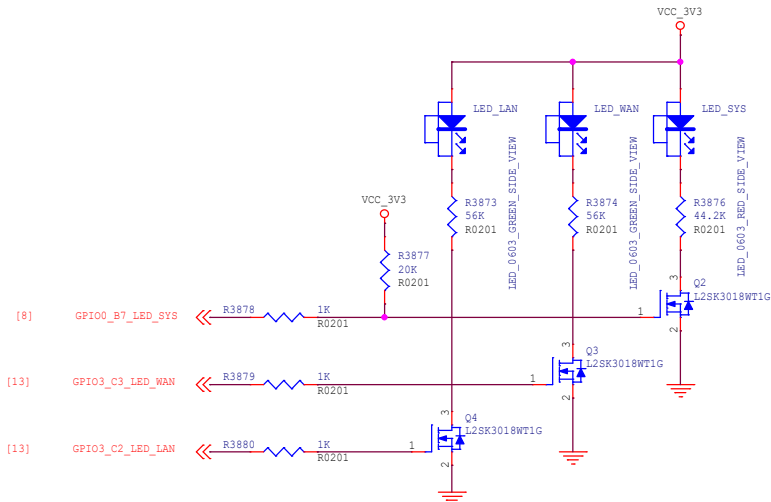
Buttons



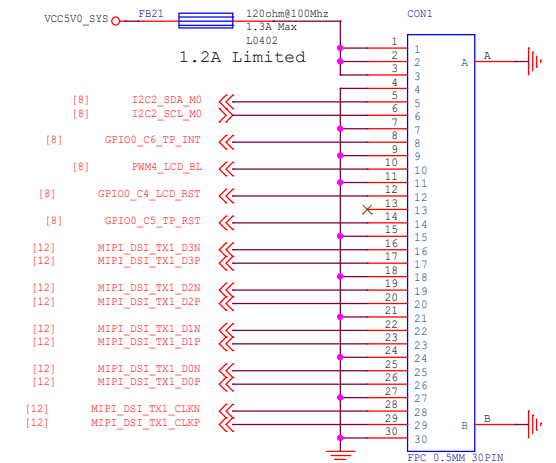
Screw Holes



LEDs



MIPI LCD



HDMI 2.0 TX

