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Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

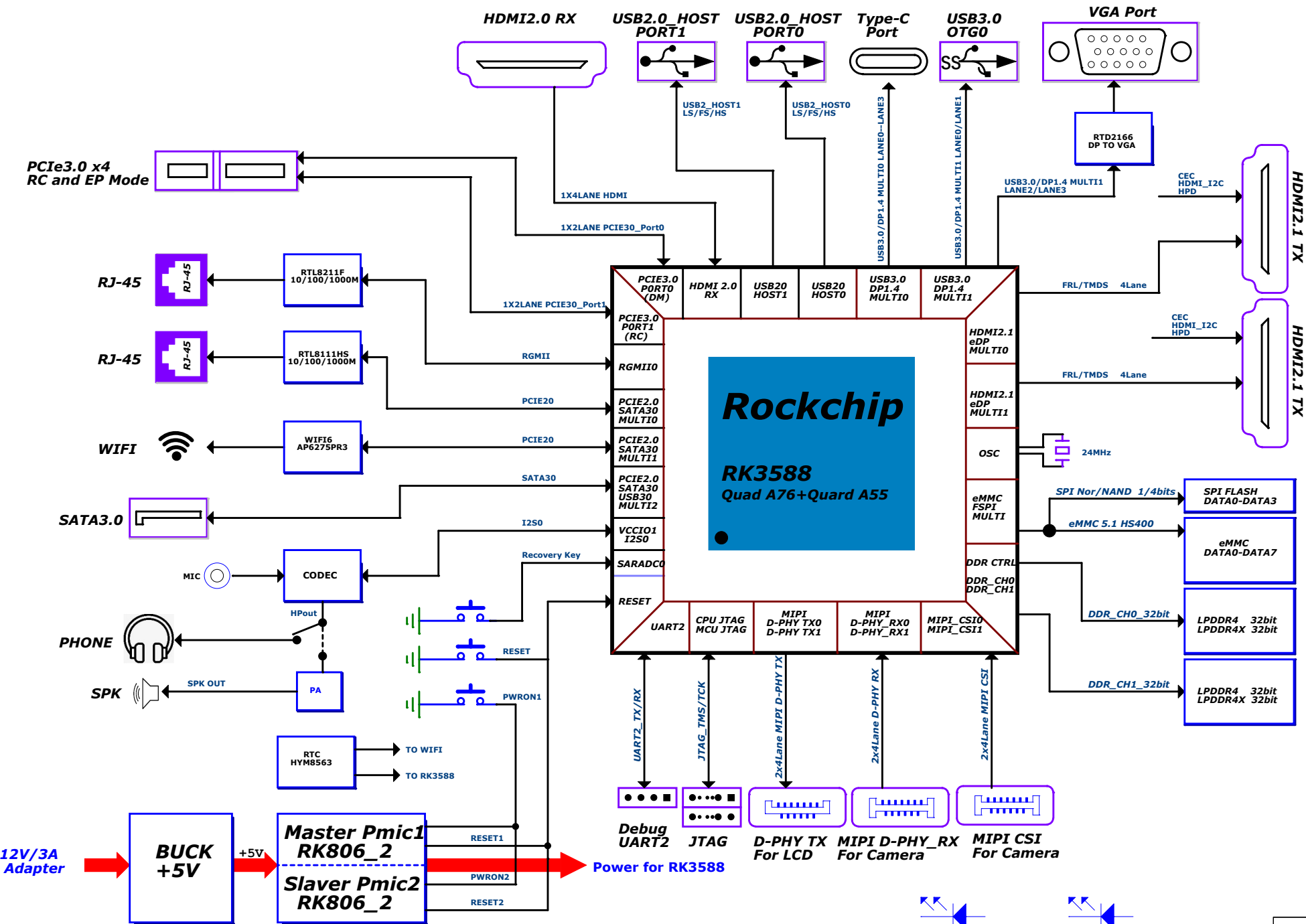
- NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted
- NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

HINLINK

Project:	H88K_V3.1	 HINLINK	
File:	01.Index and Notes		
Date:	Monday, May 06, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	1 of 43

RK3588 EVB1 Block Diagram

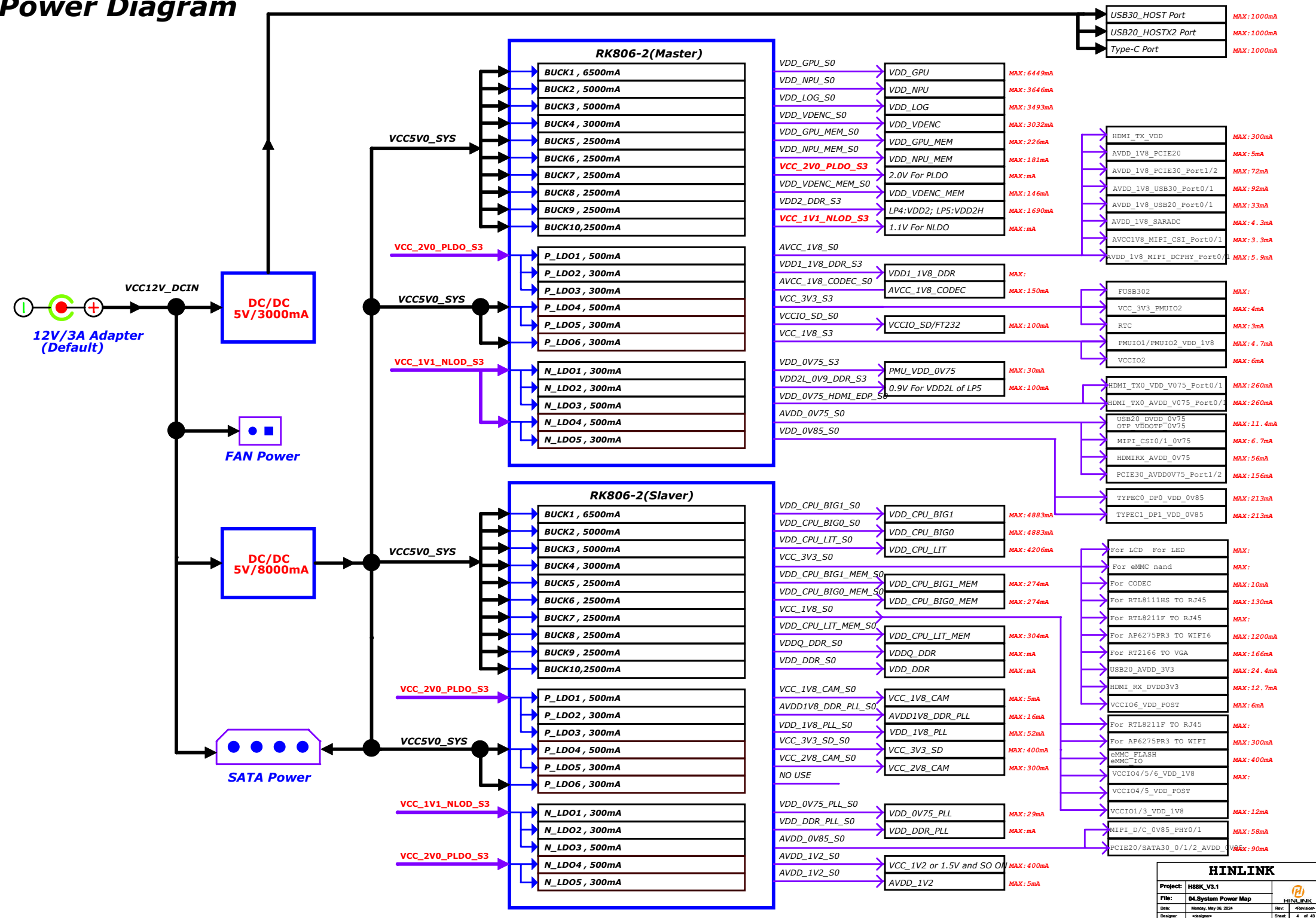
Mean to Interface
Mean to IC



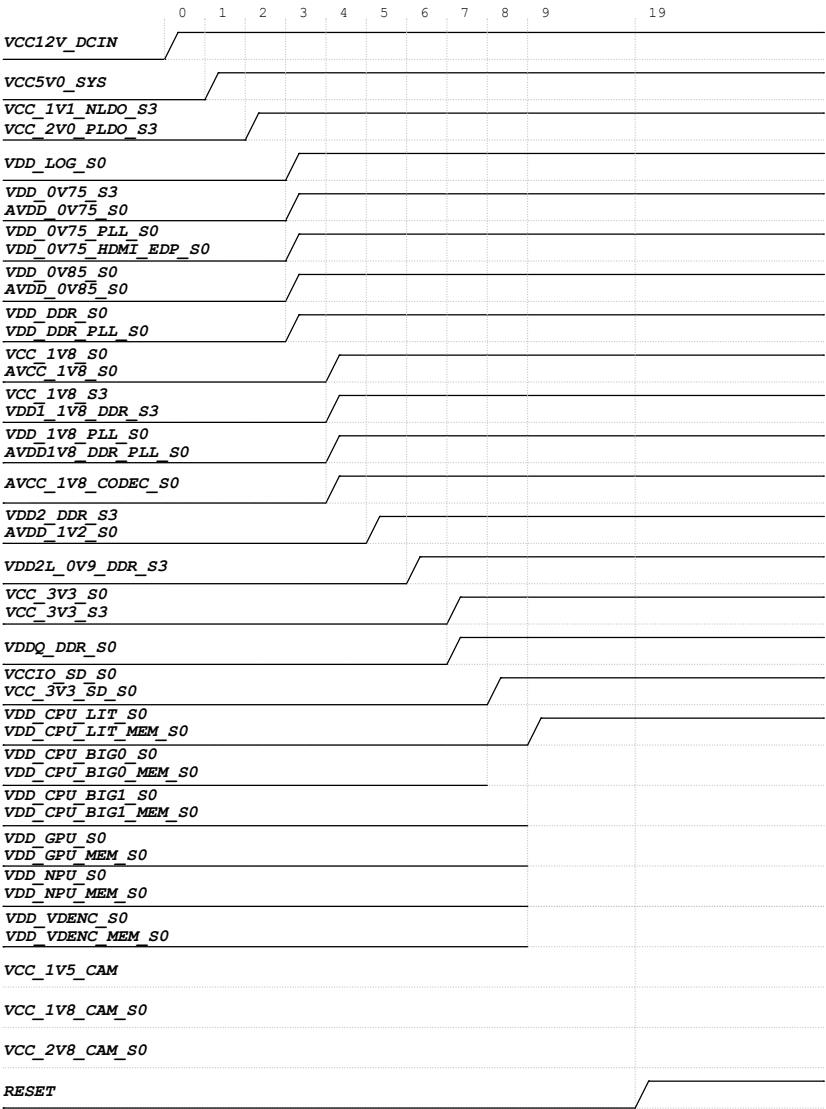
Work LED
Power LED

HINLINK			
Project:	H88K_V3.1		Rev: 00000000
File:	03.Block Diagram		
Date:	Monday, May 06, 2024		
Designer:	<designer>	Rev:	3 of 43

Power Diagram



Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC5V0_SYS	PMIC1_BUCK1	6.5A	VDD_GPU_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK2	5A	VDD_NPU_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK3	5A	VDD_LOG_S0		0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK4	3A	VDD_VDENC_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK5	2.5A	VDD_GPU_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK6	2.5A	VDD_NPU_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK7	2.5A	VCC_2V0_PLDO_S3		2.0V	ON	ON	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK8	2.5A	VDD_VDENC_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK9	2.5A	VDD2_DDR_S3		1.1V	ON	ON	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK10	2.5A	VCC_1V1_NLDO_S3		1.1V	ON	ON	TBD	TBD
VCC_2V0_PLDO	PMIC1_PLDO1	0.3A	AVCC_1V8_S0		1.8V	ON	OFF	TBD	TBD
	PMIC1_PLDO2	0.3A	VDD1_1V8_DDR_S3		1.8V	ON	ON	TBD	TBD
	PMIC1_PLDO3	0.5A	AVCC_1V8_CODECC_S0		1.8V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_PLDO4	0.5A	VCC_3V3_S3		3.3V	ON	ON	TBD	TBD
	PMIC1_PLDO5	0.3A	VCCIO_SD_S0		3.3V	ON	OFF	TBD	TBD
VCC5V0_VCCA	PMIC1_PLDO6	0.3A	VCC_1V8_S3		1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	PMIC1_NLDO1	0.3A	VDD_0V75_S3		0.75V	ON	ON	TBD	TBD
	PMIC1_NLDO2	0.3A	VDD2L_0V9_DDR_S3		0.9V	ON	ON	TBD	TBD
	PMIC1_NLDO3	0.5A	VDD_0V75_HDMI_EDP_S0		0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	PMIC1_NLDO4	0.5A	AVDD_0V75_S0		0.75V	ON	OFF	TBD	TBD
	PMIC1_NLDO5	0.3A	VDD_0V85_S0		0.85V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK1	6.5A	VDD_CPU_BIG1_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK2	5A	VDD_CPU_BIG0_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK3	5A	VDD_CPU_LIT_S0		0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK4	3A	VCC_3V3_S0		3.3V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK5	2.5A	VDD_CPU_BIG1_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK6	2.5A	VDD_CPU_BIG0_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK7	2.5A	VCC_1V8_S0		1.8V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK8	2.5A	VDD_CPU_LIT_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK9	2.5A	VDDQ_DDR_S0		0.6V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK10	2.5A	VDD_DDR_S0		0.85V	ON	OFF	TBD	TBD
VCC_2V0_PLDO	PMIC2_PLDO1	0.3A	VCC_1V8_CAM_S0		0V	OFF	OFF	TBD	TBD
	PMIC2_PLDO2	0.3A	AVDD1V8_DDR_PLL_S0		1.8V	ON	OFF	TBD	TBD
	PMIC2_PLDO3	0.5A	VDD_1V8_PLL_S0		1.8V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_PLDO4	0.5A	VCC_3V3_SD_S0		3.3V	ON	OFF	TBD	TBD
	PMIC2_PLDO5	0.3A	VCC_2V8_CAM_S0		0V	OFF	OFF	TBD	TBD
VCC_1V1_NLDO	PMIC2_NLDO1	0.3A	VDD_0V75_PLL_S0		0.75V	ON	OFF	TBD	TBD
	PMIC2_NLDO2	0.3A	VDD_DDR_PLL_S0		0.85V	ON	OFF	TBD	TBD
	PMIC2_NLDO3	0.5A	AVDD_0V85_S0		0.85V	ON	OFF	TBD	TBD
VCC_2V0_PLDO	PMIC2_NLDO4	0.5A	VCC_1V2_CAM_S0		0V	OFF	OFF	TBD	TBD
	PMIC2_NLDO5	0.3A	AVDD_1V2_S0		1.2V	ON	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3 VCC_3V3_S3	3.3V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VDDIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VDDIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_1V8/3V3_S0	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VDDIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VDDIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VDDIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VDDIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

IO Type	Operating Voltage
1.8V Only	VCCIO*_1V8=1.8V
1.8V or 3.3V	VCCIO*_1V8=1.8V VCCIO*=1.8V or 3.3V

HINLINK

Project: H88K_V3.1

File: 05.Power Sequence/IO Power

Date: Monday, May 06, 2024

Designer: <designer>

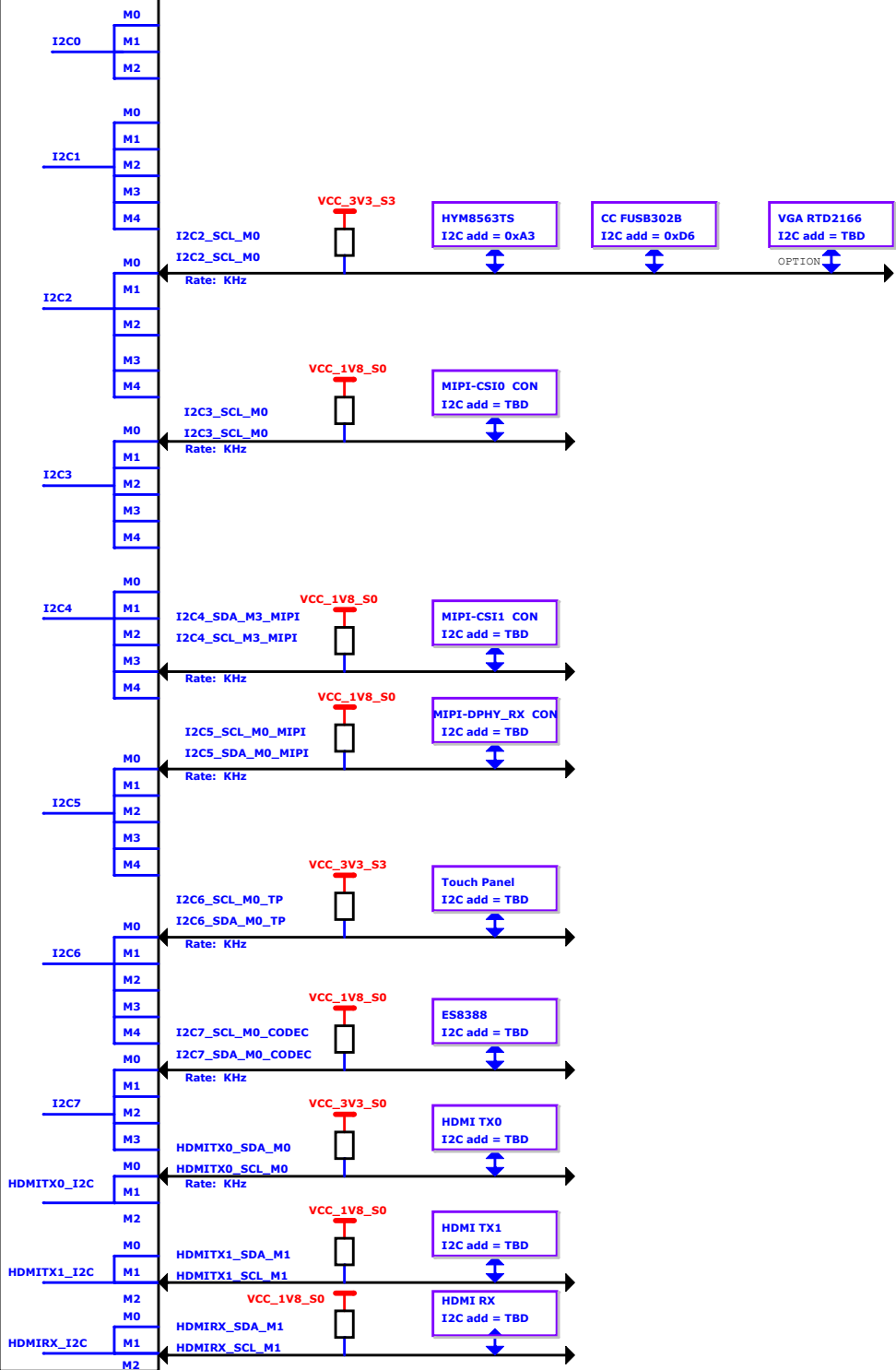
HINLINK

Rev: <Revision>

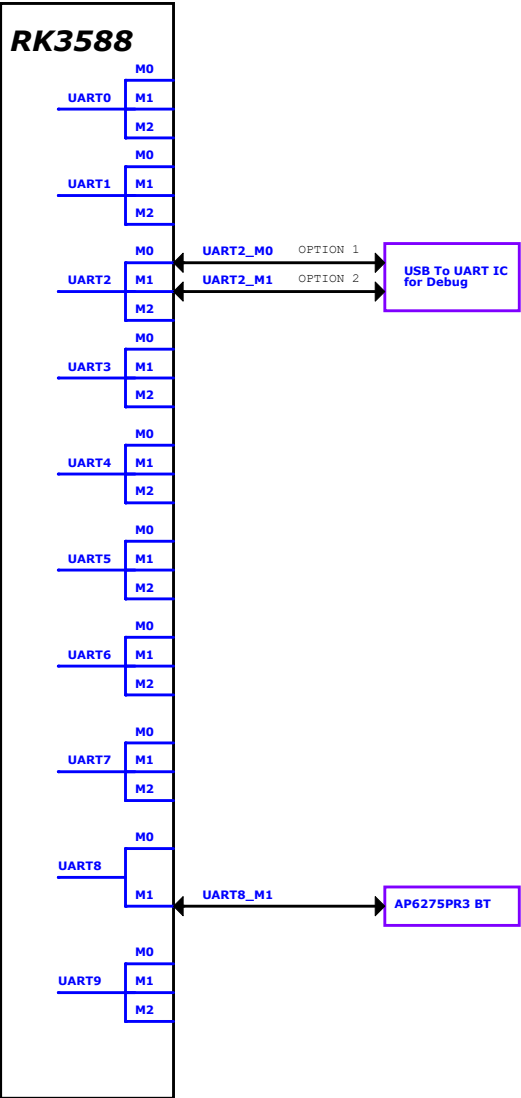
Sheet: 5 of 43

I2C MAP

RK3588



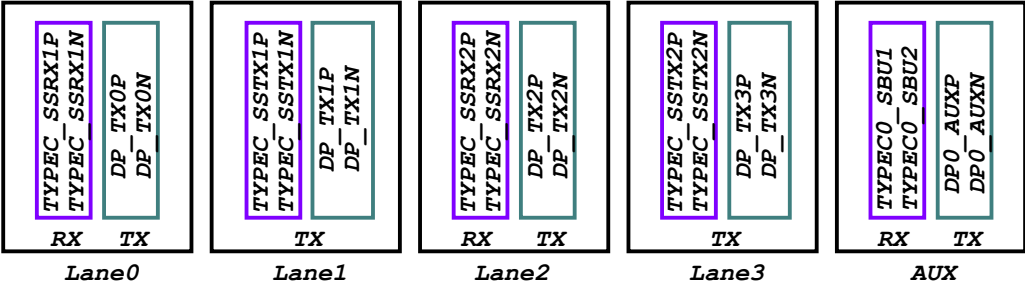
UART MAP



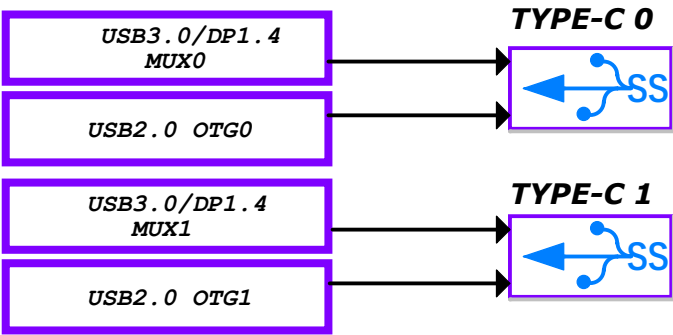
USB Controller Configure Table

Controller Name	Pin Name	Type-C Function	DPx4Lane Function		USB30 HOST+DPx2Lane Function		USB20 HOST+DPx2Lane Function		USB20 HOST+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM			TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
USB30 OTG1 Device or Host	TYPEC1_SBU1/DP1_AUXP TYPEC1_SBU2/DP1_AUXN	TYPEC1_SBU1 TYPEC1_SBU2	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN
	TYPEC1_SSRX1P/DP1_TX0P TYPEC1_SSRX1N/DP1_TX0N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX0P DP1_TX0N		DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N
	TYPEC1_SSTX1P/DP1_TX1P TYPEC1_SSTX1N/DP1_TX1N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX1P DP1_TX1N		DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N
	TYPEC1_SSRX2P/DP1_TX2P TYPEC1_SSRX2N/DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N		DP1_TX2P DP1_TX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N
	TYPEC1_SSTX2P/DP1_TX3P TYPEC1_SSTX2N/DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N		DP1_TX3P DP1_TX3N	DP1_TX3P DP1_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG1 Device or Host	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM			TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM
USB30 OTG2 Device or Host			OPTION1 USB30 HOST		OPTION2 USB30 HOST		Note: DP Lane swap enable 0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N 1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N			
	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP		USB30_2_SSTXP USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN					
	PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN									
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP		USB30_2_SSRXP USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN					
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM							
	USB20_HOST1_DP USB20_HOST1_DM				USB20_HOST1_DP USB20_HOST1_DM					

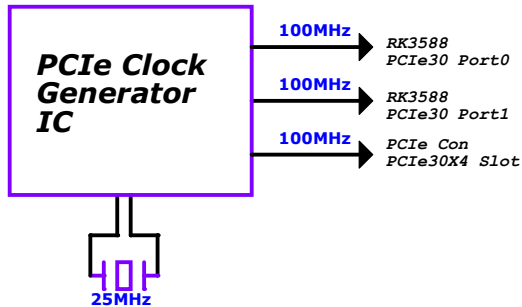
USB3.0/DP1.4 Lane Diagram



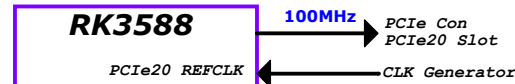
TYPE-C Connector Diagram



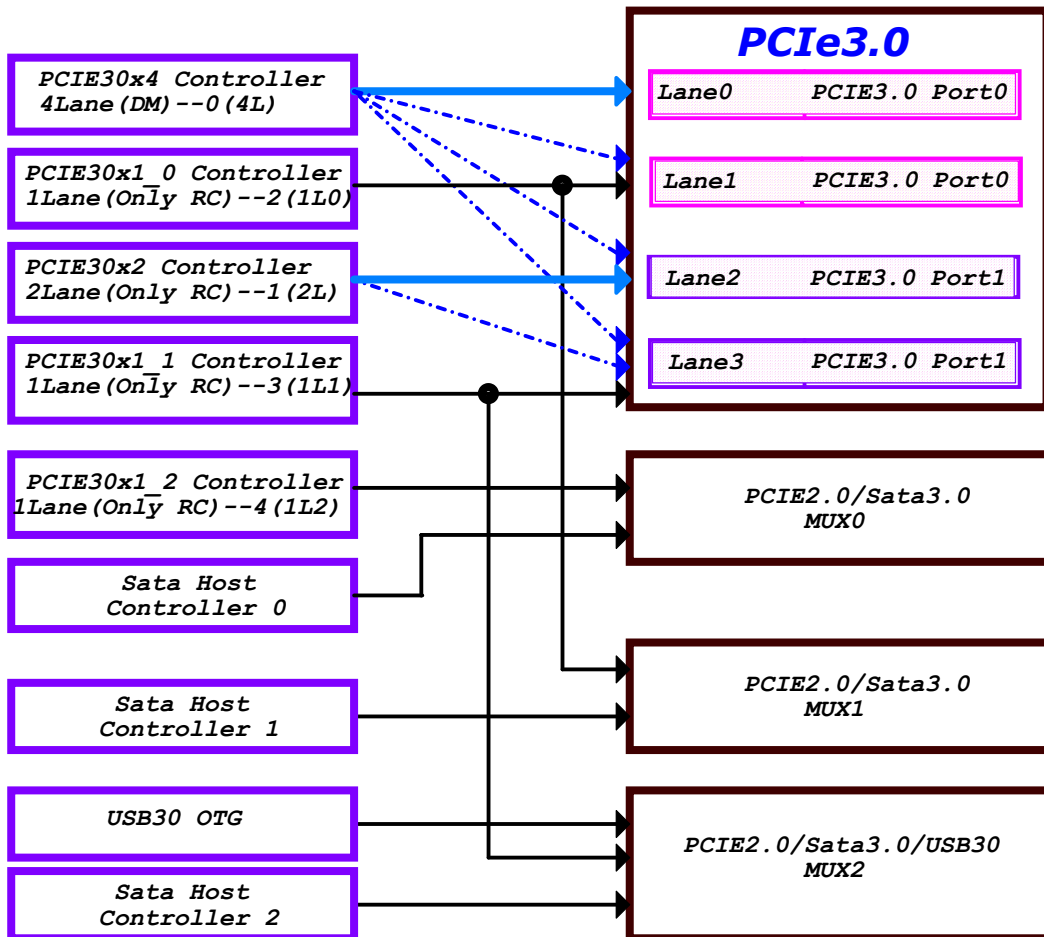
PCIe3.0 REFCLK



PCIe2.0 REFCLK



PCIe/SATA Connector Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO
	OPTION	CLK LANE	DATA LANE	
PCIe30X4 RC & EP	OPTION1	PCIe30_PORT0_REF_CLKP PCIe30_PORT0_REF_CLKN	PCIe30_PORT0_TX0 PCIe30_PORT0_RX0	PCIe30X4_CLKREQ_M* PCIe30X4_WAKEN_M* PCIe30X4_PERSTN_M* PCIe30X4_BUTTON_RSTN
	OPTION2	PCIe30_PORT0_REF_CLKP PCIe30_PORT0_REF_CLKN	PCIe30_PORT0_TX0 PCIe30_PORT0_RX0 PCIe30_PORT0_TX1 PCIe30_PORT0_RX1	
	OPTION3	PCIe30_PORT0_REF_CLKP PCIe30_PORT0_REF_CLKN PCIe30_PORT1_REF_CLKP PCIe30_PORT1_REF_CLKN	PCIe30_PORT0_TX0 PCIe30_PORT0_RX0 PCIe30_PORT1_TX0 PCIe30_PORT1_RX0 PCIe30_PORT0_TX1 PCIe30_PORT0_RX1 PCIe30_PORT1_TX1 PCIe30_PORT1_RX1	
PCIe30X2 RC	OPTION1	PCIe30_PORT1_REF_CLKP PCIe30_PORT1_REF_CLKN	PCIe30_PORT1_TX0 PCIe30_PORT1_RX0	PCIe30X2_CLKREQ_M* PCIe30X2_WAKEN_M* PCIe30X2_PERSTN_M* PCIe30X2_BUTTON_RSTN
	OPTION2	PCIe30_PORT1_REF_CLKP PCIe30_PORT1_REF_CLKN	PCIe30_PORT1_TX0 PCIe30_PORT1_RX0 PCIe30_PORT1_TX1 PCIe30_PORT1_RX1	
PCIe30X1_0 RC	OPTION1	PCIe30_PORT0_REF_CLKP PCIe30_PORT0_REF_CLKN	PCIe30_PORT0_TX1 PCIe30_PORT0_RX1	PCIe30X1_0_CLKREQ_M* PCIe30X1_0_WAKEN_M* PCIe30X1_0_PERSTN_M* PCIe30X1_0_BUTTON_RSTN
	OPTION2	PCIe20_1_REFCLKP PCIe20_1_REFCLKN	PCIe20_1_TXP PCIe20_1_TXN PCIe20_1_RXP PCIe20_1_RXN	
PCIe30X1_1 RC	OPTION1	PCIe30_PORT1_REF_CLKP PCIe30_PORT1_REF_CLKN	PCIe30_PORT1_TX1 PCIe30_PORT1_RX1	PCIe30X1_1_CLKREQ_M* PCIe30X1_1_WAKEN_M* PCIe30X1_1_PERSTN_M* PCIe30X1_1_BUTTON_RSTN
	OPTION2	PCIe20_2_REFCLKP PCIe20_2_REFCLKN	PCIe20_2_TXP PCIe20_2_TXN PCIe20_2_RXP PCIe20_2_RXN	
PCIe30X1_2 RC	OPTION1	PCIe20_0_REFCLKP PCIe20_0_REFCLKN	PCIe20_0_TXP PCIe20_0_TXN PCIe20_0_RXP PCIe20_0_RXN	PCIe20X1_2_CLKREQ_M* PCIe20X1_2_WAKEN_M* PCIe20X1_2_PERSTN_M* PCIe20X1_2_BUTTON_RSTN

Note:

PCIe30_PORT*_REF_CLKP/N is input gpio

PCIe20_*_REFCLKP/N is output or input gpio

Note:

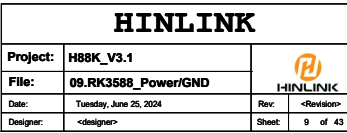
M*=Mean to M0 or M1, It's the same source, Just multiplex to M0 or M1, So, Only use one at the same time.

PCIe/SATA Function Combination

Function Combination				
Function Item	PCIEX4	PCIEX2	PCIEX1	SATA
Option1	1(DM)	0	3(RC)	0
Option2	1(DM)	0	2(RC)	1
Option3	1(DM)	0	1(RC)	2
Option4	1(DM)	0	0	3
Option5	0	1(DM)+1(RC)	3(RC)	0
Option6	0	1(DM)+1(RC)	2(RC)	1
Option7	0	1(DM)+1(RC)	1(RC)	2
Option8	0	1(DM)+1(RC)	0	3
Option9	0	1(DM)	4(RC)	1
Option10	0	1(DM)	3(RC)	2
Option11	0	1(DM)	2(RC)	3
Option12	0	0	5(RC)	2
Option13	0	0	4(RC)	3

HINLINK

Project:	H88K_V3.1	
File:	08.PCIE Fun Map	
Date:	Monday, May 06, 2024	
Designer:	<designer>	Rev: <Revision> Sheet: 8 of 43



D

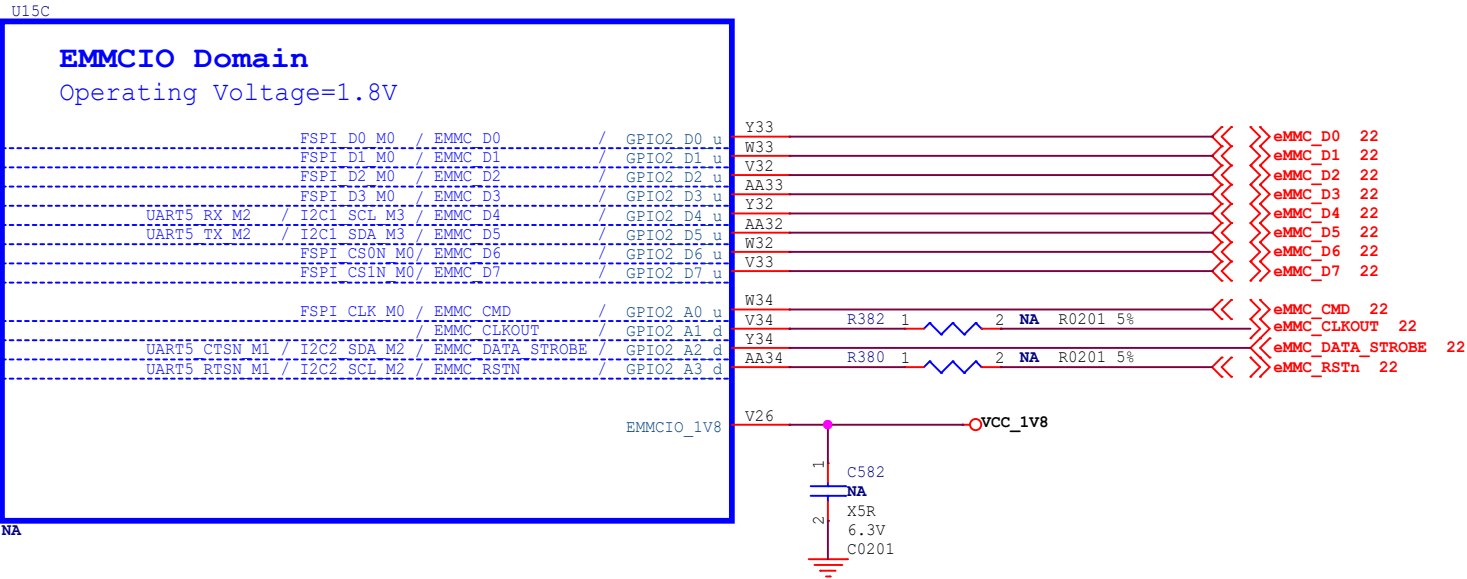


B

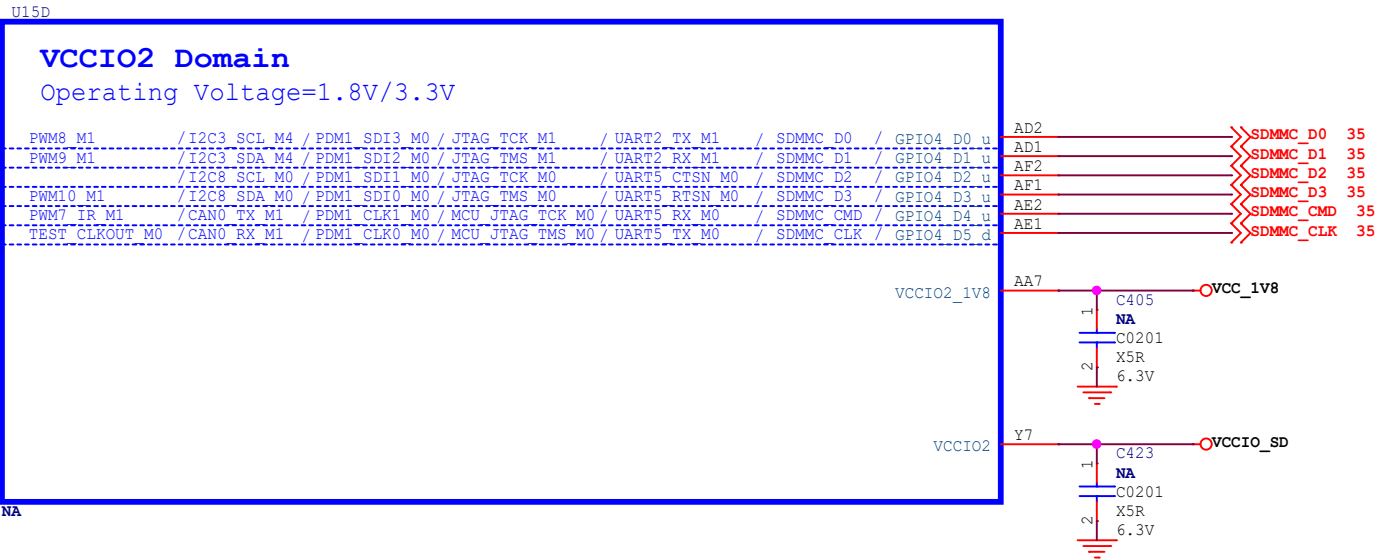


1

RK3588_C (EMMCIO Domain)



RK3588_D (VCCIO2 Domain)



HINLINK

Project:	H88K_V3.1		
File:	12.RK3588_Flash/SD Controller		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	12 of 43

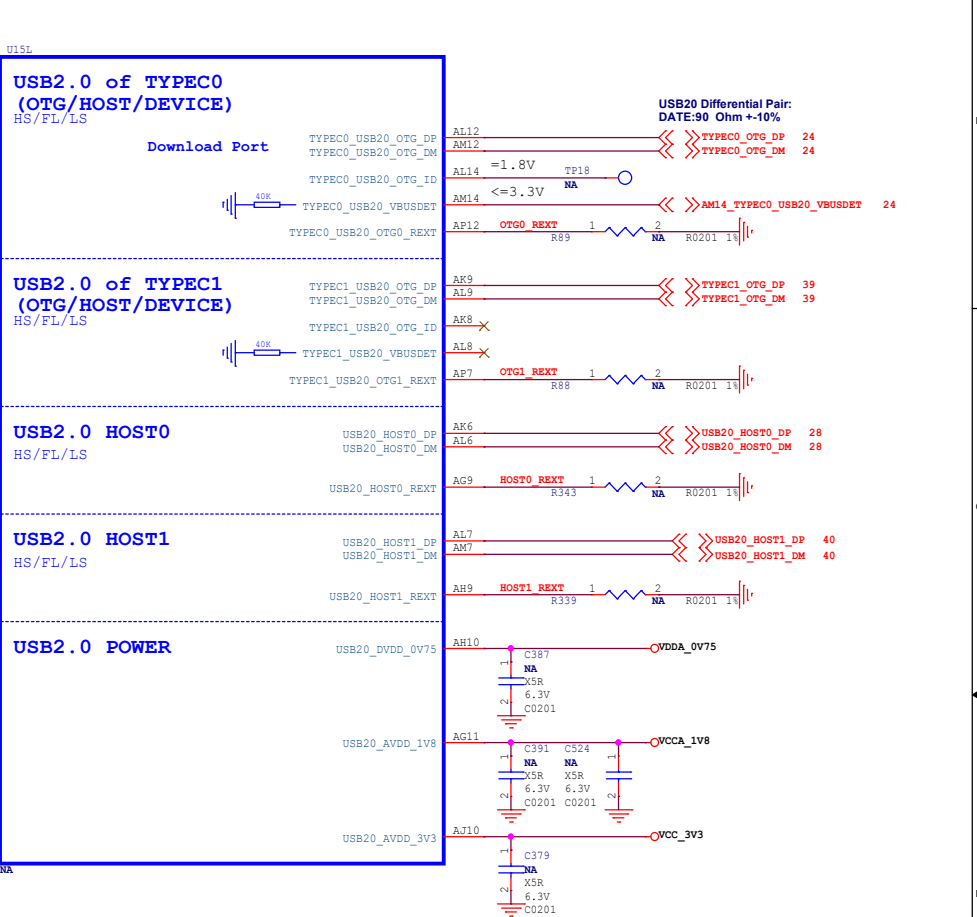
RK3588_M(TYPEC/DP)



USB30/DP1.4 Alt Mode Configuration

Option1	DP x4Lane	DP_TX_Lane0-3
Option2	USB30 x4Lane	DP_TX_Lane0-3
Option3	USB30X2Lane+DPX2Lane	USB30: Lane0 Lane1 DP: Lane2 Lane3
Option4	USB30X2Lane+DPX2Lane	USB30: Lane2 Lane3 DP: Lane0 Lane1

RK3588_L(USB2.0 HOST/OTG)

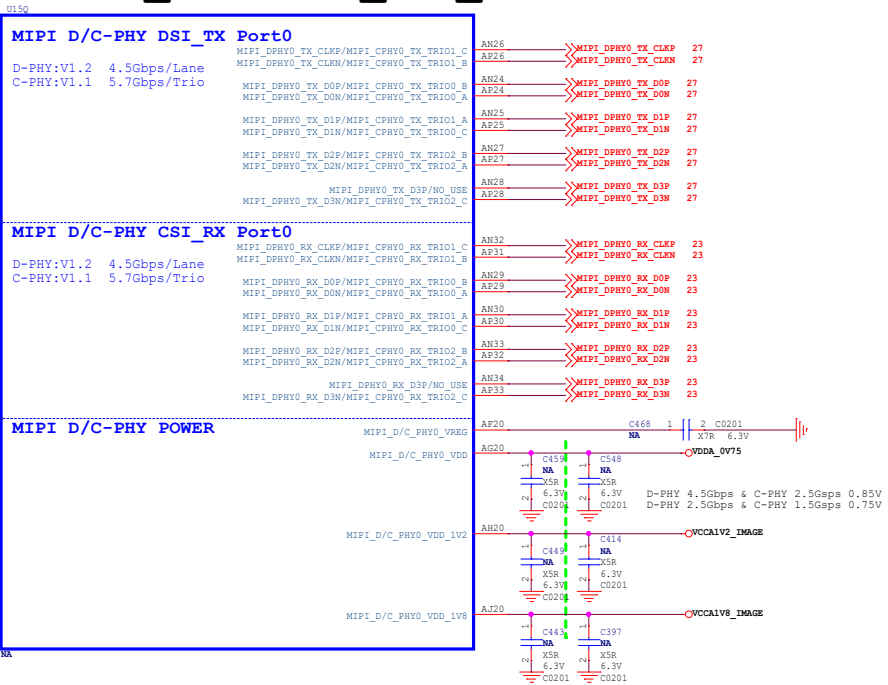


Note:

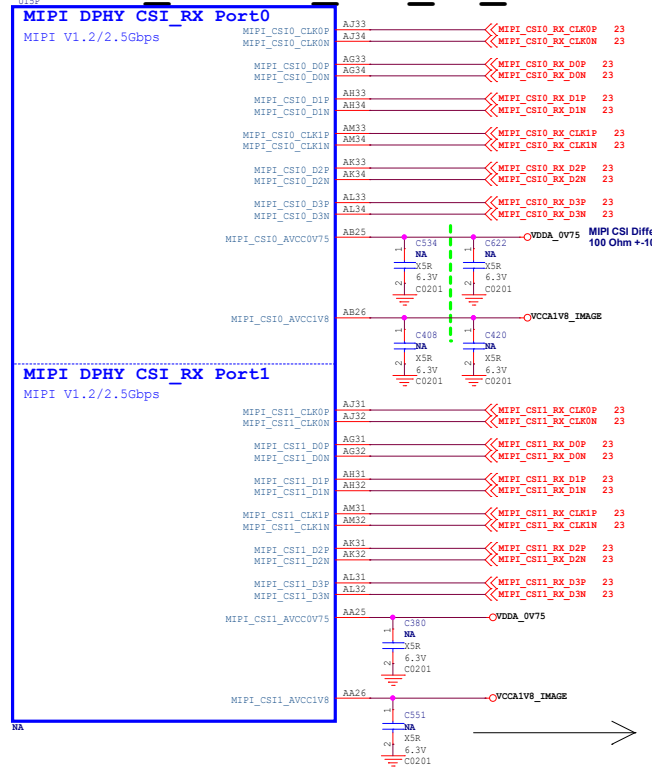
The USB20 VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

HINLINK			
Project:	H88K_V3.1	Rev:	<Revision>
File:	13.RK3588_USB30/USB20_Ctrl	Sheet:	13 of 43
Date:	Tuesday, June 25, 2024		
Designer:	<designer>		

RK3588_Q/R(MIPI_D/C_PHY0/1)



RK3588_P(MIPI_CSI_RX_PHY)



MIPI_CSI_RX Configuration

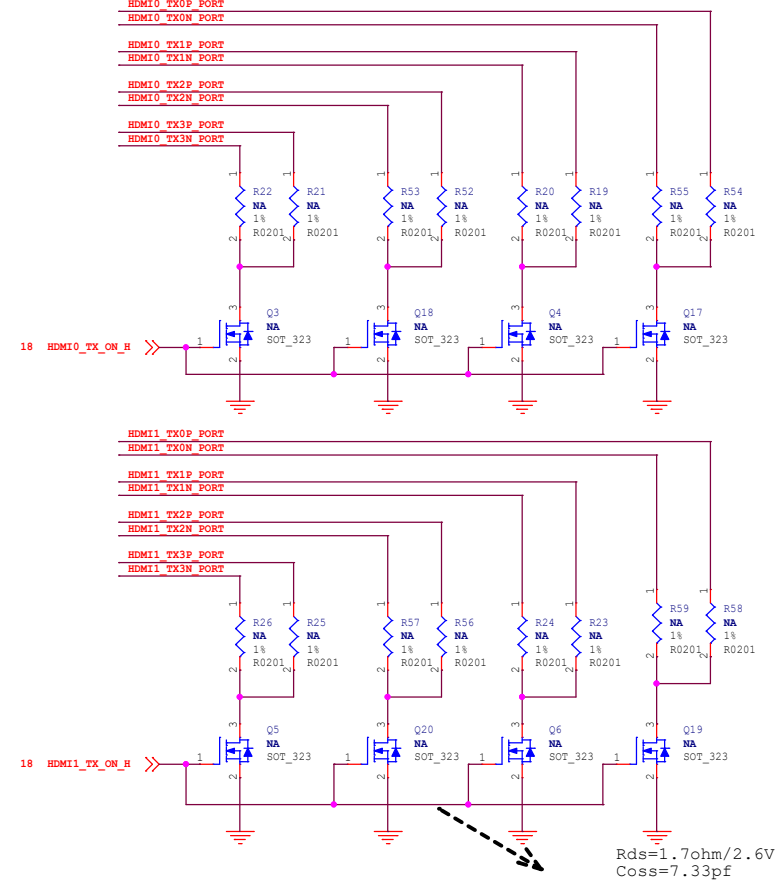
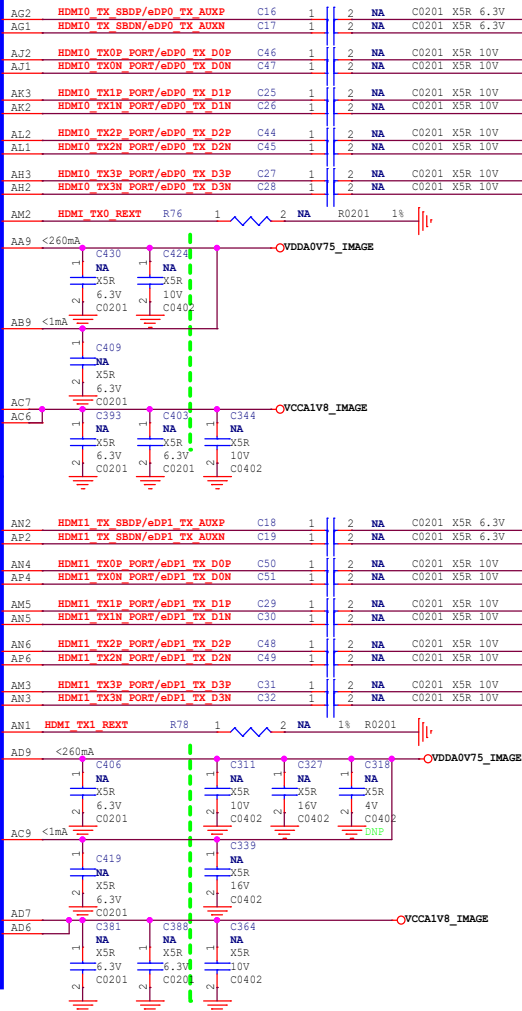
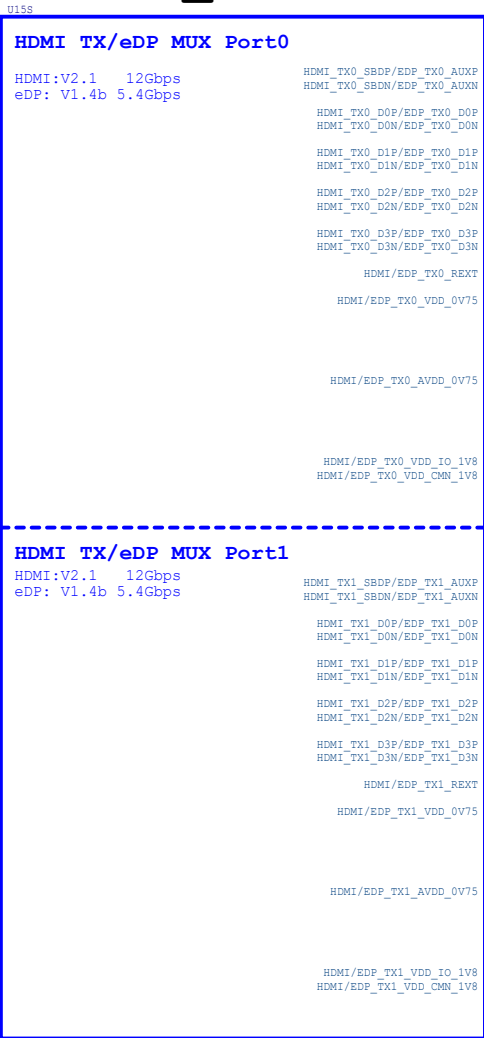
Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3, but clock lane1 is invalid; In dual clock lanes mode, CLK0P/0N is the clock lane of Data lane0 and Data lane1, while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
The Caps to the left of green line should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

Note:
Merge the two mipi csi's power need 1X105+1X104 cap.

RK3588_S (HDMI2.1 TX)



Note:

The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

Note:

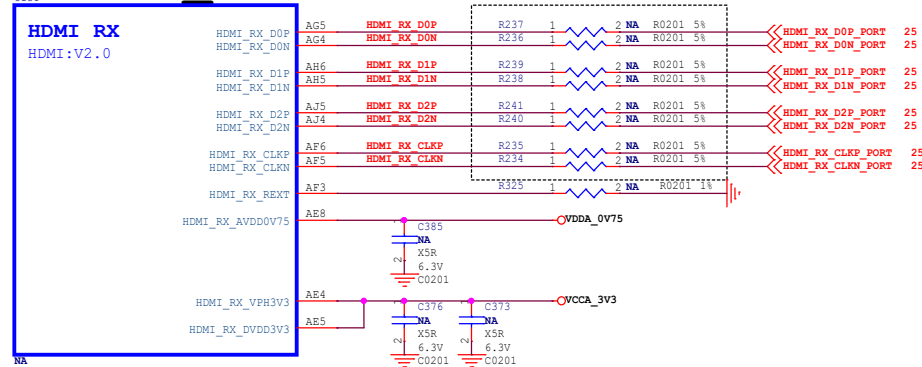
The Caps to the left of green line should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

Note:

The controller only support AC coupled link In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.

RK3588_T (HDMI20 RX)



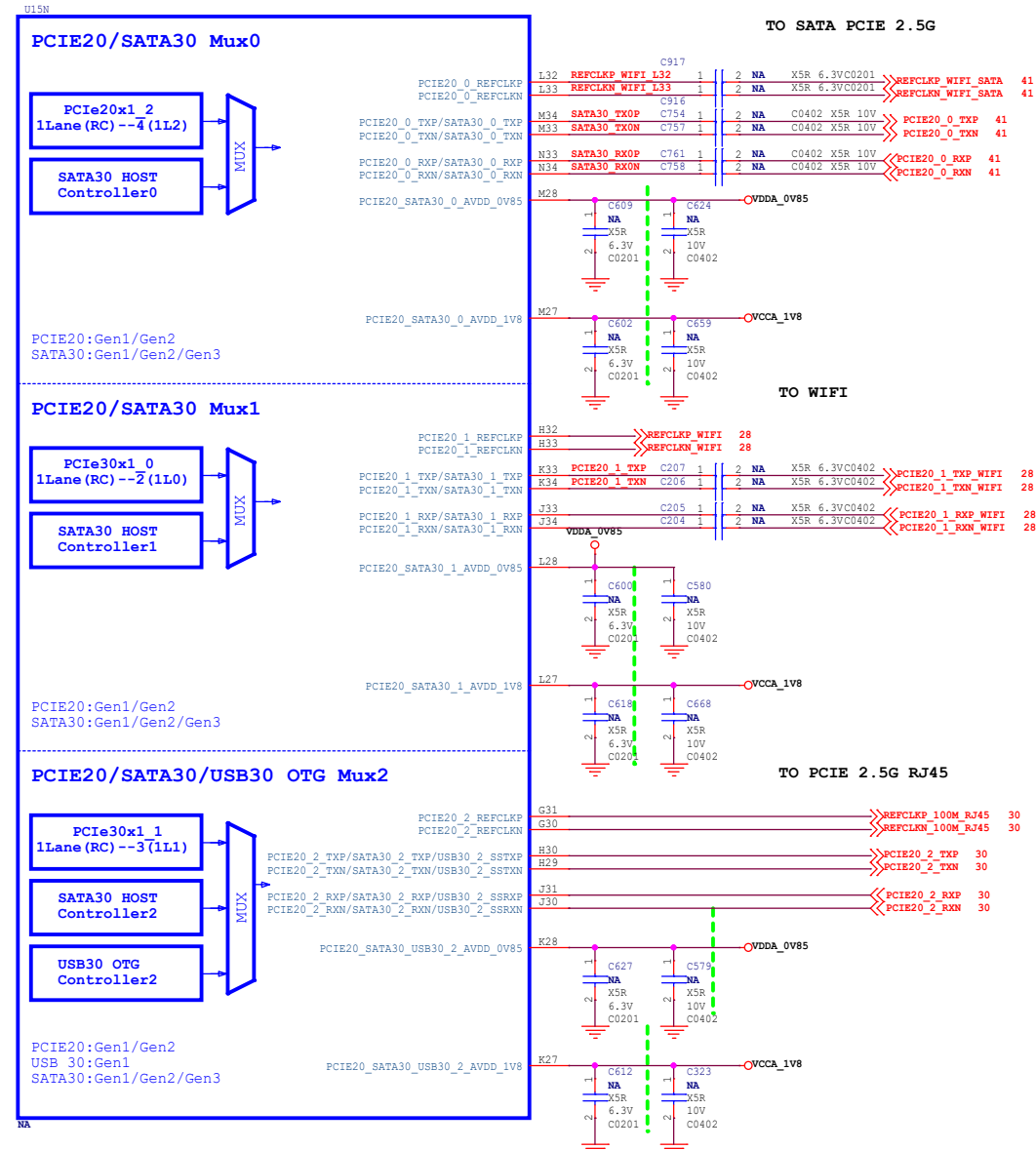
HDMI20_RX
100 Ohm +-10%

HINLINK

Project:	H88K_V3.1	Rev:	<Revision>
File:	16.RK3588_HDMI/eDP Interface	Sheet:	16 of 43
Date:	Tuesday, June 25, 2024		
Designer:	<designer>		

RK3588_N (PCIE20)

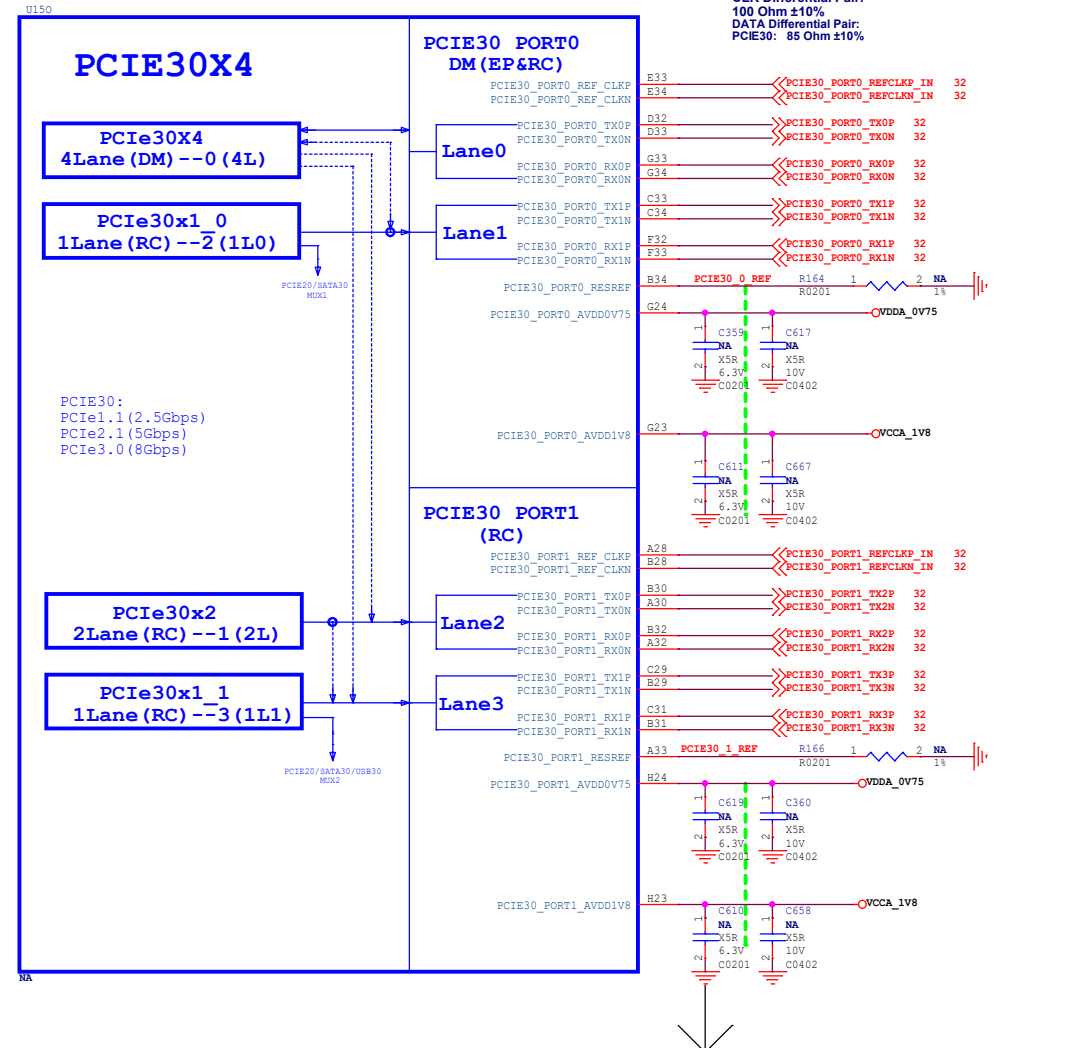
CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%
USB30: 90ohm ±10%



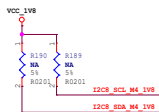
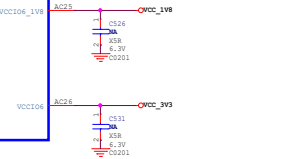
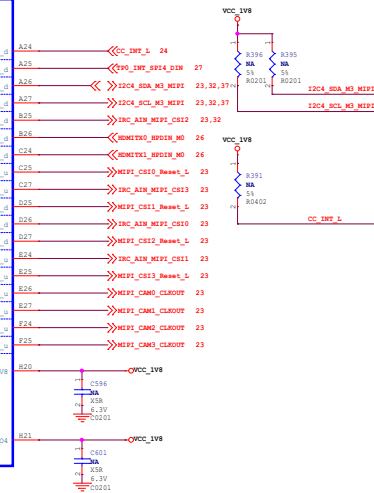
RK3588_O (PCIE30)

Note:
Only PCIE30 Controller 0
support RC and EP,Other
controller only support RC
Mode.

CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE30: 85 Ohm ±10%



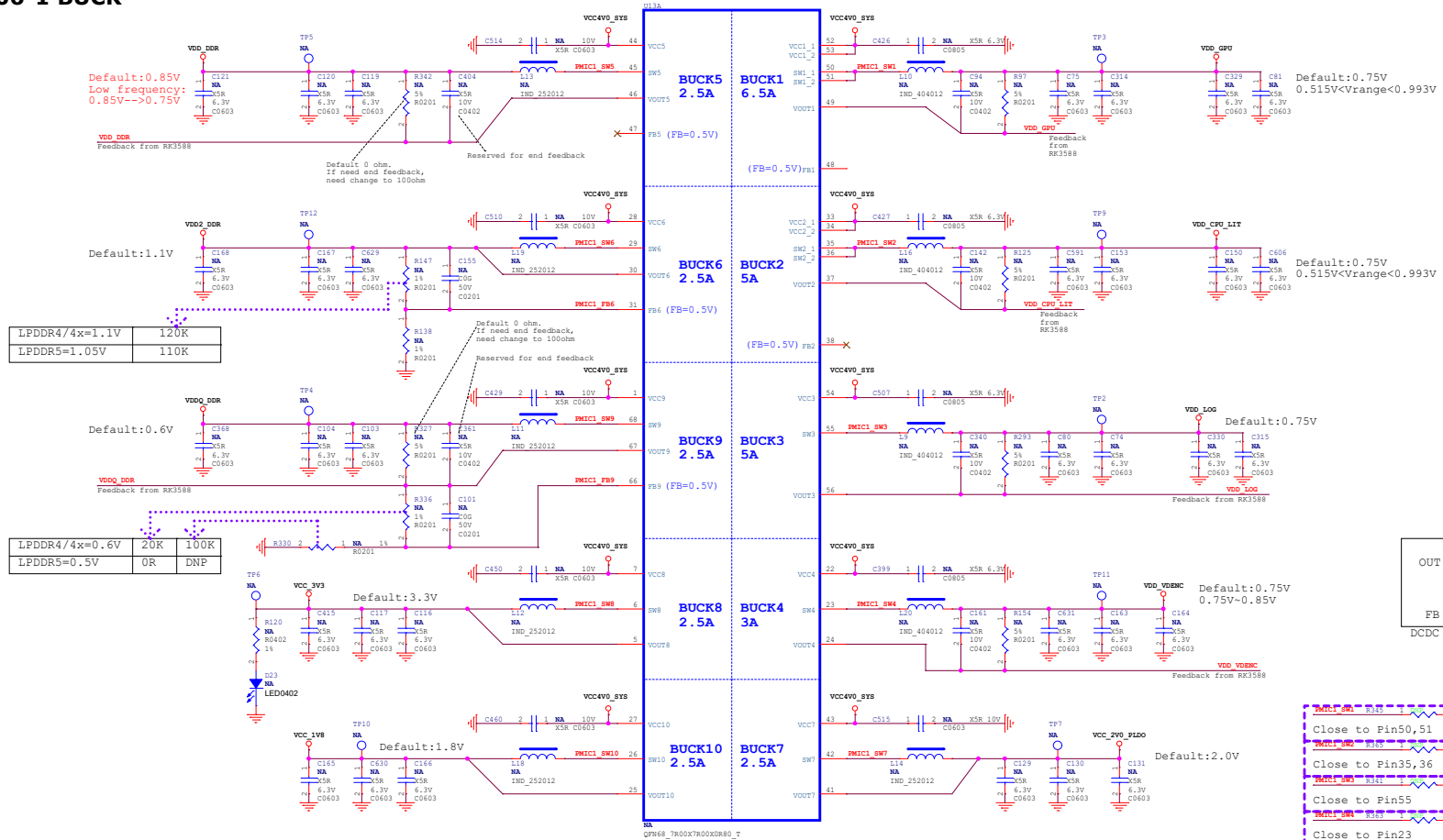
HINLINK			
Project:	H88K_V3.1		
File:	17.RK3588_PCIE30/PCIE20/SATA30		
Date:	Tuesday, June 25, 2024		
Designer:	<designer>		
Rev:	<Revision>	Sheet:	17 of 43

[illegible][illegible][illegible]

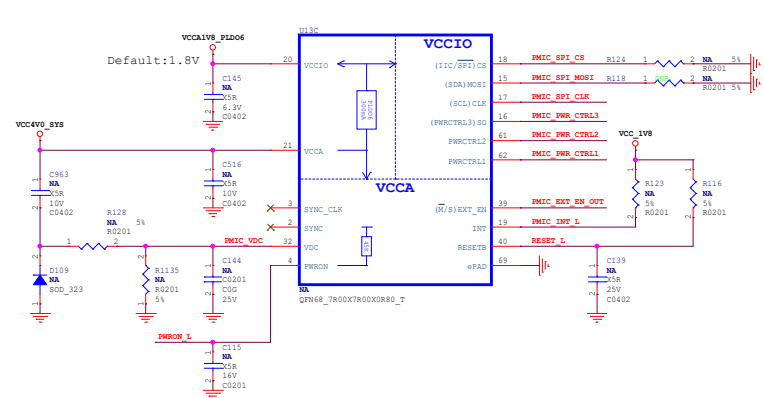
HINLINK			
Project:	H88K_V3.1	 HINLINK	
File:	18.RK3588_1.8V/ 3.3V GPIO		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<Designer>	Sheet:	16 of 43

PMIC RK806-1 BUCK

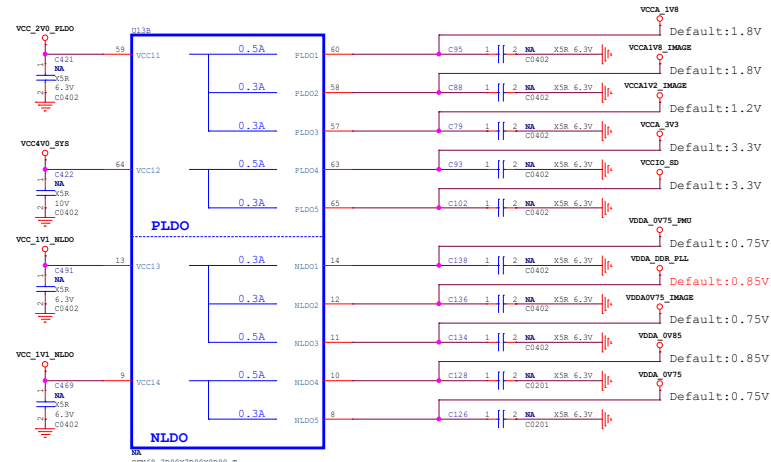
>>>PMIC_SPI_CS 10
 >>>PMIC_SPI_MOSI 10
 >>>PMIC_SPI_CLK 10
 >>>PMIC_PWD_CTLB1 10
 >>>PMIC_PWD_CTLB2 10
 >>>PMIC_PWD_CTLB3 10
 >>>PMIC_INT_1 10
 >>>RESET_1 10,36
 >>>PWRON_L 36
 >>>PMIC_EXT_EN_OUT 20



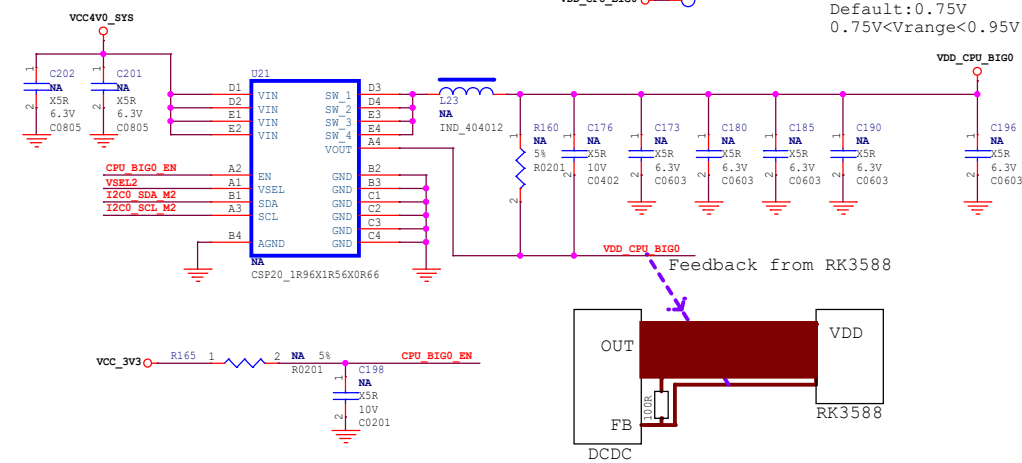
PMIC RK806-1 Managerment



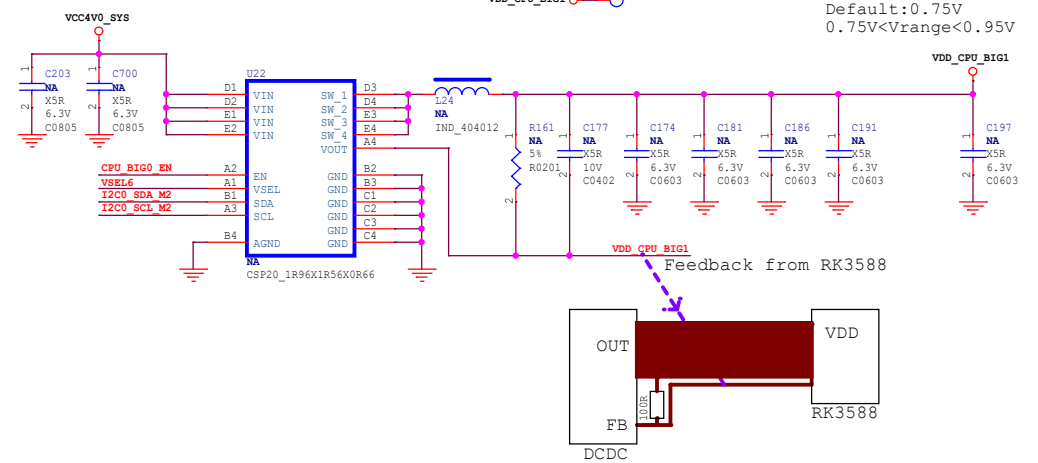
PMIC RK806-1 LDO



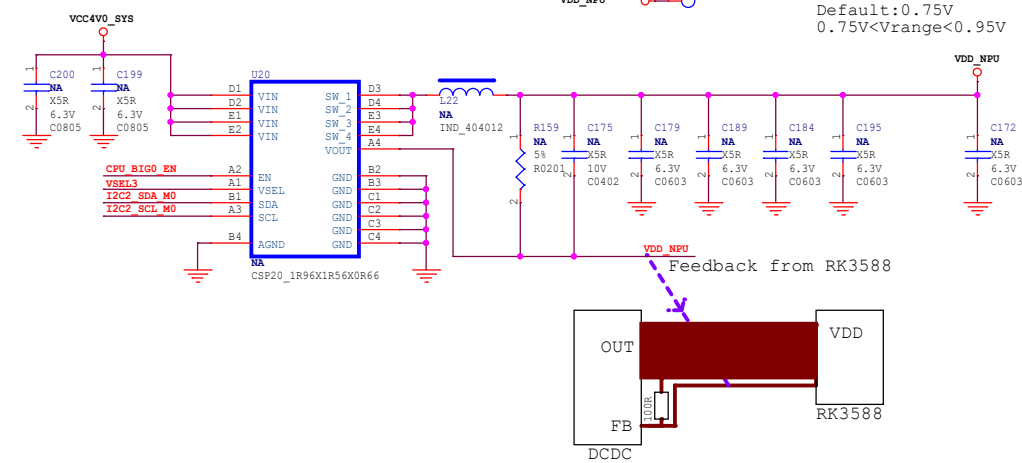
VDD_CPU_BIG0



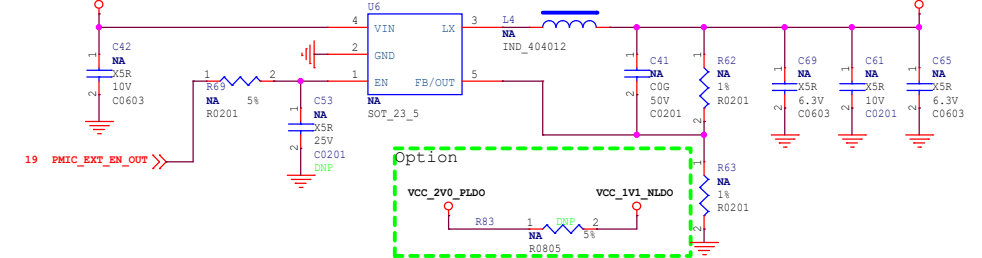
VDD_CPU_BIG1



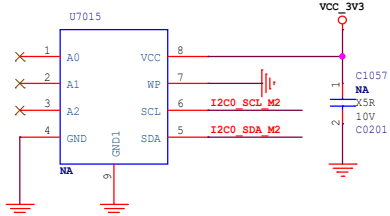
VDD_NPU



VCC_1V1_NLDO_S3



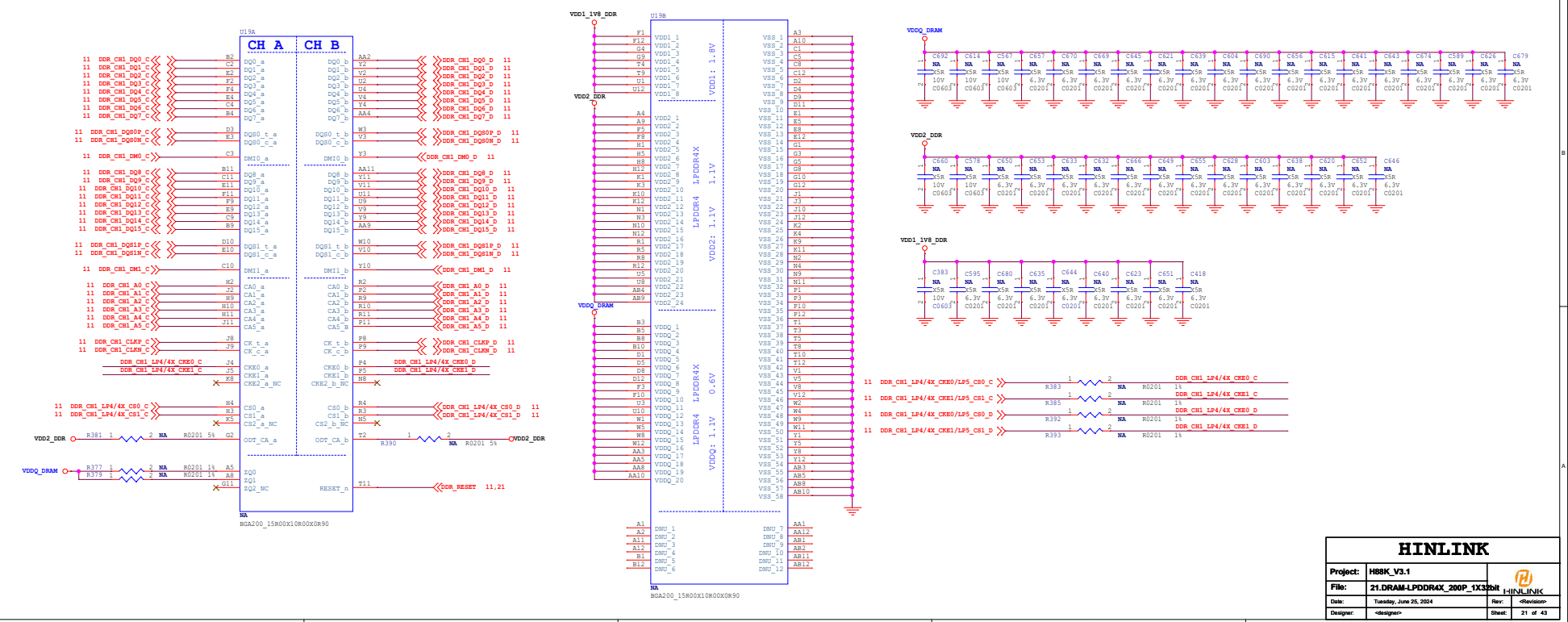
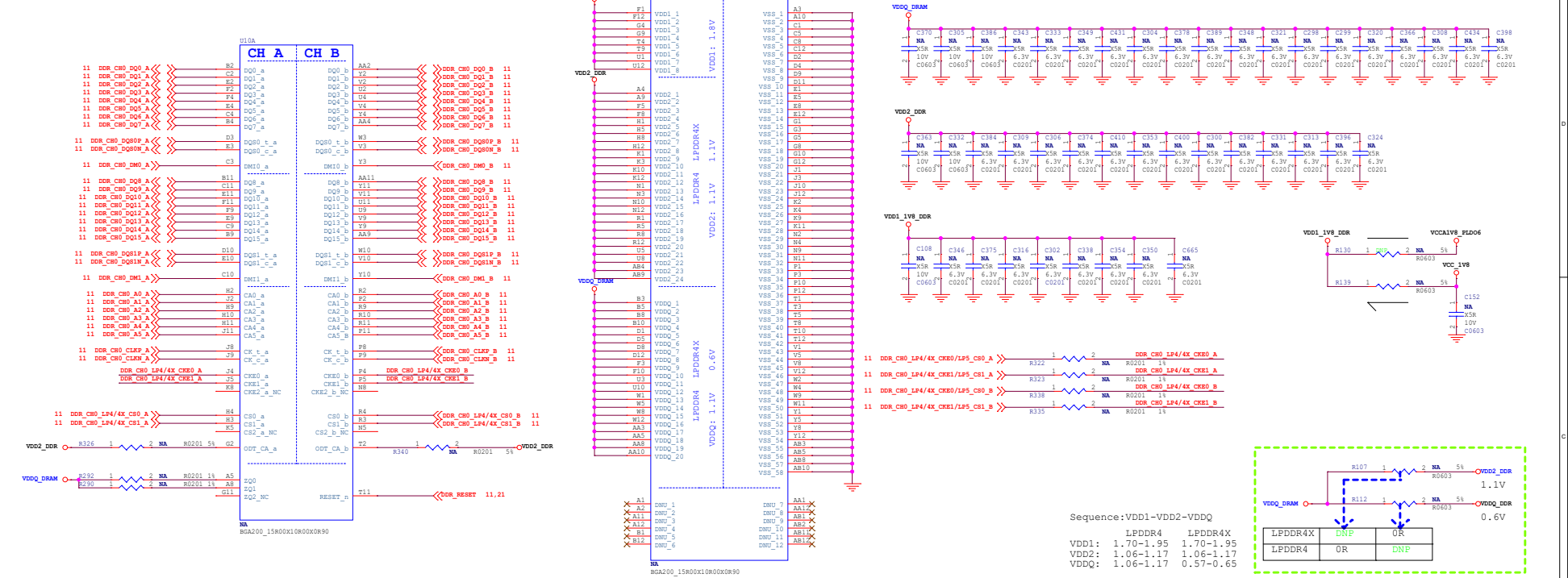
加密



HINLINK

Project:	H88K_V3.1	Rev:	<Revision>
File:	20.Power_Ext Discrete	Sheet:	20 of 43
Date:	Tuesday, June 25, 2024		
Designer:	<designer>		

LPDDR4/4X



eMMC FLASH

12 eMMC_RSTn >> eMMC_RSTn

12 eMMC_D0 << >> A3 DATA0 VCCQ1

12 eMMC_D1 << >> A4 DATA1 VCCQ2

12 eMMC_D2 << >> A5 DATA2 VCCQ3

12 eMMC_D3 << >> B2 DATA3 VCCQ4

12 eMMC_D4 << >> B3 DATA4 VCCQ5

12 eMMC_D5 << >> B4 DATA5 VCC1

12 eMMC_D6 << >> B5 DATA6 VCC2

12 eMMC_D7 << >> B6 DATA7 VCC3

12 eMMC_CMD << >> M5 CMD VCC4

12 eMMC_CLKOUT >> M6 CLK VSS1

VCC_1V8 R409 1 2 NA R0201 5% eMMC_RSTn K5 RST_n VSS2

C677 2 1 NA C0402 X5R VSS3

6.3V C682 1 NA X5R C0201 5% VSS4

12 eMMC_DATA_STROBE << R408 1 2 NA R0201 5% H5 Data Strobe VSS5

C684 1 NA X5R C0402 VSS6

C685 1 NA X5R C0402 VSSQ1

C689 1 NA X5R C0402 VSSQ2

C693 1 NA X5R C0402 VSSQ3

C699 1 NA X5R C0402 VSSQ4

C678 1 NA X5R C0402 VSSQ5

C697 1 NA X5R C0402 VSSQ1

C702 1 NA X5R C0603 VSSQ2

C689 1 NA X5R C0402 VSSQ3

C693 1 NA X5R C0402 VSSQ4

C699 1 NA X5R C0402 VSSQ5

C684 1 NA X5R C0402 VSSQ1

C685 1 NA X5R C0402 VSSQ2

C697 1 NA X5R C0402 VSSQ3

C702 1 NA X5R C0603 VSSQ4

C689 1 NA X5R C0402 VSSQ5

C693 1 NA X5R C0402 VSSQ1

C699 1 NA X5R C0402 VSSQ2

C678 1 NA X5R C0402 VSSQ3

C697 1 NA X5R C0402 VSSQ4

C702 1 NA X5R C0603 VSSQ5

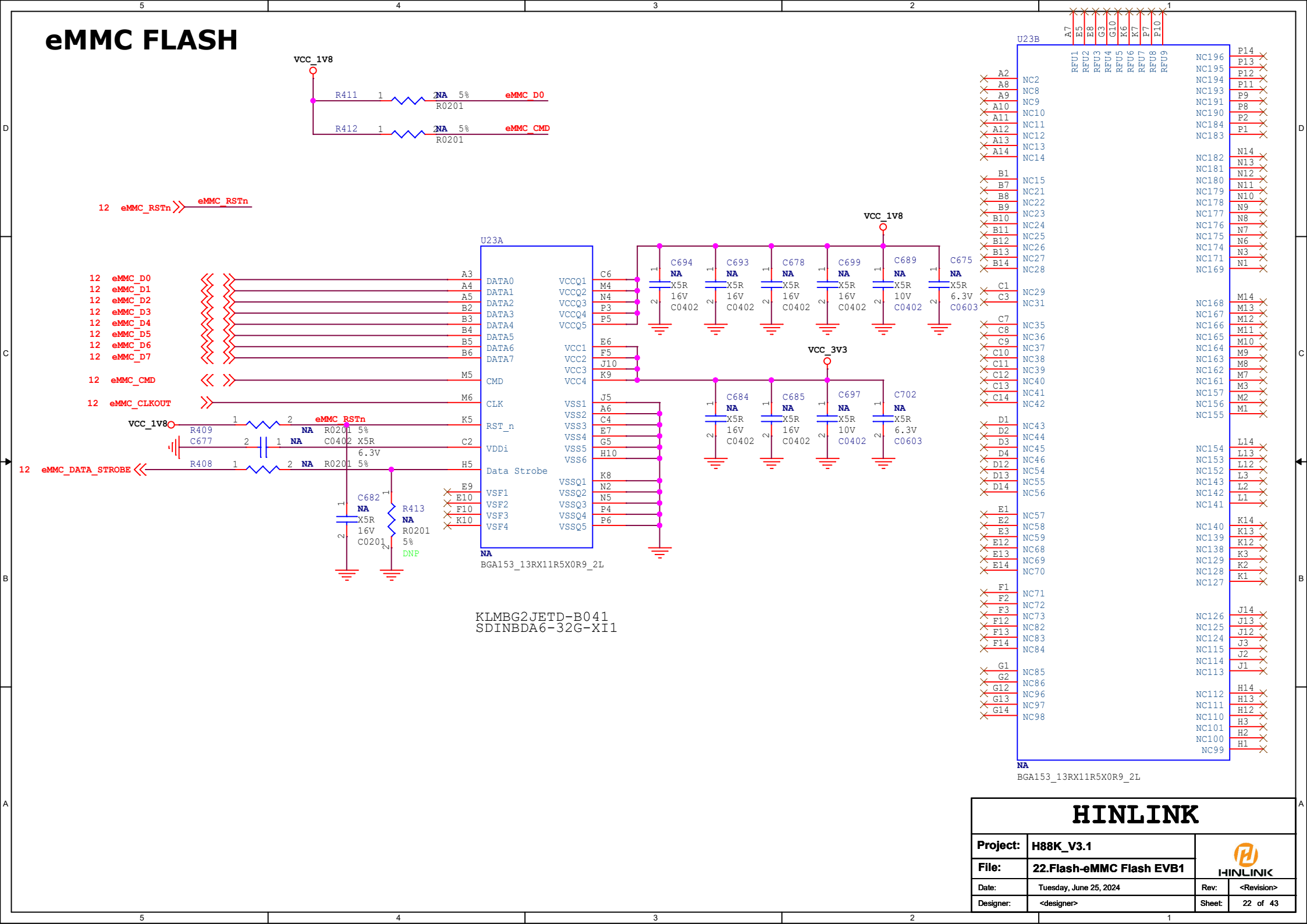
U23A BGA153_13RX11R5X0R9_2L

U23B BGA153_13RX11R5X0R9_2L

KLMBG2JETD-B041

SDINBDA6-32G-XI1

Pin	Signal	Pin	Signal	Pin	Signal
A7	NC2	NC196	P14	NC196	P14
A8	NC8	NC195	P13	NC195	P13
A9	NC9	NC194	P12	NC194	P12
A10	NC10	NC193	P11	NC193	P11
A11	NC11	NC191	P9	NC191	P9
A12	NC12	NC184	P8	NC184	P8
A13	NC13	NC183	P2	NC183	P2
A14	NC14	NC182	P1	NC182	P1
B1	NC15	NC181	N14	NC181	N14
B7	NC21	NC180	N13	NC180	N13
B8	NC22	NC179	N12	NC179	N12
B9	NC23	NC178	N11	NC178	N11
B10	NC24	NC177	N10	NC177	N10
B11	NC25	NC176	N9	NC176	N9
B12	NC26	NC175	N8	NC175	N8
B13	NC27	NC174	N7	NC174	N7
B14	NC28	NC173	N6	NC173	N6
C1	NC29	NC172	N5	NC172	N5
C3	NC31	NC171	N4	NC171	N4
C7	NC35	NC168	N3	NC168	N3
C8	NC36	NC167	N2	NC167	N2
C9	NC37	NC166	N1	NC166	N1
C10	NC38	NC165	M14	NC165	M14
C11	NC39	NC164	M13	NC164	M13
C12	NC40	NC163	M12	NC163	M12
C13	NC41	NC162	M11	NC162	M11
C14	NC42	NC161	M10	NC161	M10
D1	NC43	NC160	M9	NC160	M9
D2	NC44	NC159	M8	NC159	M8
D3	NC45	NC158	M7	NC158	M7
D4	NC46	NC157	M6	NC157	M6
D12	NC54	NC156	M5	NC156	M5
D13	NC55	NC155	M4	NC155	M4
D14	NC56	NC154	M3	NC154	M3
E1	NC57	NC153	M2	NC153	M2
E2	NC58	NC152	M1	NC152	M1
E3	NC59	NC151	L14	NC151	L14
E12	NC68	NC150	L13	NC150	L13
E13	NC69	NC149	L12	NC149	L12
E14	NC70	NC148	L11	NC148	L11
F1	NC71	NC147	L10	NC147	L10
F2	NC72	NC146	L9	NC146	L9
F3	NC73	NC145	L8	NC145	L8
F12	NC82	NC144	L7	NC144	L7
F13	NC83	NC143	L6	NC143	L6
F14	NC84	NC142	L5	NC142	L5
G1	NC85	NC141	L4	NC141	L4
G2	NC86	NC140	L3	NC140	L3
G12	NC96	NC139	L2	NC139	L2
G13	NC97	NC1			



eMMC FLASH

12 eMMC_RSTn >> eMMC_RSTn

12 eMMC_D0 << >> A3 DATA0 VCCQ1

12 eMMC_D1 << >> A4 DATA1 VCCQ2

12 eMMC_D2 << >> A5 DATA2 VCCQ3

12 eMMC_D3 << >> B2 DATA3 VCCQ4

12 eMMC_D4 << >> B3 DATA4 VCCQ5

12 eMMC_D5 << >> B4 DATA5 VCC1

12 eMMC_D6 << >> B5 DATA6 VCC2

12 eMMC_D7 << >> B6 DATA7 VCC3

12 eMMC_CMD << >> M5 CMD VCC4

12 eMMC_CLKOUT >> M6 CLK VSS1

VCC_1V8 R409 1 2 NA R0201 5% eMMC_RSTn K5 RST_n VSS2

C677 2 1 NA C0402 X5R VSS3

6.3V C682 1 NA X5R C0201 5% VSS4

12 eMMC_DATA_STROBE << R408 1 2 NA R0201 5% H5 Data Strobe VSS5

C684 1 NA X5R C0402 VSS6

C685 1 NA X5R C0402 VSSQ1

C688 1 NA X5R C0402 VSSQ2

C689 1 NA X5R C0402 VSSQ3

C690 1 NA X5R C0402 VSSQ4

C691 1 NA X5R C0402 VSSQ5

C692 1 NA X5R C0402 VSSQ6

C693 1 NA X5R C0402 VSSQ7

C694 1 NA X5R C0402 VSSQ8

C695 1 NA X5R C0402 VSSQ9

C696 1 NA X5R C0402 VSSQ10

C697 1 NA X5R C0402 VSSQ11

C698 1 NA X5R C0402 VSSQ12

C699 1 NA X5R C0402 VSSQ13

C700 1 NA X5R C0402 VSSQ14

C701 1 NA X5R C0402 VSSQ15

C702 1 NA X5R C0402 VSSQ16

C703 1 NA X5R C0402 VSSQ17

C704 1 NA X5R C0402 VSSQ18

C705 1 NA X5R C0402 VSSQ19

C706 1 NA X5R C0402 VSSQ20

C707 1 NA X5R C0402 VSSQ21

C708 1 NA X5R C0402 VSSQ22

C709 1 NA X5R C0402 VSSQ23

C710 1 NA X5R C0402 VSSQ24

C711 1 NA X5R C0402 VSSQ25

C712 1 NA X5R C0402 VSSQ26

C713 1 NA X5R C0402 VSSQ27

C714 1 NA X5R C0402 VSSQ28

C715 1 NA X5R C0402 VSSQ29

C716 1 NA X5R C0402 VSSQ30

C717 1 NA X5R C0402 VSSQ31

C718 1 NA X5R C0402 VSSQ32

C719 1 NA X5R C0402 VSSQ33

C720 1 NA X5R C0402 VSSQ34

C721 1 NA X5R C0402 VSSQ35

C722 1 NA X5R C0402 VSSQ36

C723 1 NA X5R C0402 VSSQ37

C724 1 NA X5R C0402 VSSQ38

C725 1 NA X5R C0402 VSSQ39

C726 1 NA X5R C0402 VSSQ40

C727 1 NA X5R C0402 VSSQ41

C728 1 NA X5R C0402 VSSQ42

C729 1 NA X5R C0402 VSSQ43

C730 1 NA X5R C0402 VSSQ44

C731 1 NA X5R C0402 VSSQ45

C732 1 NA X5R C0402 VSSQ46

C733 1 NA X5R C0402 VSSQ47

C734 1 NA X5R C0402 VSSQ48

C735 1 NA X5R C0402 VSSQ49

C736 1 NA X5R C0402 VSSQ50

C737 1 NA X5R C0402 VSSQ51

C738 1 NA X5R C0402 VSSQ52

C739 1 NA X5R C0402 VSSQ53

C740 1 NA X5R C0402 VSSQ54

C741 1 NA X5R C0402 VSSQ55

C742 1 NA X5R C0402 VSSQ56

C743 1 NA X5R C0402 VSSQ57

C744 1 NA X5R C0402 VSSQ58

C745 1 NA X5R C0402 VSSQ59

C746 1 NA X5R C0402 VSSQ60

C747 1 NA X5R C0402 VSSQ61

C748 1 NA X5R C0402 VSSQ62

C749 1 NA X5R C0402 VSSQ63

C750 1 NA X5R C0402 VSSQ64

C751 1 NA X5R C0402 VSSQ65

C752 1 NA X5R C0402 VSSQ66

C753 1 NA X5R C0402 VSSQ67

C754 1 NA X5R C0402 VSSQ68

C755 1 NA X5R C0402 VSSQ69

C756 1 NA X5R C0402 VSSQ70

C757 1 NA X5R C0402 VSSQ71

C758 1 NA X5R C0402 VSSQ72

C759 1 NA X5R C0402 VSSQ73

C760 1 NA X5R C0402 VSSQ74

C761 1 NA X5R C0402 VSSQ75

C762 1 NA X5R C0402 VSSQ76

C763 1 NA X5R C0402 VSSQ77

C764 1 NA X5R C0402 VSSQ78

C765 1 NA X5R C0402 VSSQ79

C766 1 NA X5R C0402 VSSQ80

C767 1 NA X5R C0402 VSSQ81

C768 1 NA X5R C0402 VSSQ82

C769 1 NA X5R C0402 VSSQ83

C770 1 NA X5R C0402 VSSQ84

C771 1 NA X5R C0402 VSSQ85

C772 1 NA X5R C0402 VSSQ86

C773 1 NA X5R C0402 VSSQ87

C774 1 NA X5R C0402 VSSQ88

C775 1 NA X5R C0402 VSSQ89

C776 1 NA X5R C0402 VSSQ90

C777 1 NA X5R C0402 VSSQ91

C778 1 NA X5R C0402 VSSQ92

C779 1 NA X5R C0402 VSSQ93

C780 1 NA X5R C0402 VSSQ94

C781 1 NA X5R C0402 VSSQ95

C782 1 NA X5R C0402 VSSQ96

C783 1 NA X5R C0402 VSSQ97

C784 1 NA X5R C0402 VSSQ98

C785 1 NA X5R C0402 VSSQ99

C786 1 NA X5R C0402 VSSQ100

C787 1 NA X5R C0402 VSSQ101

C788 1 NA X5R C0402 VSSQ102

C789 1 NA X5R C0402 VSSQ103

C790 1 NA X5R C0402 VSSQ104

C791 1 NA X5R C0402 VSSQ105

C792 1 NA X5R C0402 VSSQ106

C793 1 NA X5R C0402 VSSQ107

C794 1 NA X5R C0402 VSSQ108

C795 1 NA X5R C0402 VSSQ109

C796 1 NA X5R C0402 VSSQ110

C797 1 NA X5R C0402 VSSQ111

C798 1 NA X5R C0402 VSSQ112

C799 1 NA X5R C0402 VSSQ113

C800 1 NA X5R C0402 VSSQ114

C801 1 NA X5R C0402 VSSQ115

C802 1 NA X5R C0402 VSSQ116

C803 1 NA X5R C0402 VSSQ117

C804 1 NA X5R C0402 VSSQ118

C805 1 NA X5R C0402 VSSQ119

C806 1 NA X5R C0402 VSSQ120

C807 1 NA X5R C0402 VSSQ121

C808 1 NA X5R C0402 VSSQ122

C809 1 NA X5R C0402 VSSQ123

C810 1 NA X5R C0402 VSSQ124

C811 1 NA X5R C0402 VSSQ125

C812 1 NA X5R C0402 VSSQ126

C813 1 NA X5R C0402 VSSQ127

C814 1 NA X5R C0402 VSSQ128

C815 1 NA X5R C0402 VSSQ129

C816 1 NA X5R C0402 VSSQ130

C817 1 NA X5R C0402 VSSQ131

C818 1 NA X5R C0402 VSSQ132

C819 1 NA X5R C0402 VSSQ133

C820 1 NA X5R C0402 VSSQ134

C821 1 NA X5R C0402 VSSQ135

C822 1 NA X5R C0402 VSSQ136

C823 1 NA X5R C0402 VSSQ137

C824 1 NA X5R C0402 VSSQ138

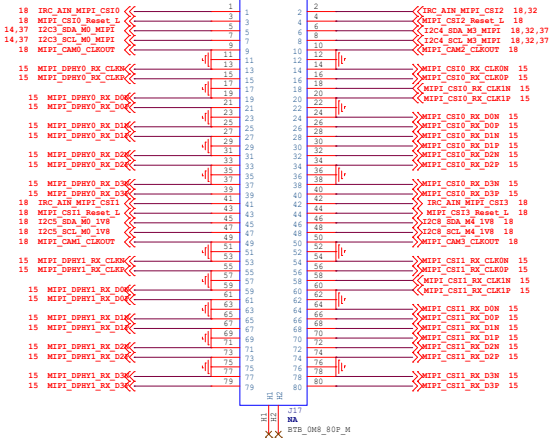
C825 1 NA X5R C0402 VSSQ139

C826 1 NA X5

[illegible]

MIPI D/C PHY0 CSI_RX

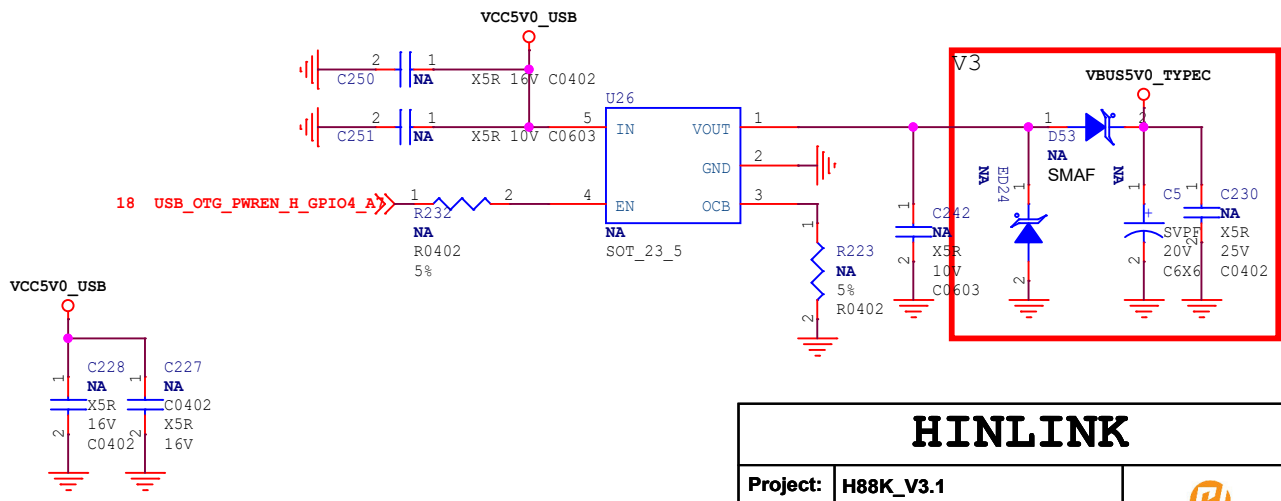
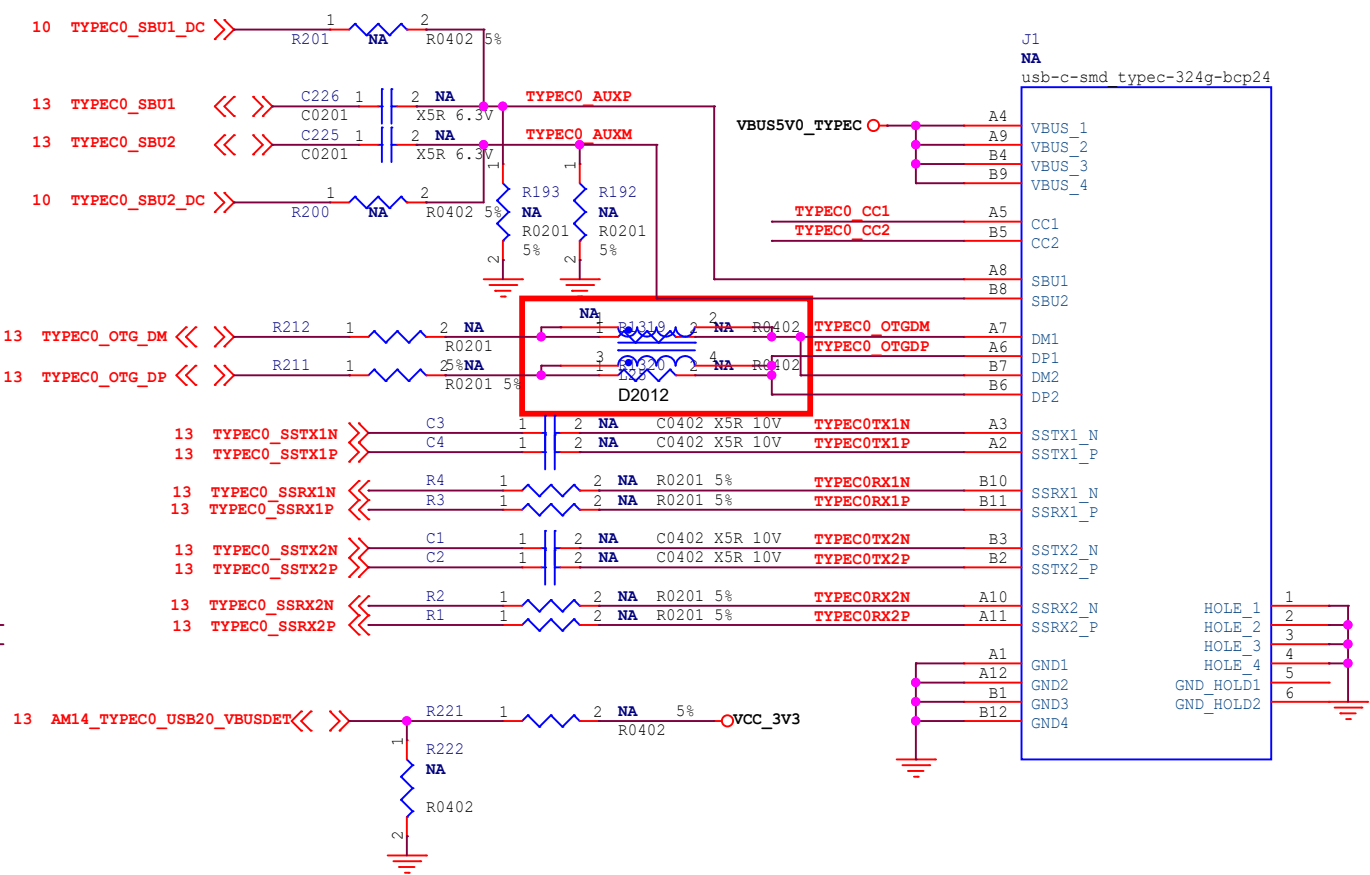
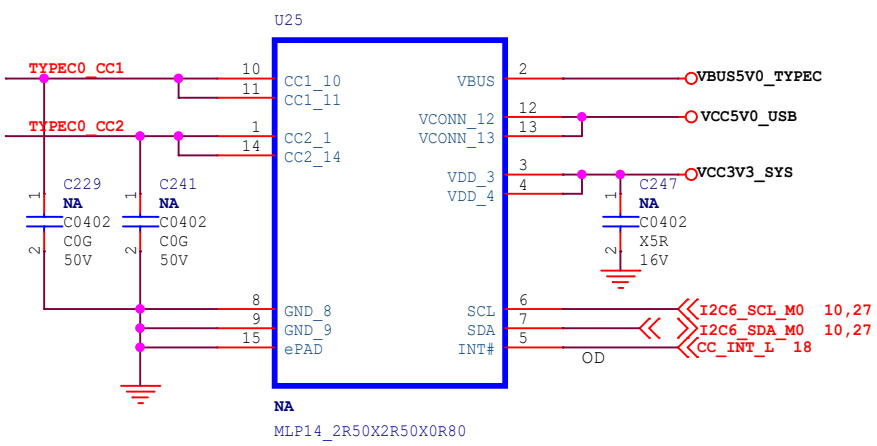
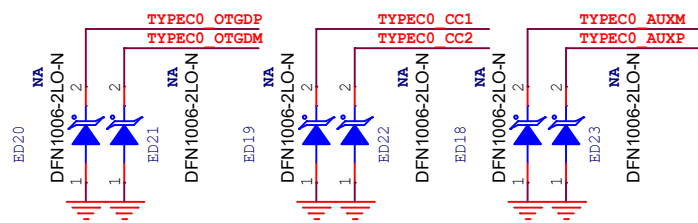
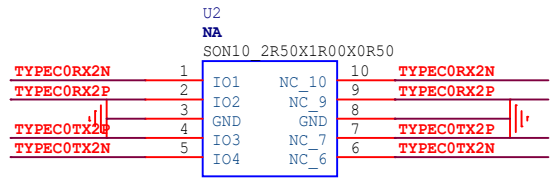
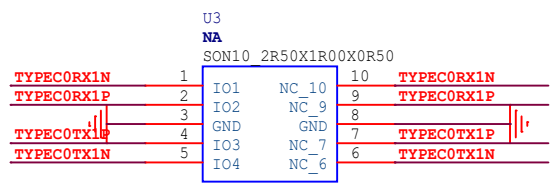
MIPI D/C PHY1 CSI_RX



MIPI-CSI0_RX

MIPI-CSI1_RX

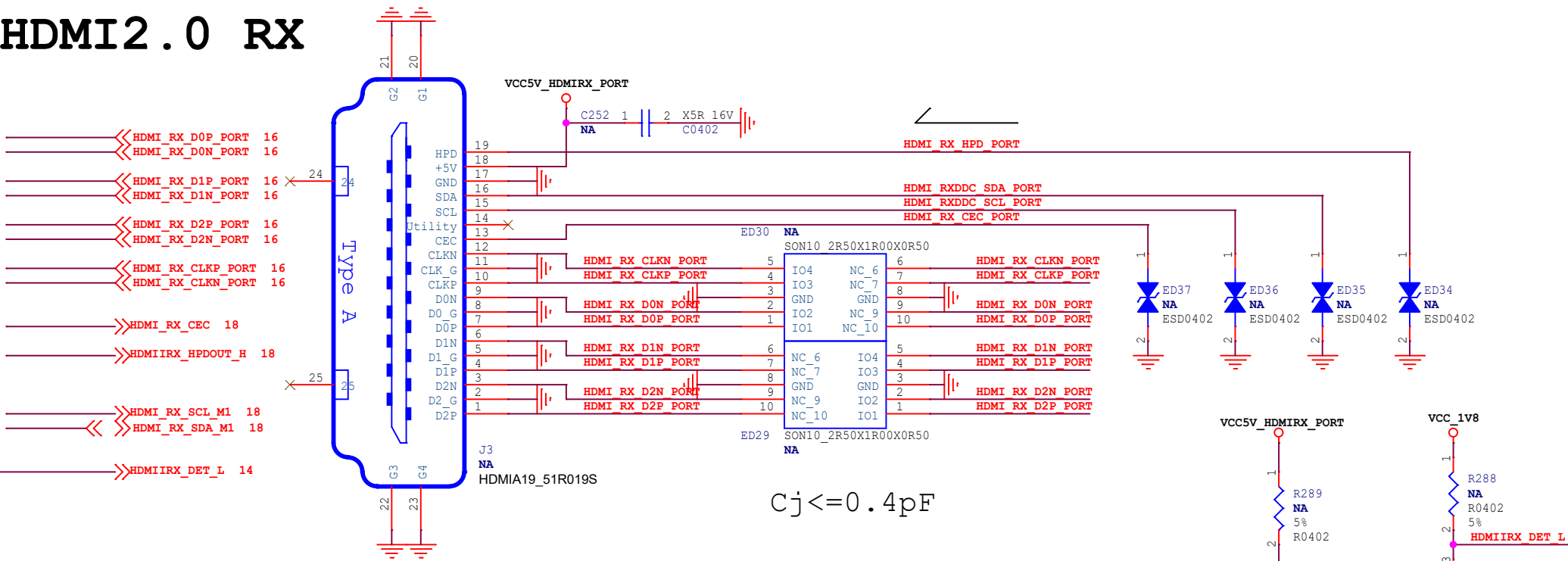
Type-C PORT



HINLINK

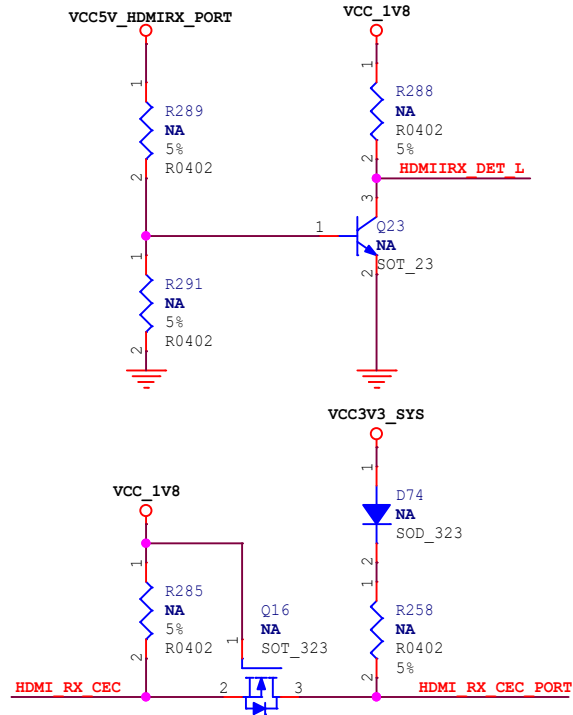
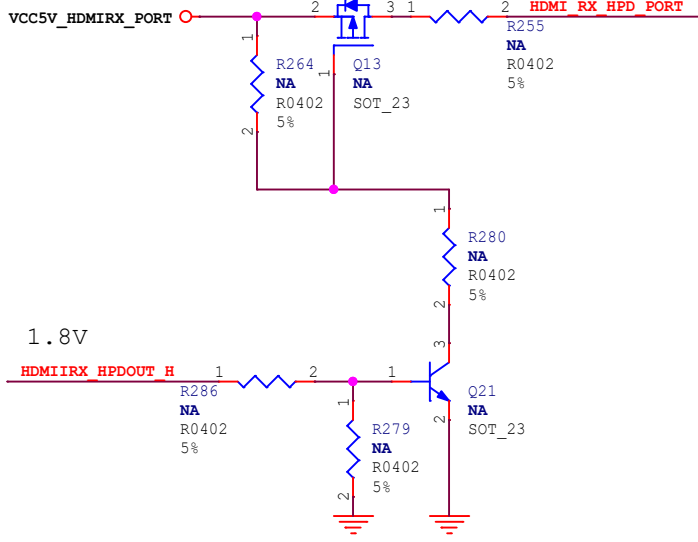
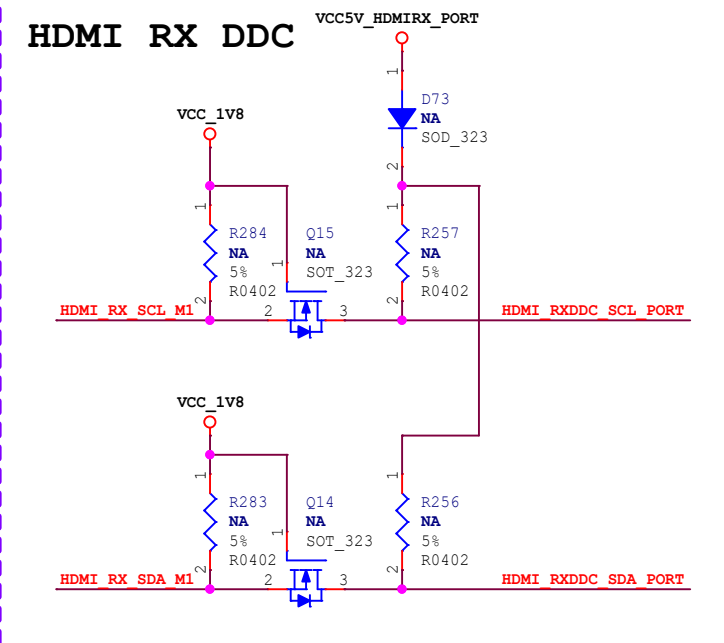
Project:	H88K_V3.1	 HINLINK	
File:	24.PD-TYPE-C		
Date:	Tuesday, June 25, 2024		
Designer:	<designer>		
Rev:	<Revision>	Sheet:	24 of 43

HDMI2.0 RX



$C_j \leq 0.4 \text{ pF}$

HDMI RX DDC



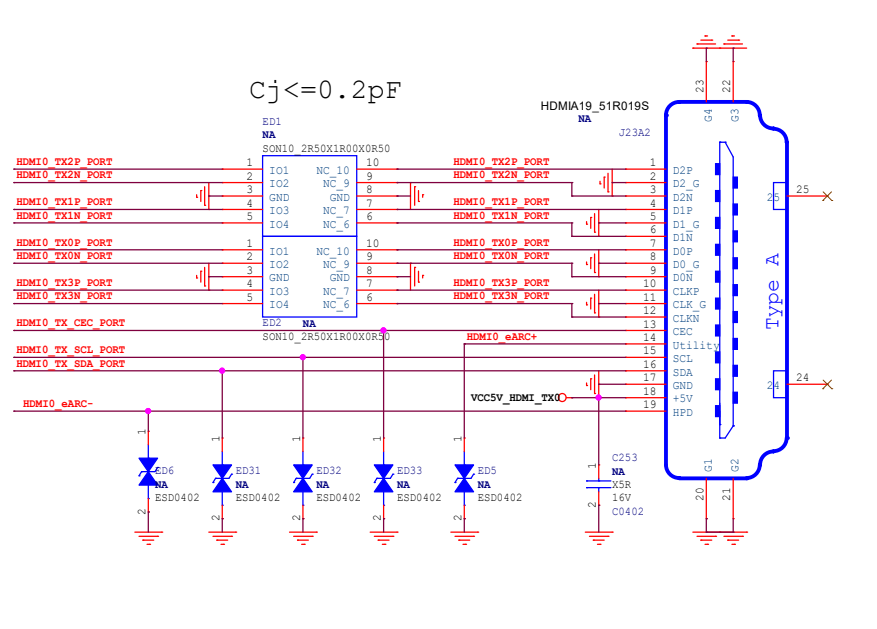
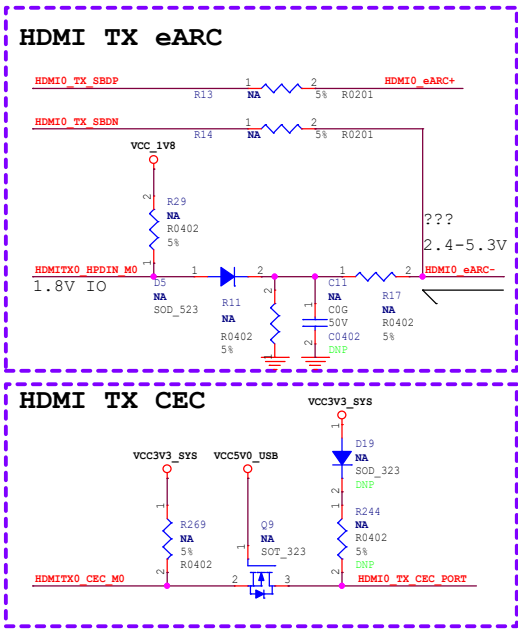
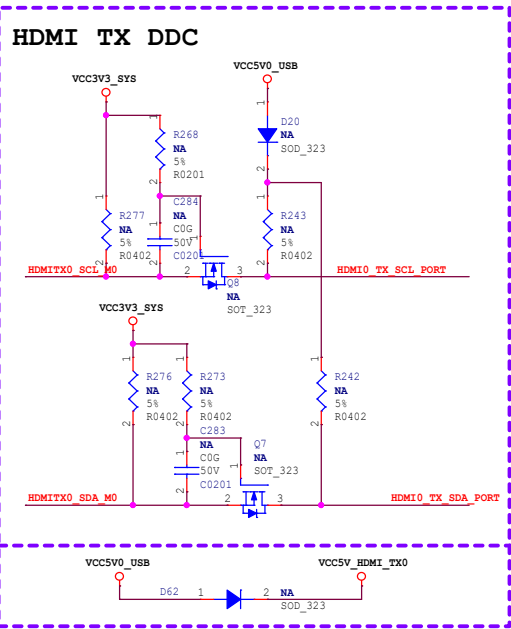
HPD:
Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side:Require input and Detection.
Min 2.0V,Max:5.3V.

HINLINK

Project:	H88K_V3.1	
File:	25.VI-HDMI2.0 RX	
Date:	Tuesday, June 25, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 25 of 43

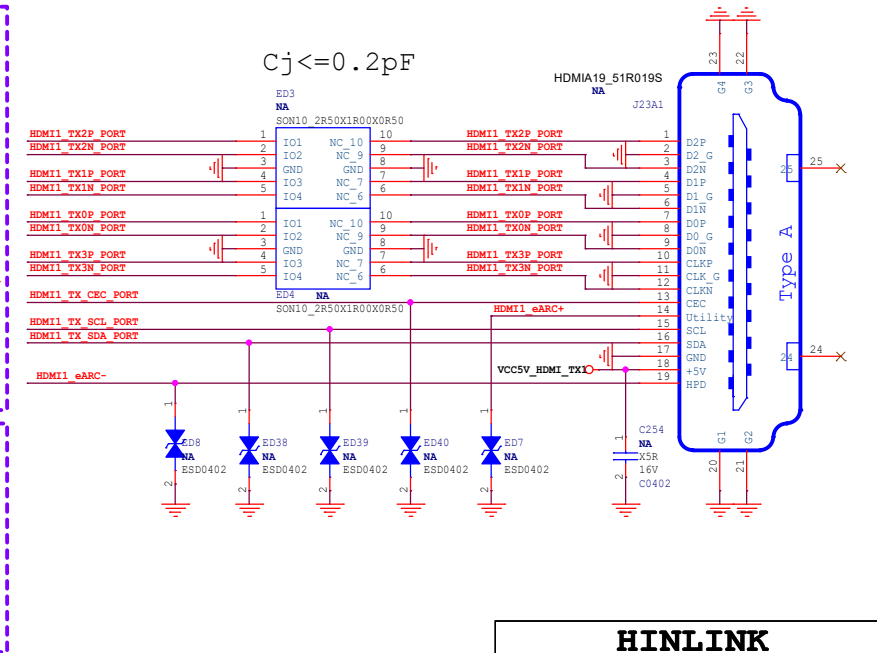
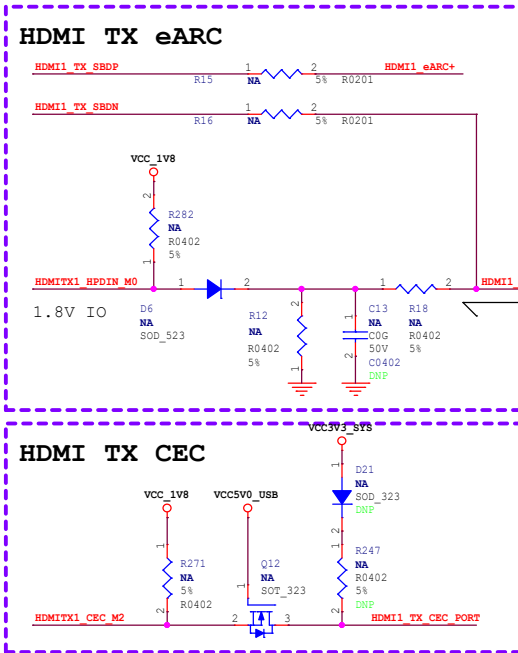
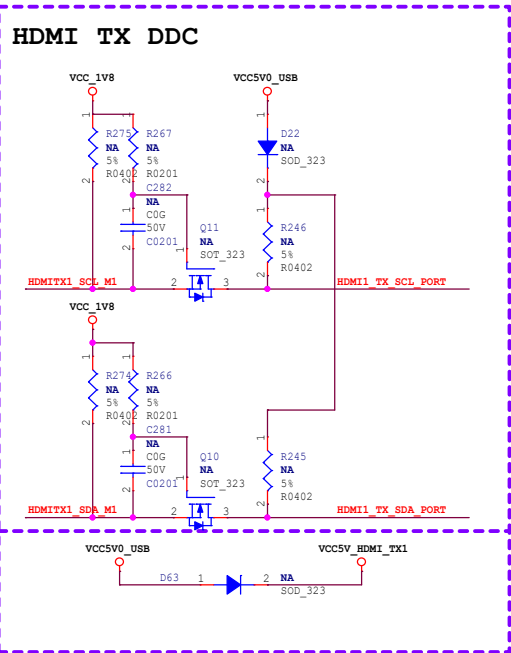
HDMI TX0

- >>> HDMI_TX_SBDP 16
- >>> HDMI_TX_SBDN 16
- >>> HDMI_TX0P_PORT 16
- >>> HDMI_TX0N_PORT 16
- >>> HDMI_TX1P_PORT 16
- >>> HDMI_TX1N_PORT 16
- >>> HDMI_TX2P_PORT 16
- >>> HDMI_TX2N_PORT 16
- >>> HDMI_TX3P_PORT 16
- >>> HDMI_TX3N_PORT 16
- <<< HDMI_TX0_SDA_M0 18
- <<< HDMI_TX0_SCL_M0 18
- <<< HDMI_TX0_CEC_M0 18
- <<< HDMI_TX0_HPDIN_M0 18

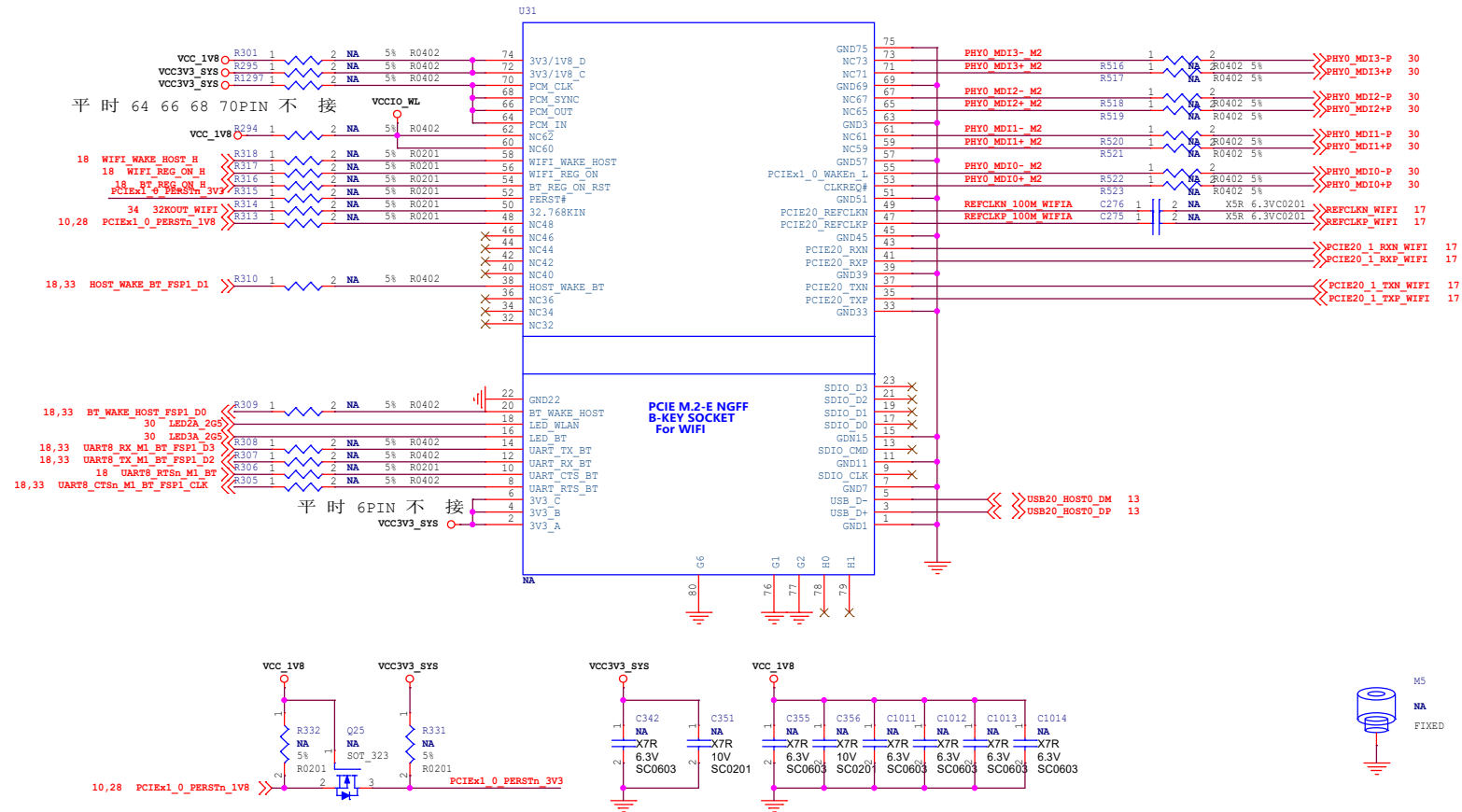


HDMI TX1

- >>> HDMI1_TX_SBDP 16
- >>> HDMI1_TX_SBDN 16
- >>> HDMI1_TX0P_PORT 16
- >>> HDMI1_TX0N_PORT 16
- >>> HDMI1_TX1P_PORT 16
- >>> HDMI1_TX1N_PORT 16
- >>> HDMI1_TX2P_PORT 16
- >>> HDMI1_TX2N_PORT 16
- >>> HDMI1_TX3P_PORT 16
- >>> HDMI1_TX3N_PORT 16
- <<< HDMI_TX1_SDA_M1 18
- <<< HDMI_TX1_SCL_M1 18
- <<< HDMI_TX1_CEC_M2 18
- <<< HDMI_TX1_HPDIN_M0 18

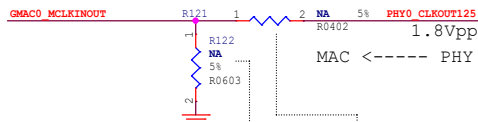
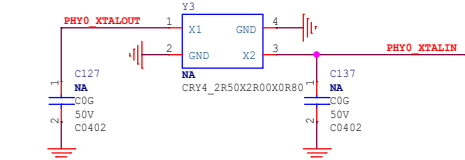


PCIe WIFI6/BT Module-2T2R



HINLINK			
Project:	H88K_V3.1	 HINLINK	
File:	28.WIF/BT-M2		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 43

GMACO_TXD0 14
GMACO_TXD1 14
GMACO_TXD2 14
GMACO_TXD3 14
GMACO_TXEN 14
GMACO_TXCLK 14
GMACO_RXD0 14
GMACO_RXD1 14
GMACO_RXD2 14
GMACO_RXD3 14
GMACO_RXDV_CRS 14
GMACO_RXCLK 14
GMACO_MCLKINOUT 14
GMACO_MDC 14
GMACO_MDIO 14
GMACO_RSTn_L_GPIO4_B3 18



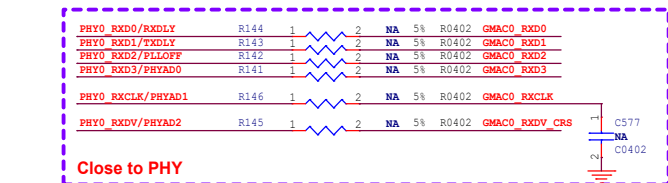
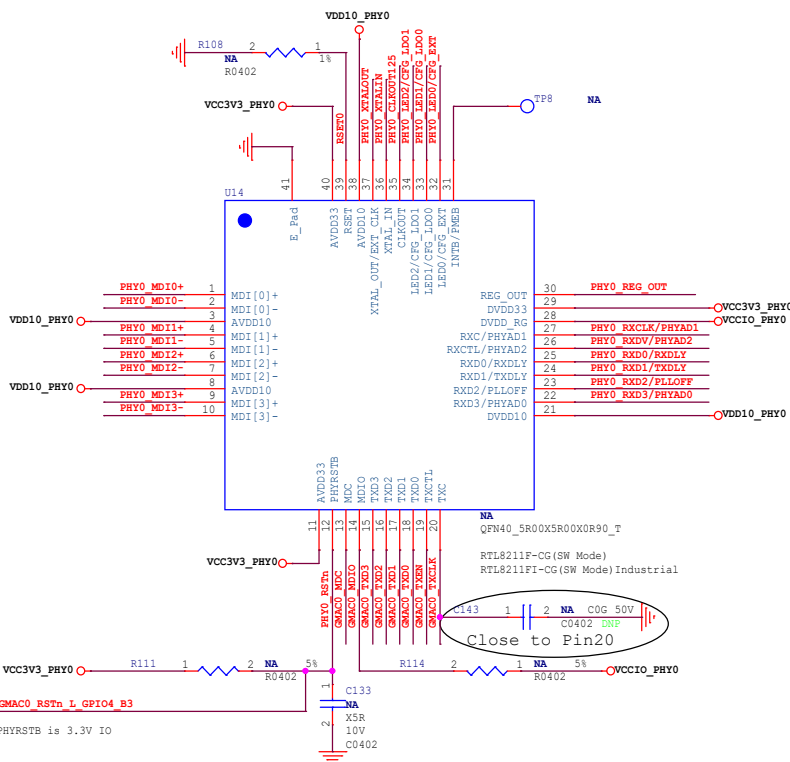
VCCIO_PHY0=3.3V	DNP	22R	Default
VCCIO_PHY0=1.8V	120R	100R	

PHY0_LED2/CFG_LD01
PHY0_LED1/CFG_LD00

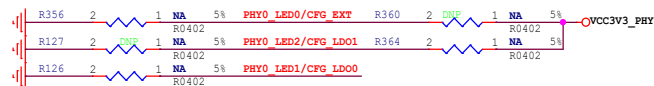
PHY0_MD13-
PHY0_MD13+
PHY0_MD12-
PHY0_MD12+
PHY0_MD11-
PHY0_MD11+
PHY0_MD10-
PHY0_MD10+

PHY0_LED2/CFG_LD01 30
PHY0_LED1/CFG_LD00 30

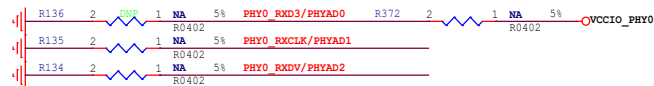
PHY0_MD13- 30
PHY0_MD13+ 30
PHY0_MD12- 30
PHY0_MD12+ 30
PHY0_MD11- 30
PHY0_MD11+ 30
PHY0_MD10- 30
PHY0_MD10+ 30



Rockchip Confidential



VCC_PHY0_IO Voltage Config



PHY Address Config



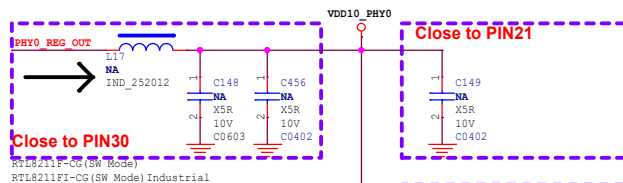
Pull-up for additional 2ns delay to RXC for data latching



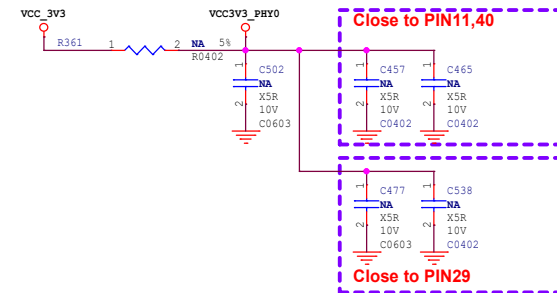
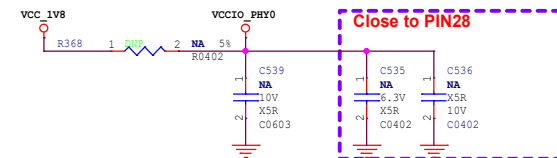
Pull-up for additional 2ns delay to TXC for data latching



Pull-up to disable PLL @ ALDPS mode(Low power mode)



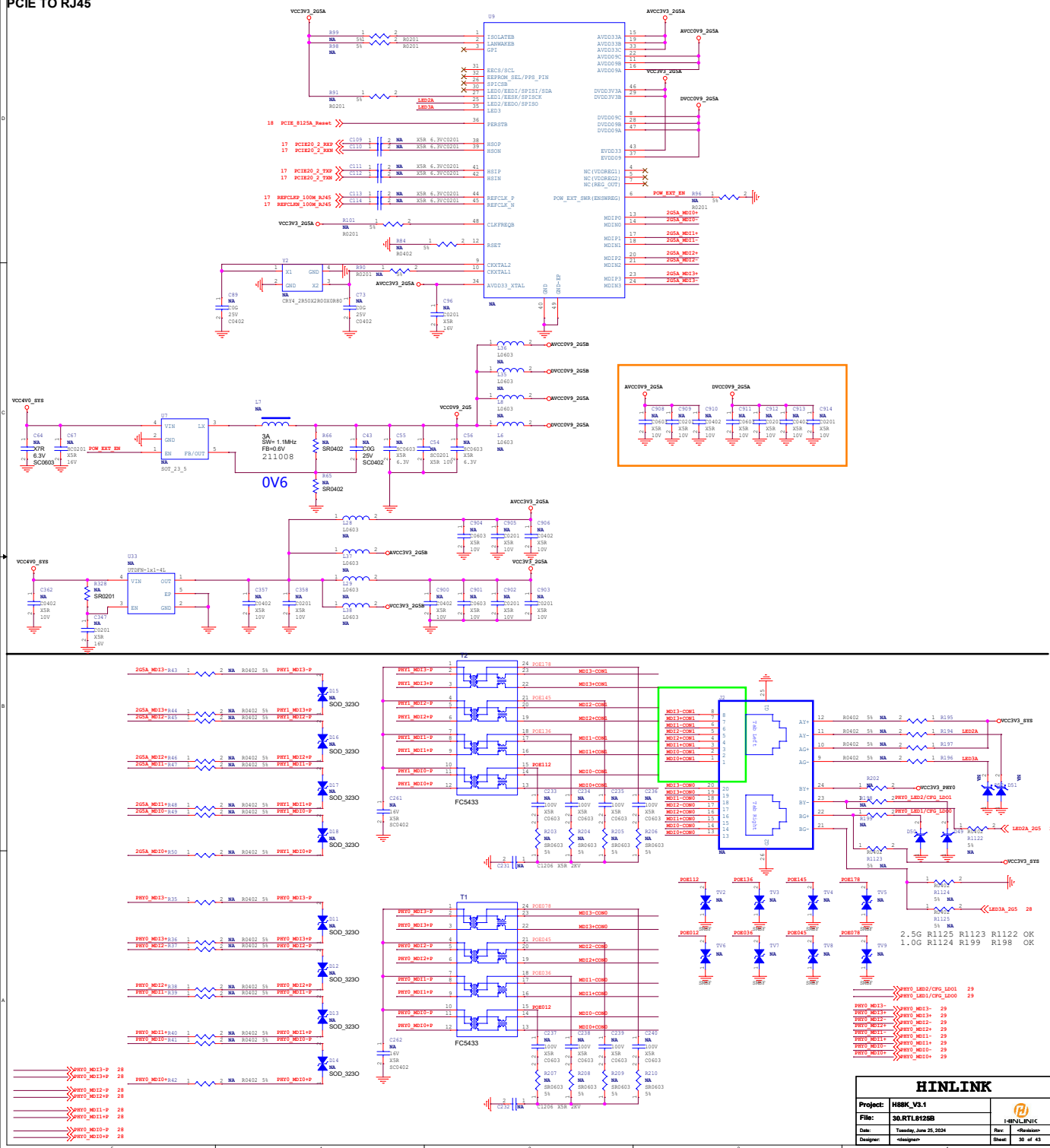
RGMI Power Source	CFG EXT	CFG LDO[1:0]
External 3.3V	1'b1	2'b00
External 1.8V	1'b1	2'b10
Internal 1.8V (default)	1'b0	2'b10



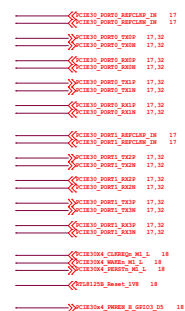
HINLINK

Project:	H88K_V3.1	Rev:	<Revision>
File:	29.RTL8211F	Sheet:	29 of 43
Date:	Tuesday, June 25, 2024		
Designer:	<designer>		

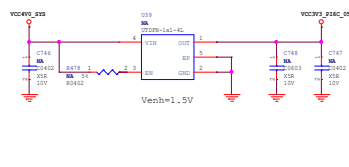
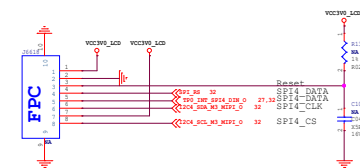
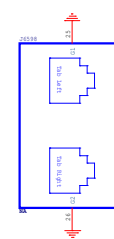
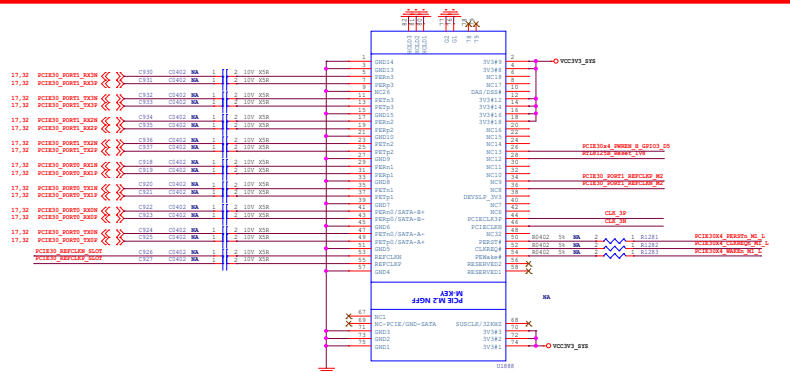
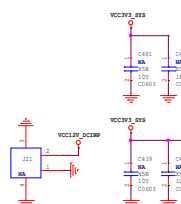
PCIE TO RJ45



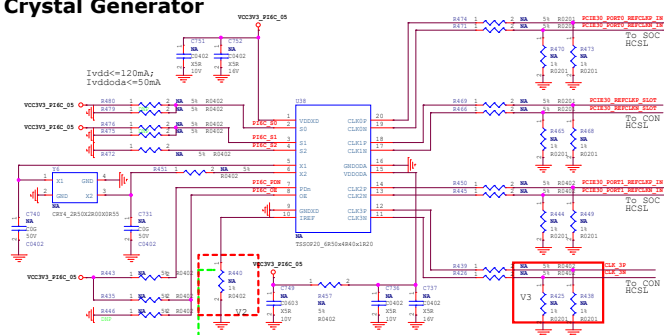
PCIe3.0 x 4 Slot



M2 PCIE SSD

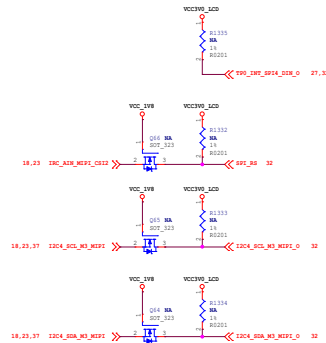


Crystal Generator

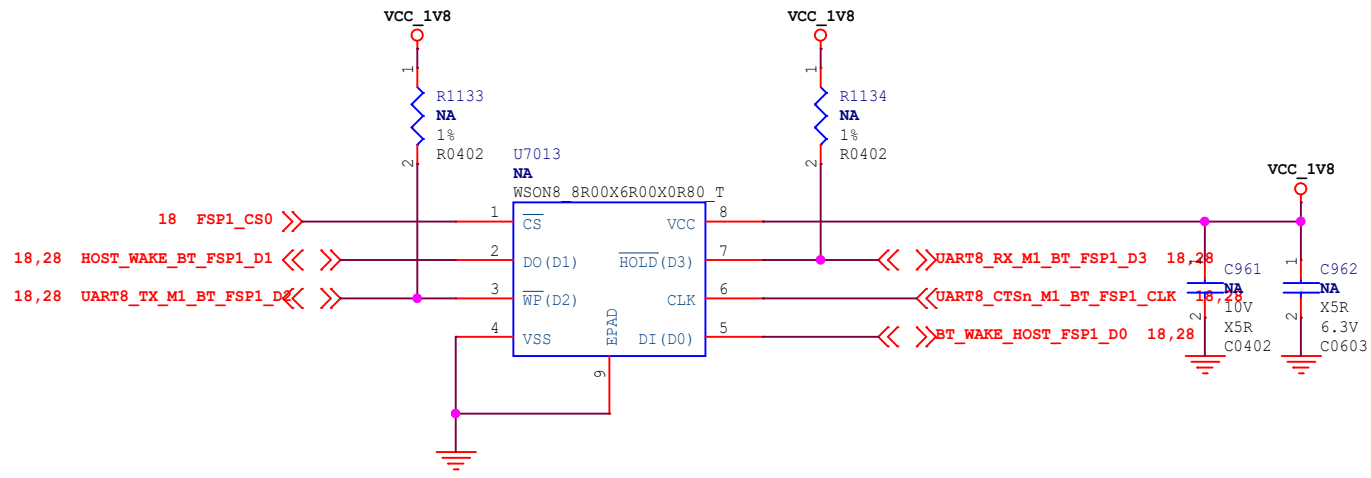


SS0	SS1	Spread(%)
0	0	Center+/-0.2
1	0	-0.5
0	1	-0.75
1	1	No Spread

If board target trace impedance is 50ohm then $R = 475\text{ohm}$ providing an IREF of 2.32 mA. The output current (IOH) is $6 * \text{IREF}$.
 $V_{ih} = 6 \times 2.32 \times 50 = 696\text{mV}$

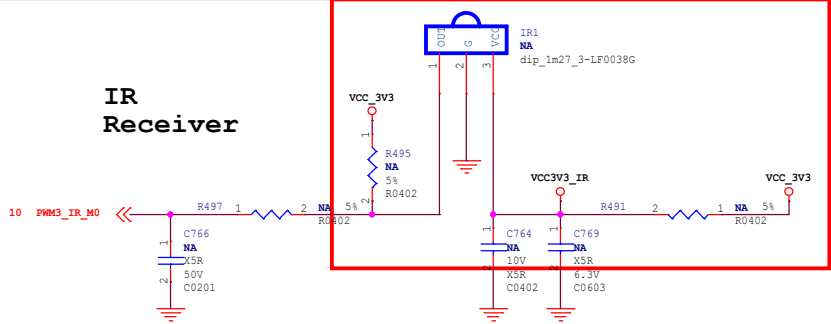


HINLINK			
Project:	H88K_V3.1	 HINLINK	
File:	32.PCE-PCIE3.0_Slot		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<Designer>	Sheet:	32 of 43

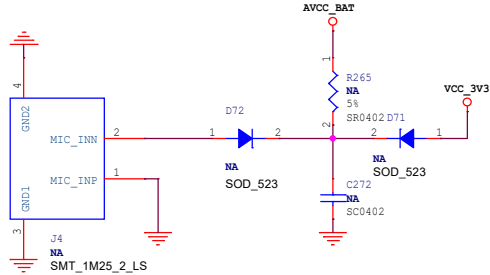
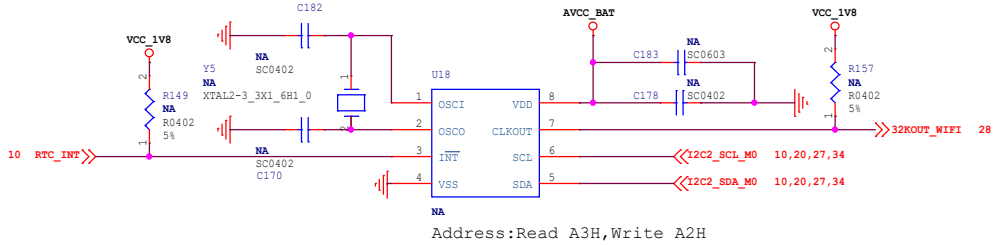


HINLINK			
Project:	H88K_V3.1		
File:	33.NAND_Flash		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	33 of 43

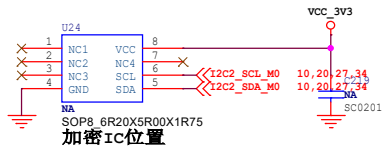
IR
Receiver



RTC IC

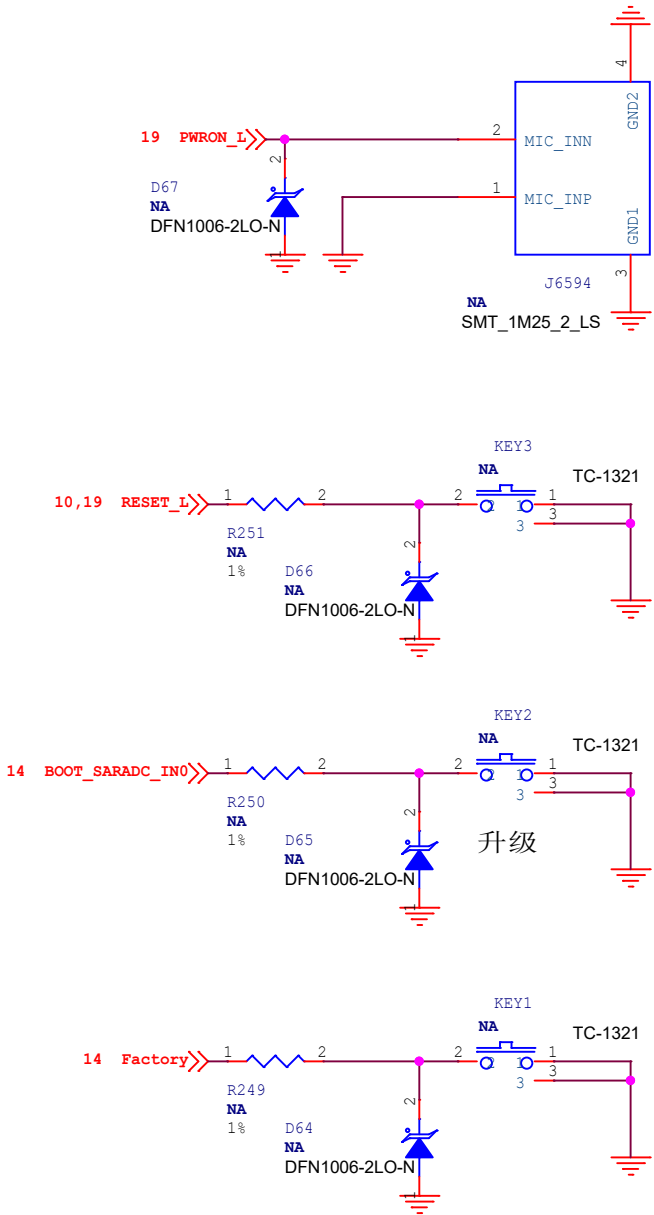


Encryption



KEY

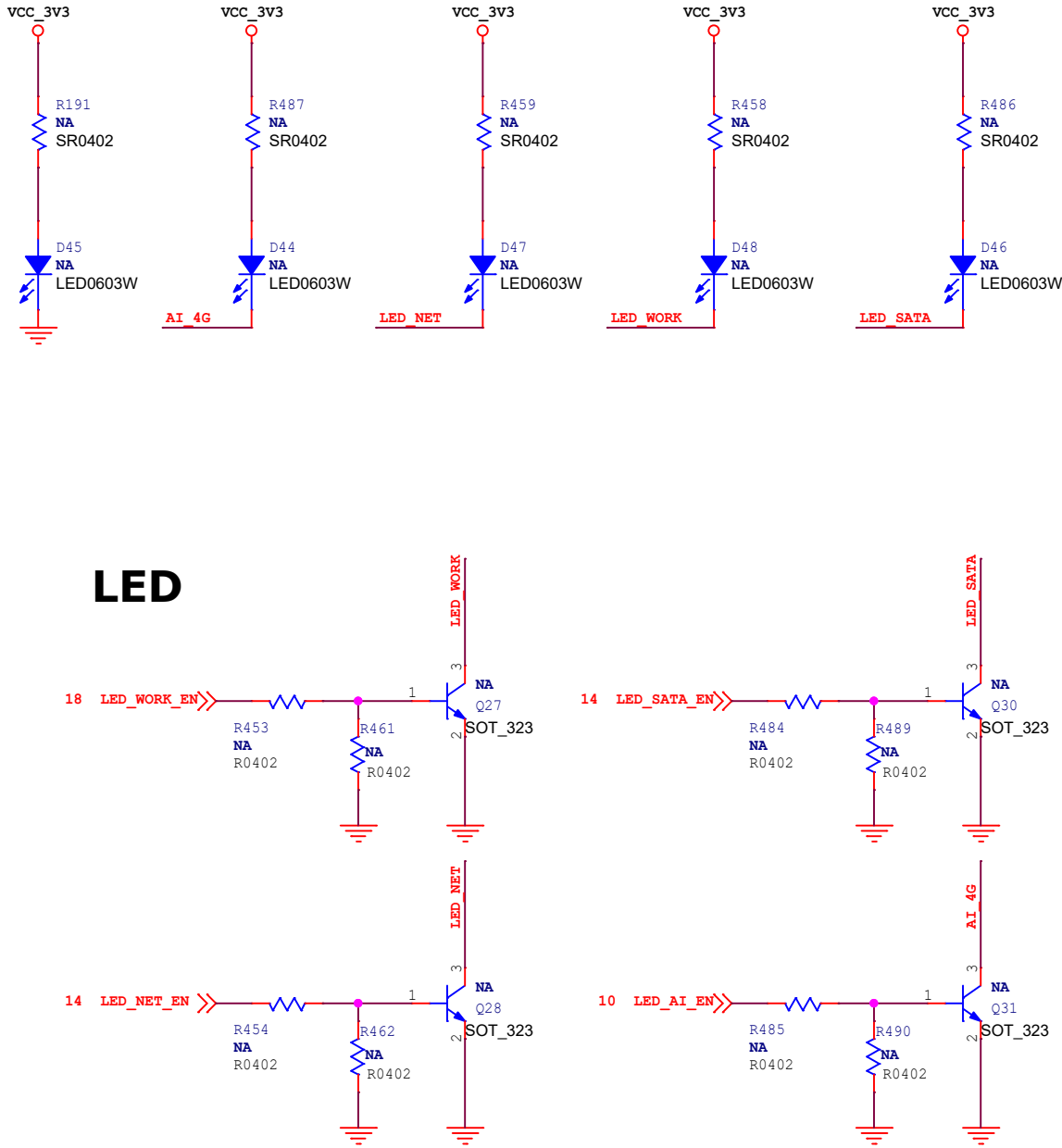
回复出厂配置



Note:

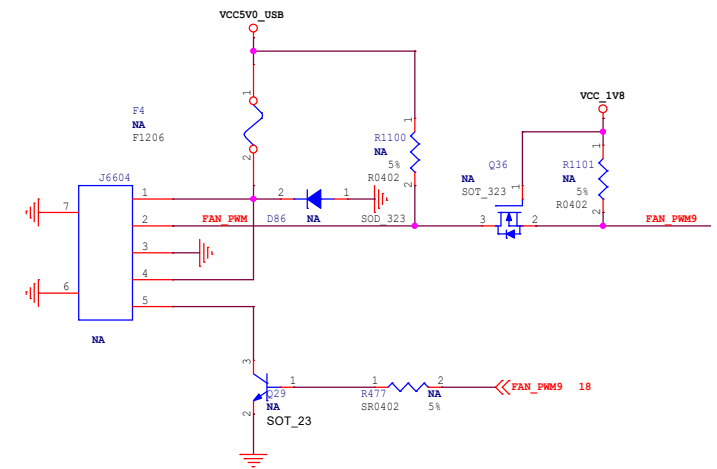
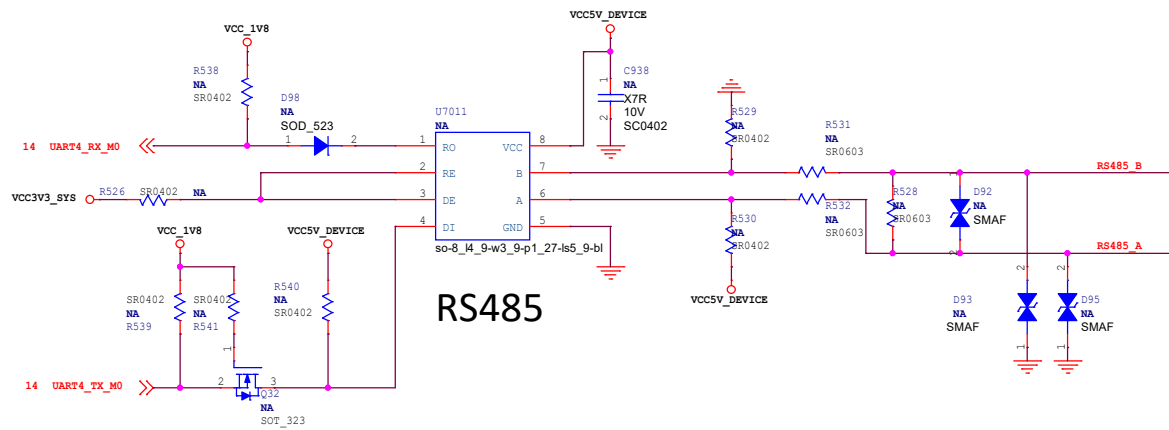
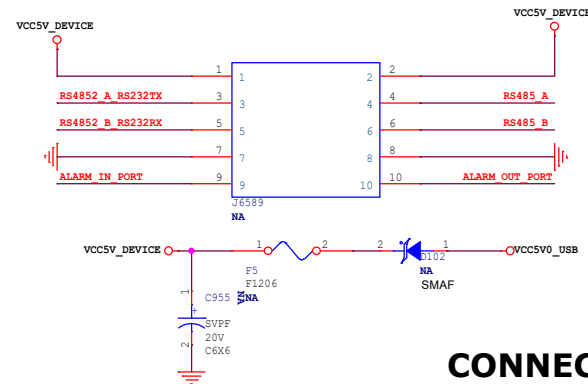
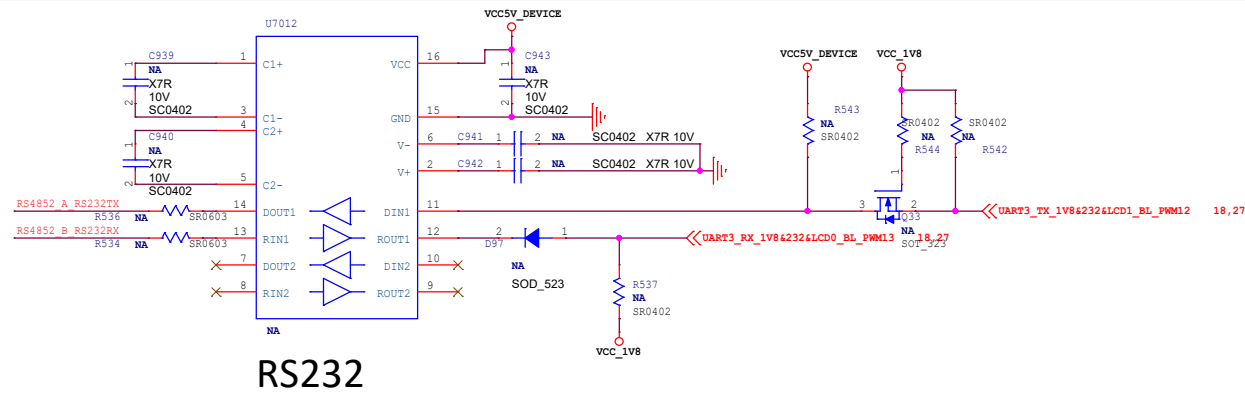
If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.

LED

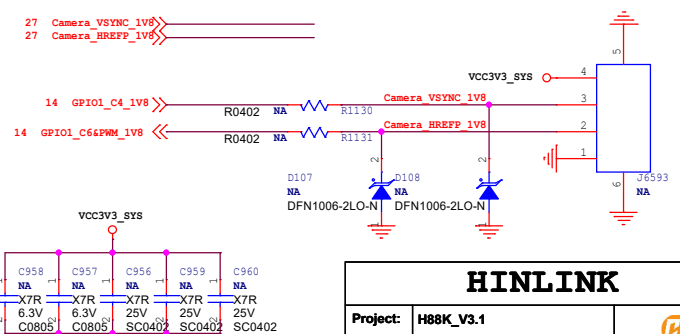


HINLINK

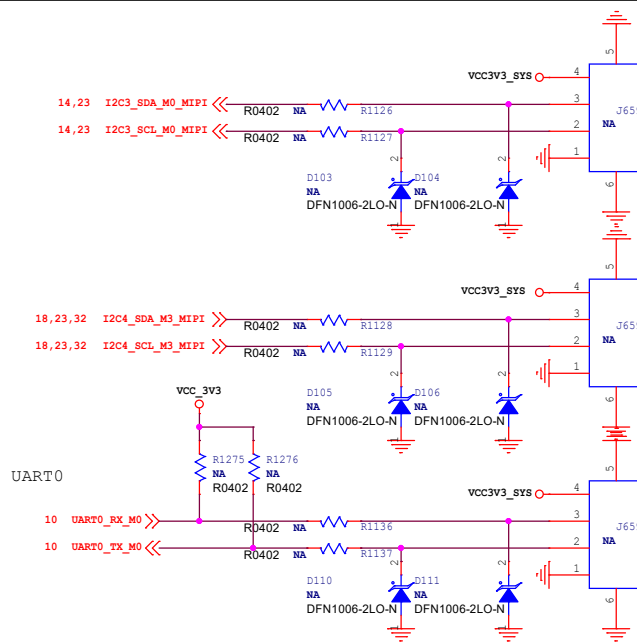
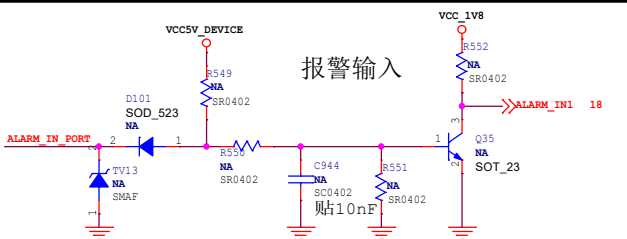
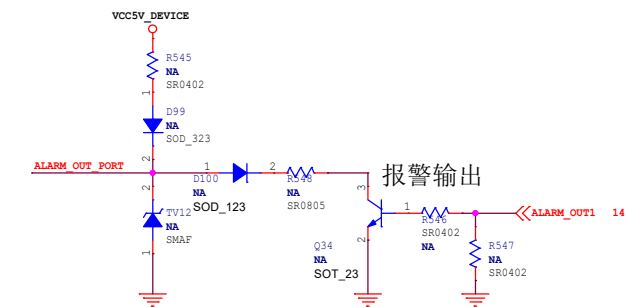
Project:	H88K_V3.1	
File:	36.KEY_Array	
Date:	Tuesday, June 25, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 36 of 43

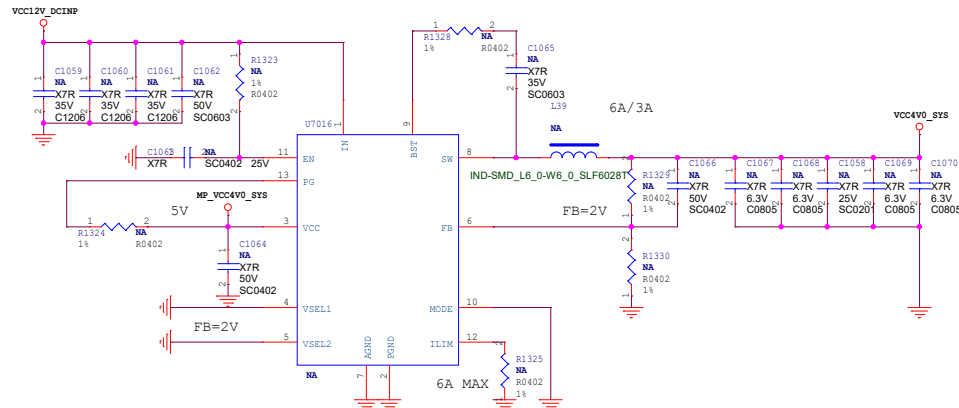
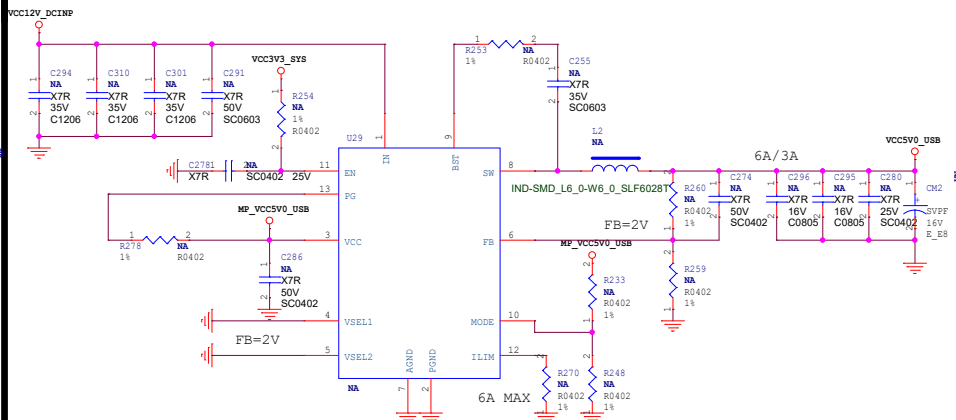
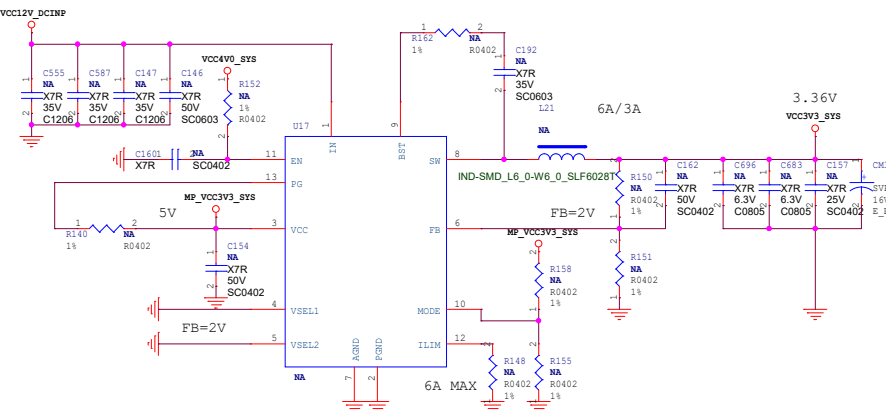
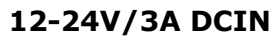
**FAN_POWER**

CONNECT



HINLINK			
Project:	H88K_V3.1	 HINLINK	
File:	37_RS485&232&FAN		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	37 of 43

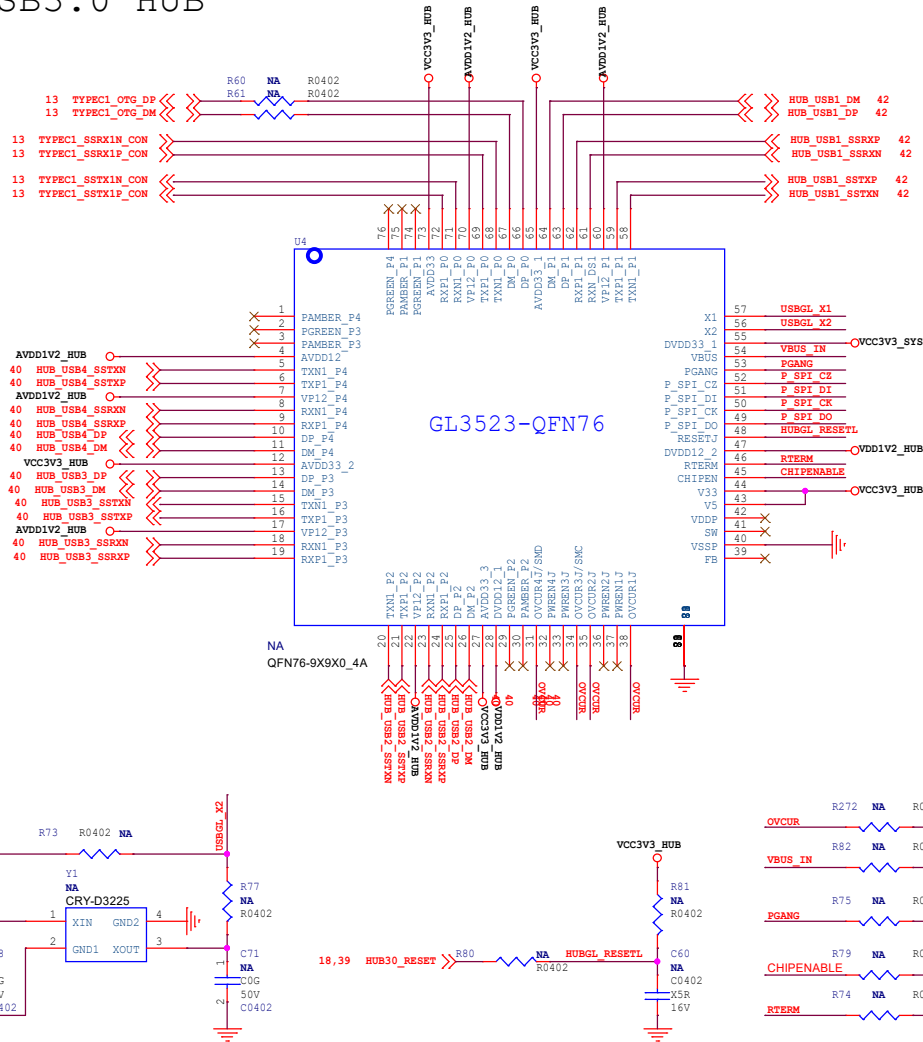




HINLINK			
Project:	H88K_V3.1	 HINLINK	
File:	38.POWER_IN		
Date:	Tuesday, June 25, 2024		
Designer:	<designer>	Rev:	<Revision>
		Sheet:	38 of 43

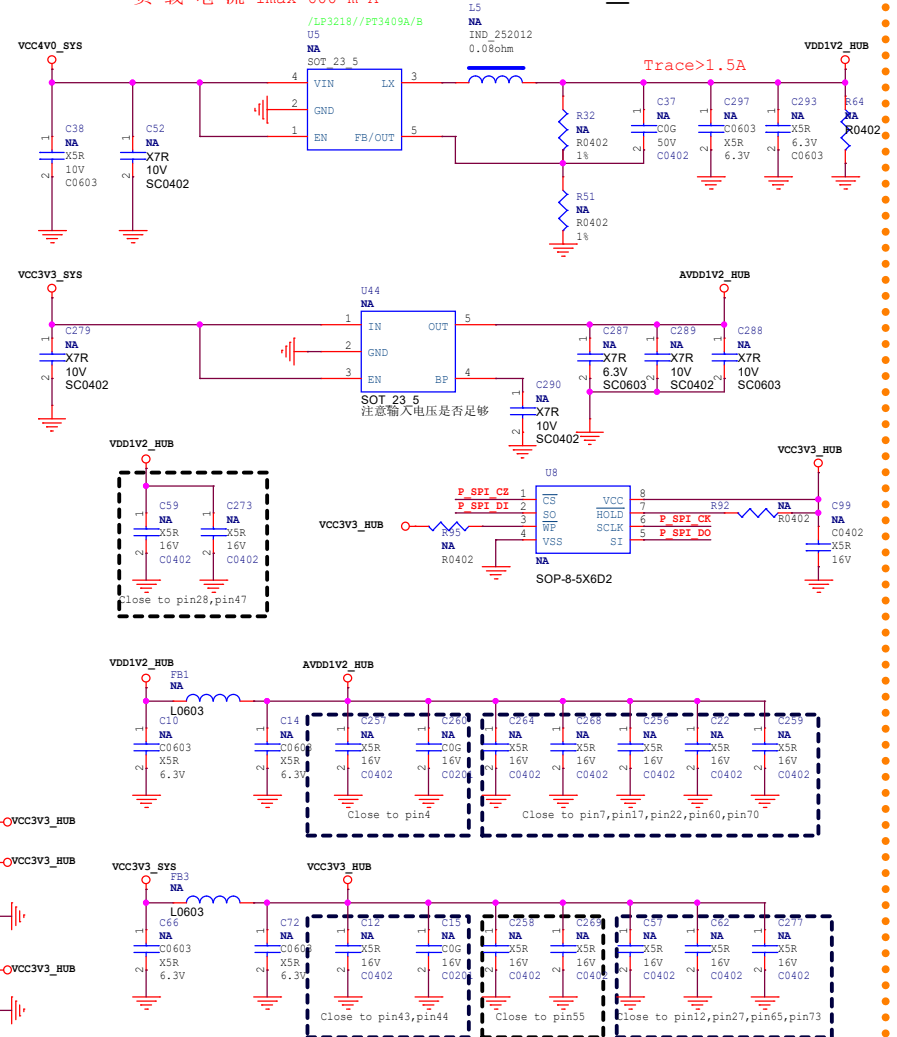
USB3.0 HUB

HUB30_RESET 18,39



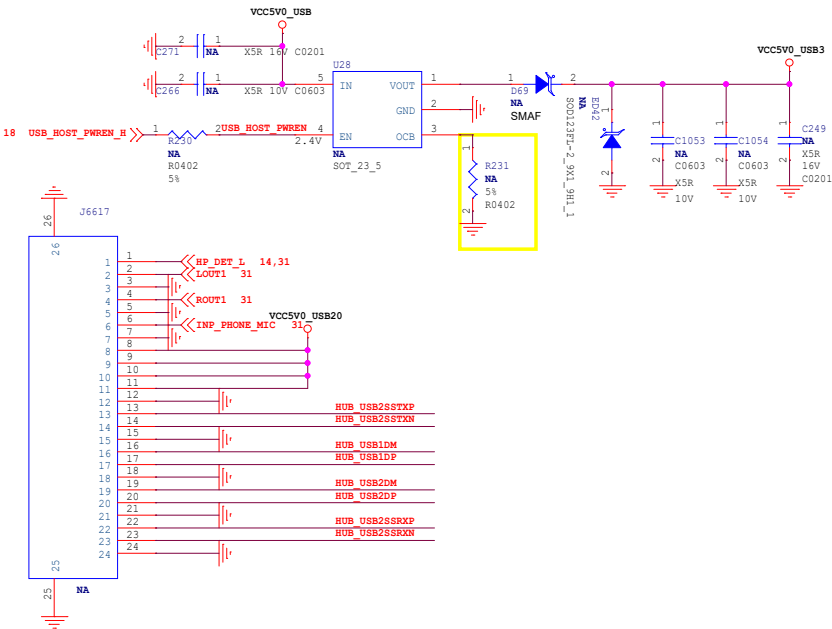
HUB_POWER

负载电流 $I_{max}=600\text{ mA}$

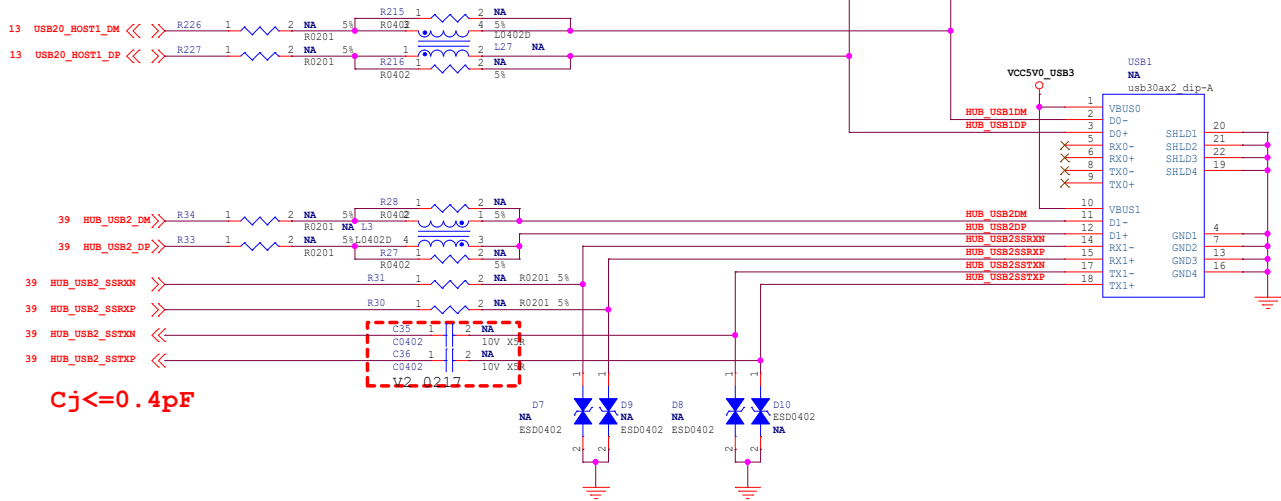


HINLINK

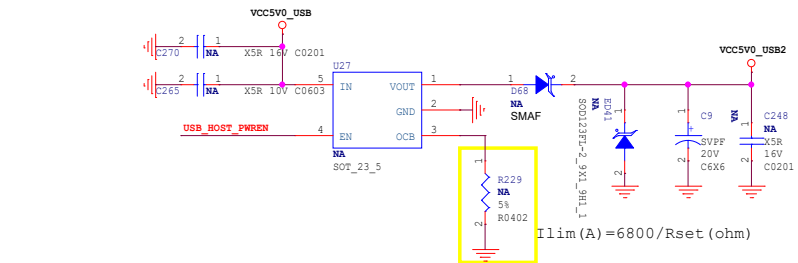
Project:	H88K_V3.1	Rev:	<Revision>
File:	39.USB_HUB	Sheet:	39 of 43
Date:	Tuesday, June 25, 2024		
Designer:	<designer>		



USB3.0 HOST PORT

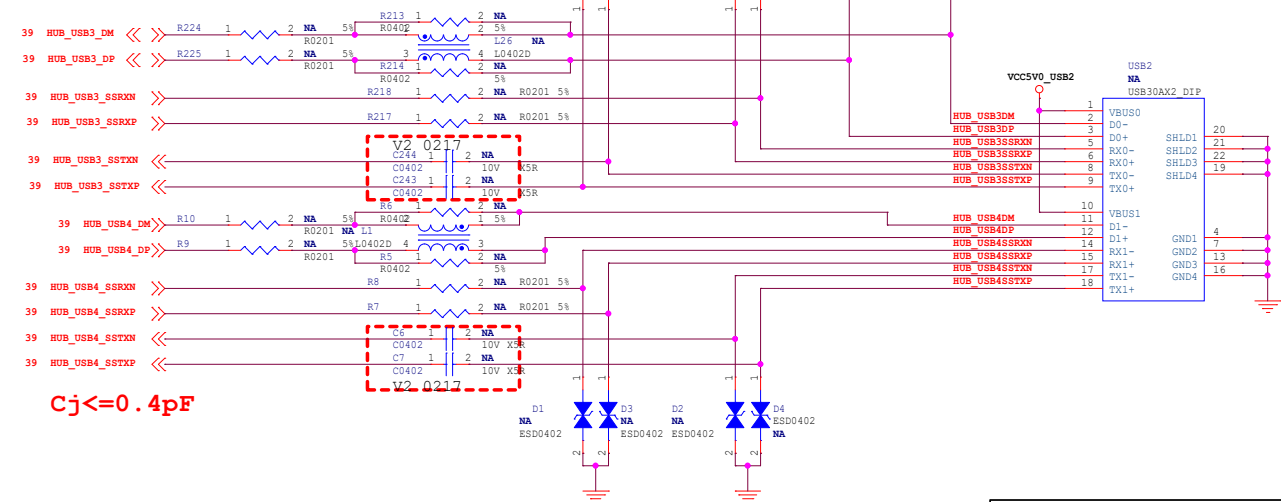


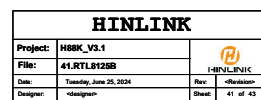
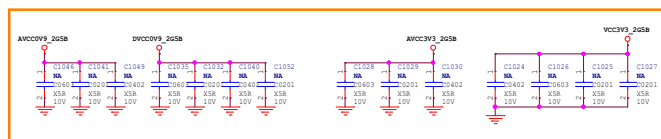
Cj<=0.4pF



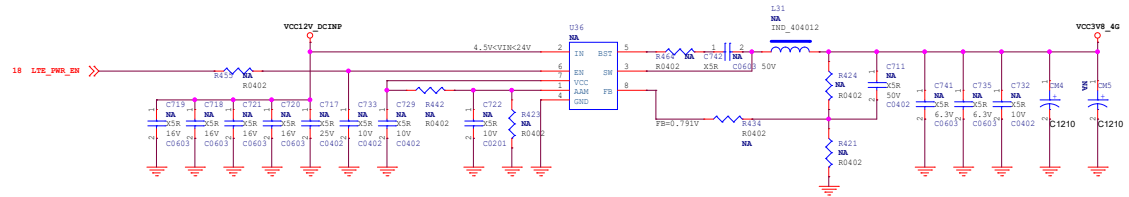
Ilim (A) = 6800/Rset (ohm)

USB3.0 HOST PORT

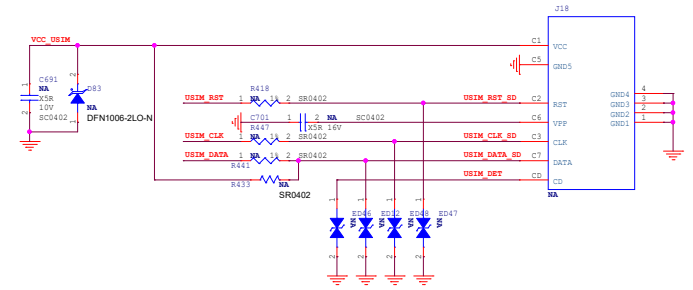




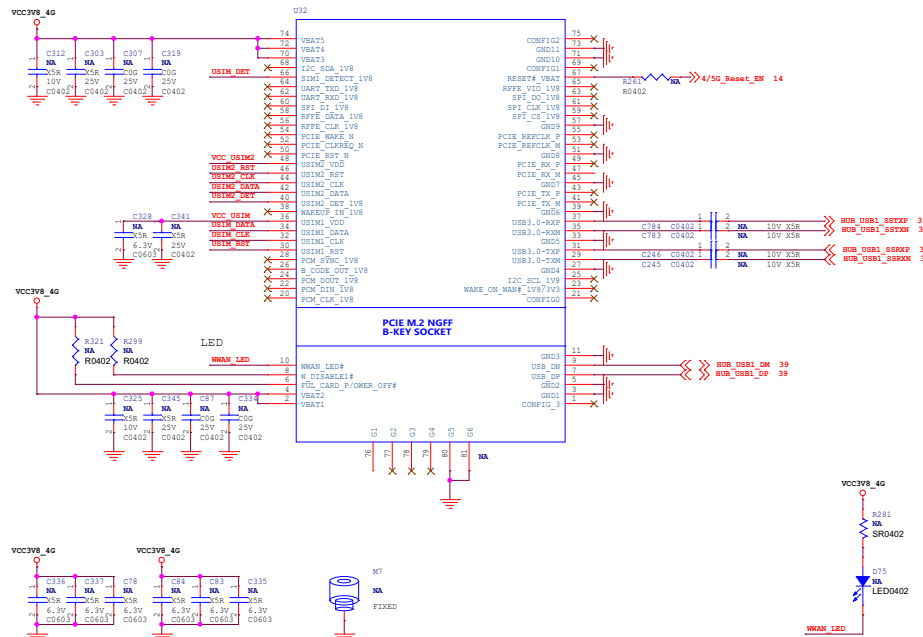
12V->3.8V

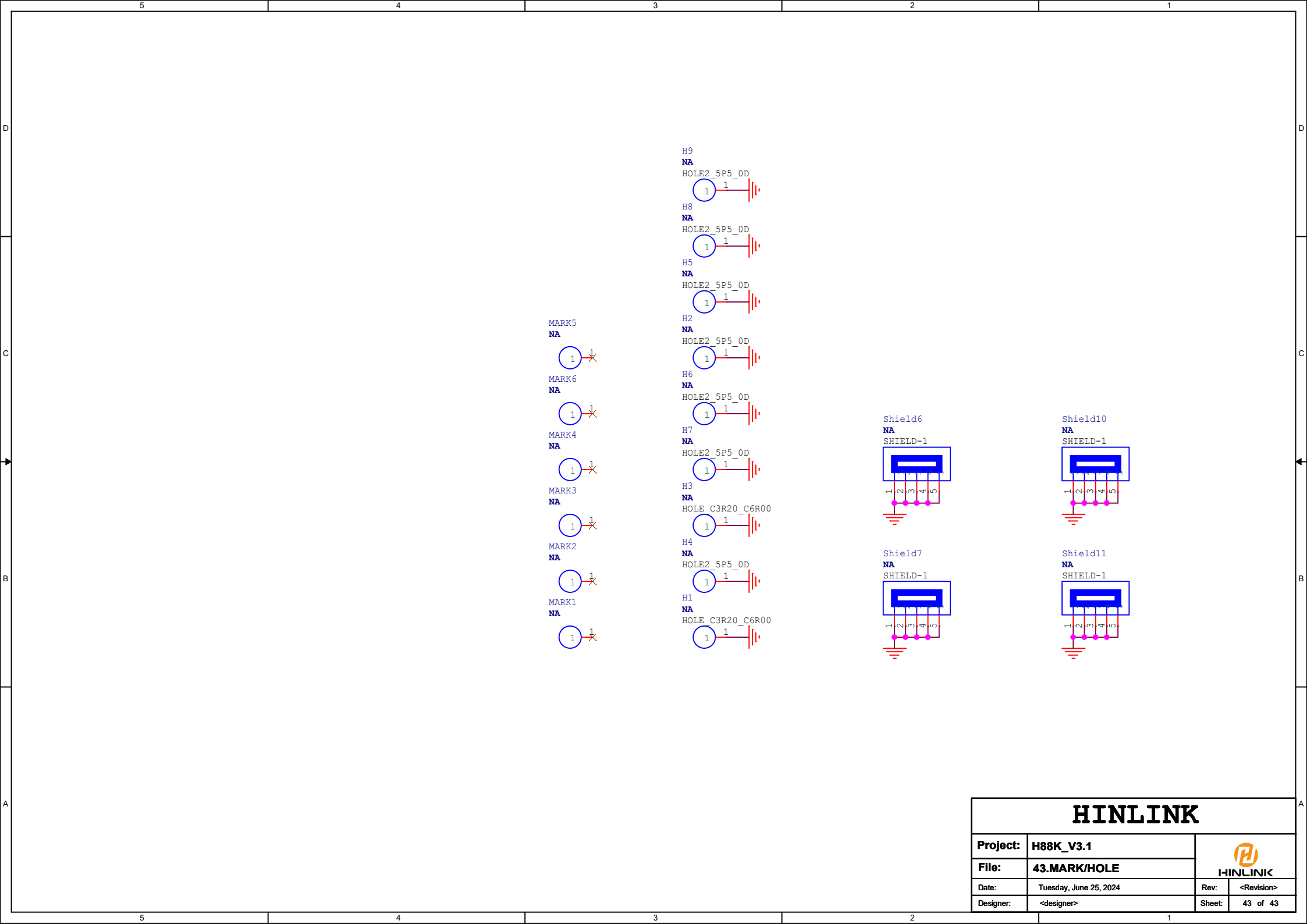


4G/5G SIM1 CARD



M2_NGFF-4G/5G





HINLINK			
Project:	H88K_V3.1	 HINLINK	
File:	43.MARK/HOLE		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	43 of 43