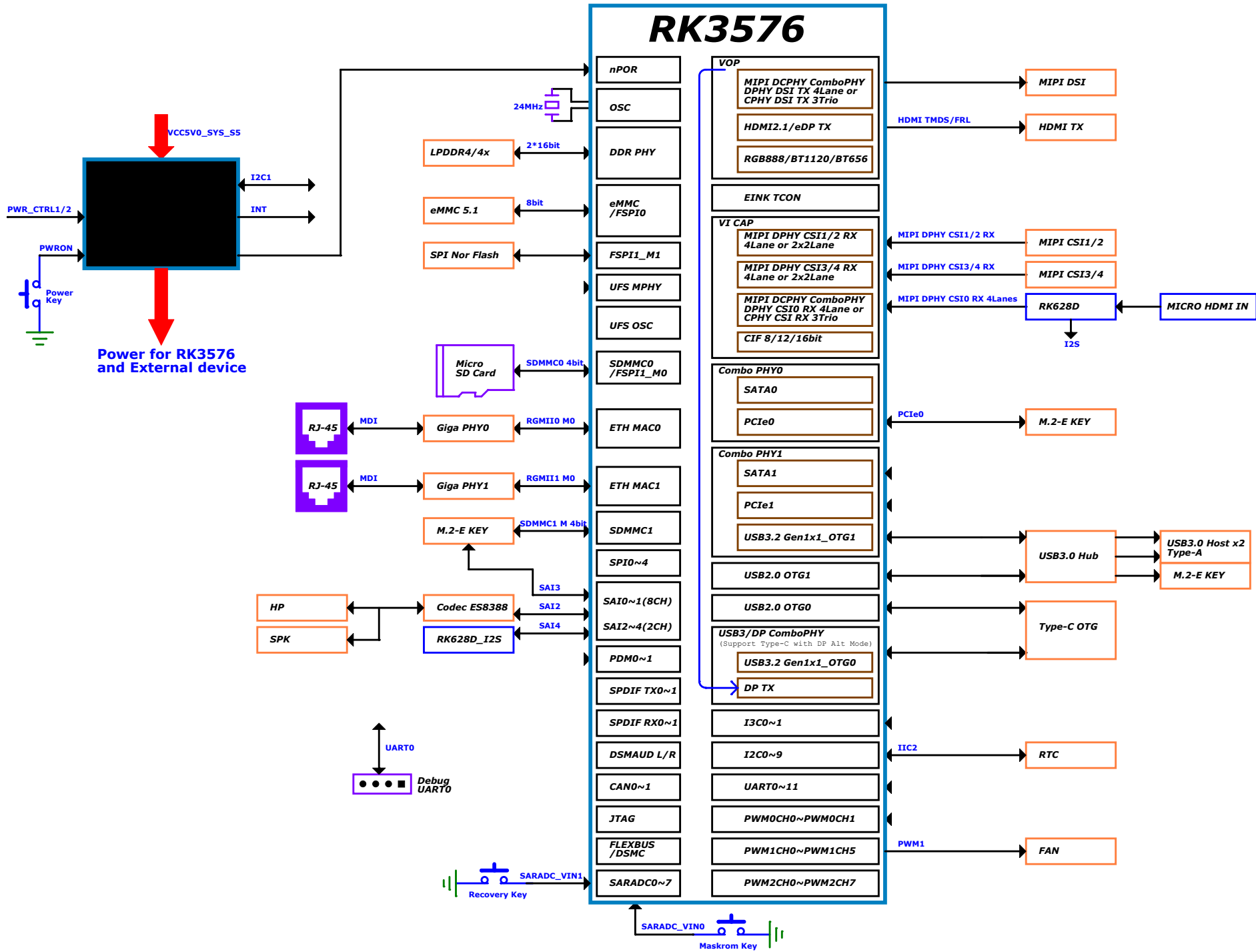


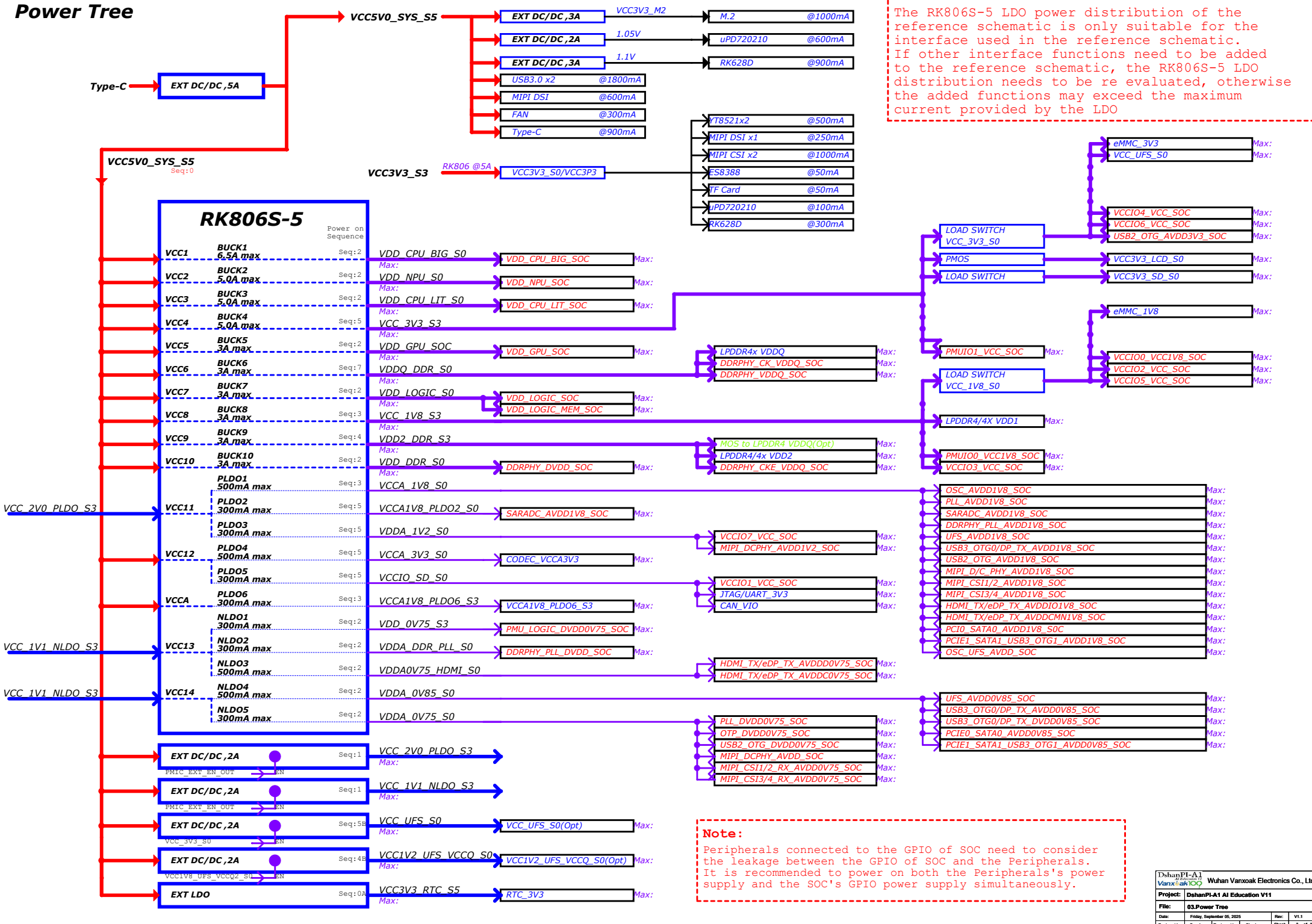
Revision History

Version	Date	By	Change Dscription	Approved
V1.0	2025-04-25		1: Draft version;	
V1.1	2025-07-17			

RK3576 Ref Block Diagram(Typical Application Case)



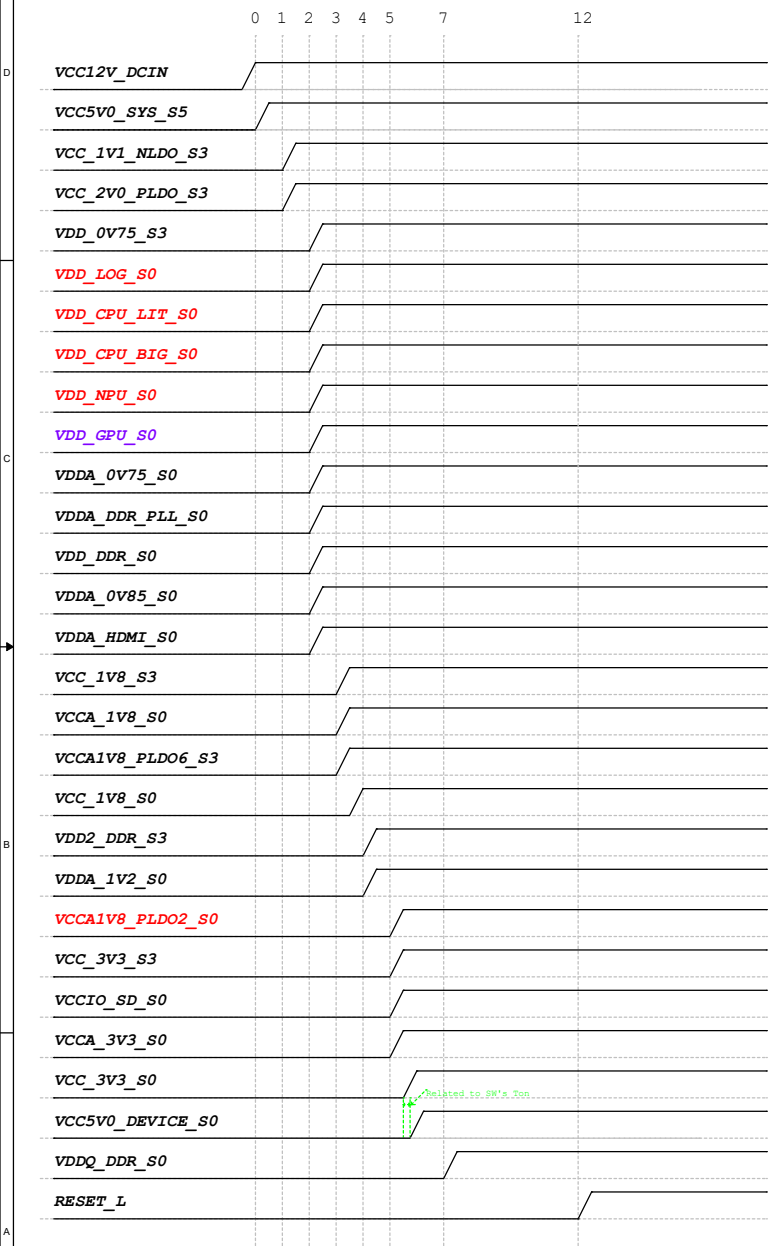
Power Tree



Note:
The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic. If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Note:
Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC5V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK3	5A	VDD_CPU_LIT_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:7	ADJ FB=0.5V	ON	0.61V-LP4/4x 0.51V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK7	3A	VDD_LOGIC_S0 VDD_LOGIC_MEM_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x 1.05V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_PLDO2_S0	Slot:5	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO4	0.5A	VCCA_3V3_S0	Slot:5	3.0V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA0V75_HDMI_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETh								
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_2V0_PLDO_S3	Slot:1	2.1V	ON	2.0V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	5A	VCC5V0_SYS_S5	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_DEVICE_S0	Slot:5A	5.2V	ON	5.2V	TBD	TBD
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	TBD	TBD
VCC_1V8_S3	SWITCH	2A	VCC_1V8_S0	Slot:3A	1.8V	ON	1.8V	TBD	TBD

Note:

The power suffix S0, S3 or S5 means:
S5: Keep power on during power down
S3: Keep power on during sleeping
S0: Power off during sleeping

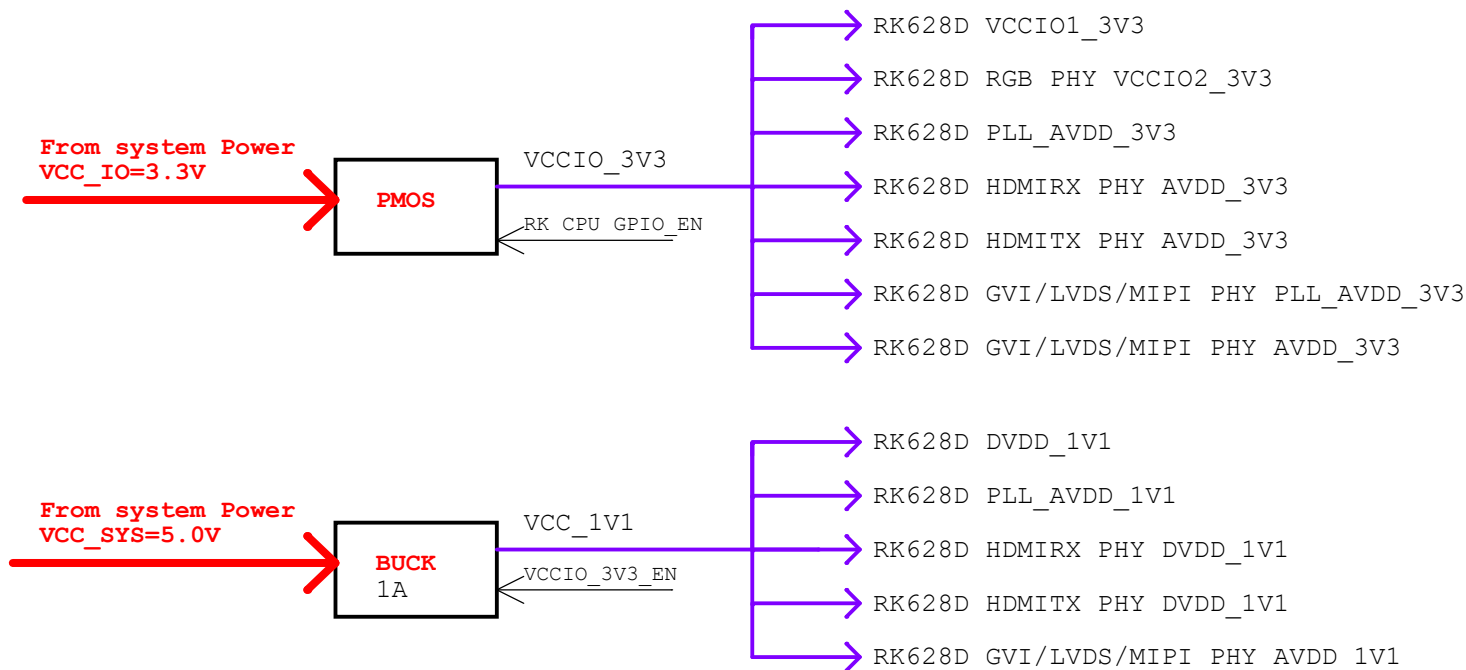
Note:

Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

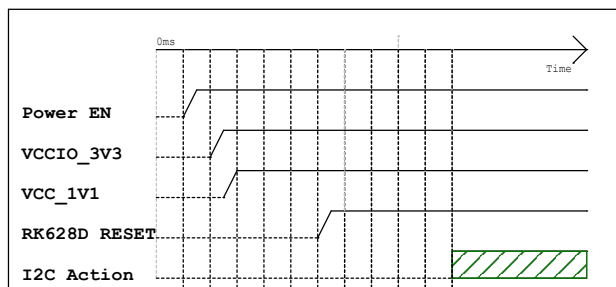
IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO0	Pin 2K11	1.8V Only	PMUIO0_VCC1V8	VCC_1V8	1.8V
PMUIO1	Pin 1U20	1.8V or 3.3V	PMUIO1_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO0	Pin 1J20	1.8V Only	VCCIO0_VCC1V8	VCC_1V8	1.8V
VCCIO1	Pin 2A8	1.8V or 3.3V	VCCIO1_VCC	VCC_1V8 VCC_3V3	1.8V/3.3V
VCCIO2	Pin 2A2	1.8V or 3.3V	VCCIO2_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO3	Pin 2B10	1.8V or 3.3V	VCCIO3_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO4	Pin 2A7	1.8V or 3.3V	VCCIO4_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO5	Pin 2A4/2A5	1.8V or 3.3V	VCCIO5_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO6	Pin 2N3	1.8V or 3.3V	VCCIO6_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO7	Pin 2M3	1.2V or 1.8V	VCCIO7_VCC	VCC_1V2 VCC_1V8	1.2V

IO Type	Operating Voltage
1.8V Only	VCCIO*_VCC1V8=1.8V
1.2V or 1.8V	VCCIO*_VCC=1.2V or 1.8V
1.8V or 3.3V	VCCIO*_VCC=1.8V or 3.3V

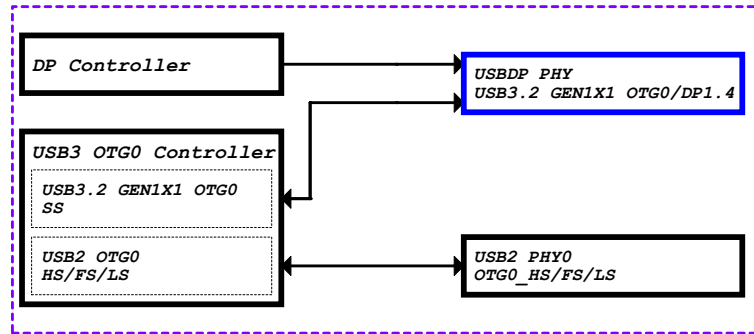


Power-on Sequence:

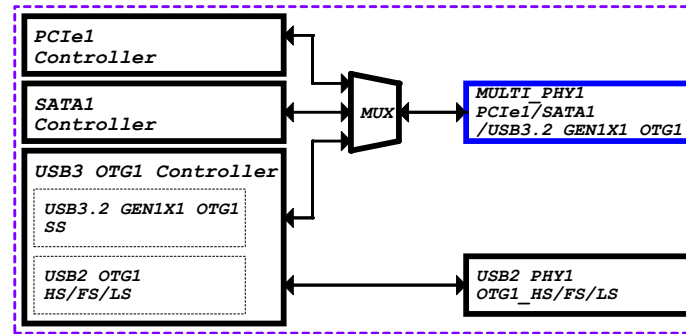


MULTI_PHY Path Map

USB DP PHY--USB3.2 GEN1X1 OTG0/DP1.4



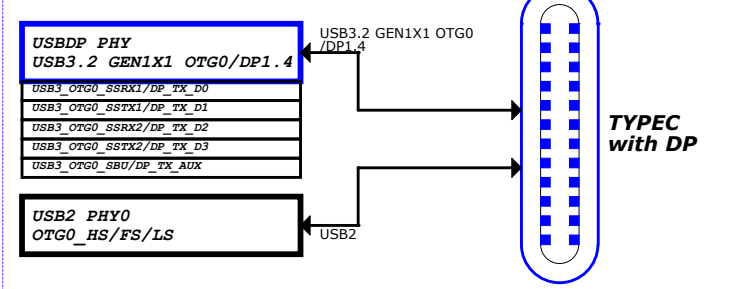
PCIe Combo PHY1-- PCIe1/SATA1/USB3.2 GEN1X1 OTG1



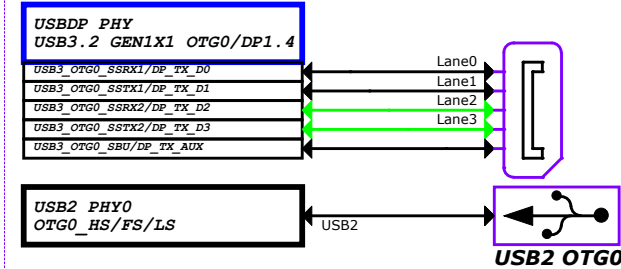
Note:
USB2 OTG1 can only be used when
PCIe1/SATA1 is not in use!!!

USB OTG0/DP Application

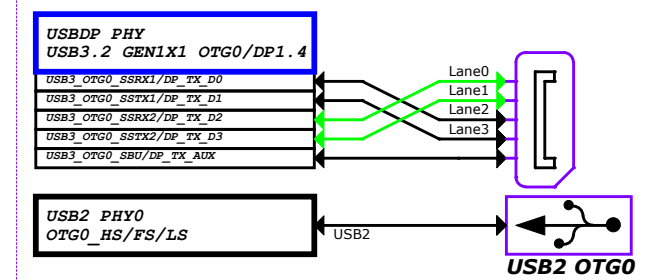
CASE0: TYPEC with DP



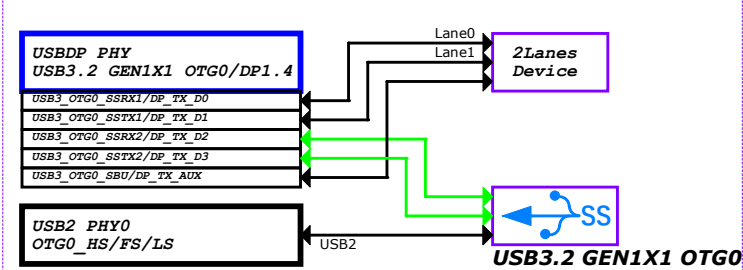
CASE1: USB2 OTG0 + DP 4Lane (Swap OFF)



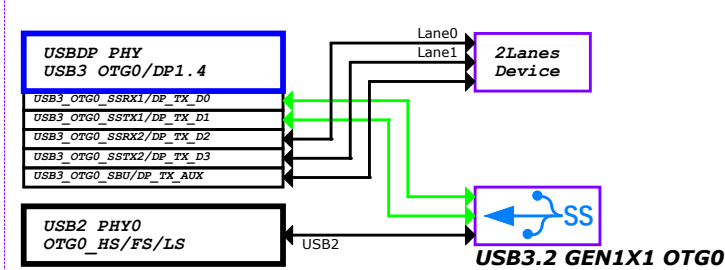
CASE2: USB2 OTG0 + DP 4Lane (Swap ON)



CASE3: USB3.2 GEN1X1 OTG0 + DP 2Lane (Swap OFF)



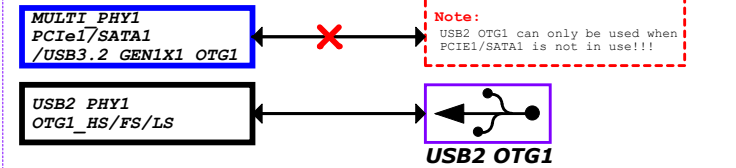
CASE4: USB3.2 GEN1X1 OTG0 + DP 2Lane (Swap ON)



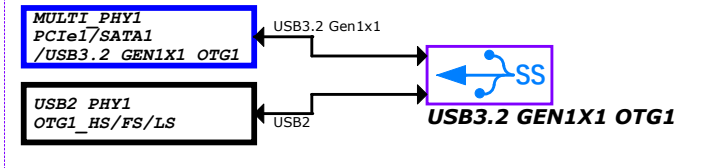
Note:
DP Lane swap enable
0: Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
1: Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

USB OTG1 Application

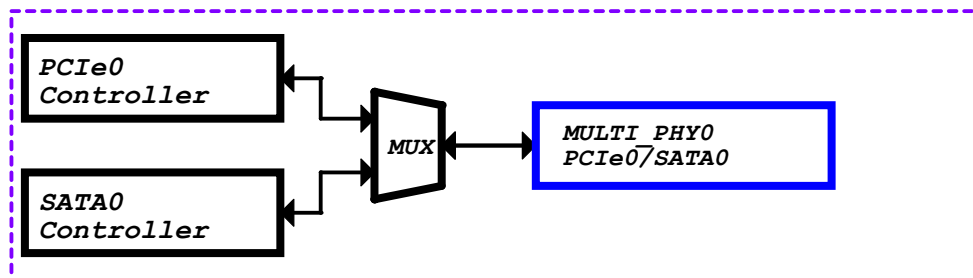
CASE0: USB2 OTG1



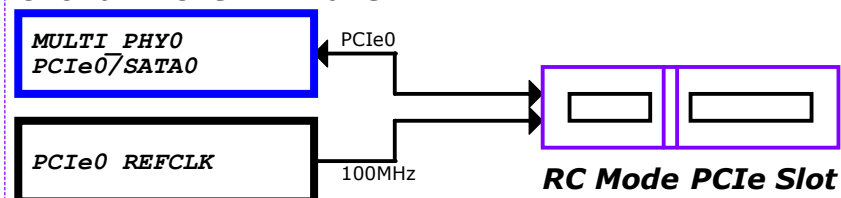
CASE1: USB3.2 GEN1X1 OTG1



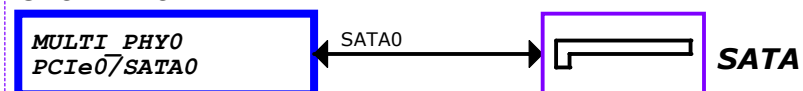
PCIE Combo PHY0--PCIE0/SATA0



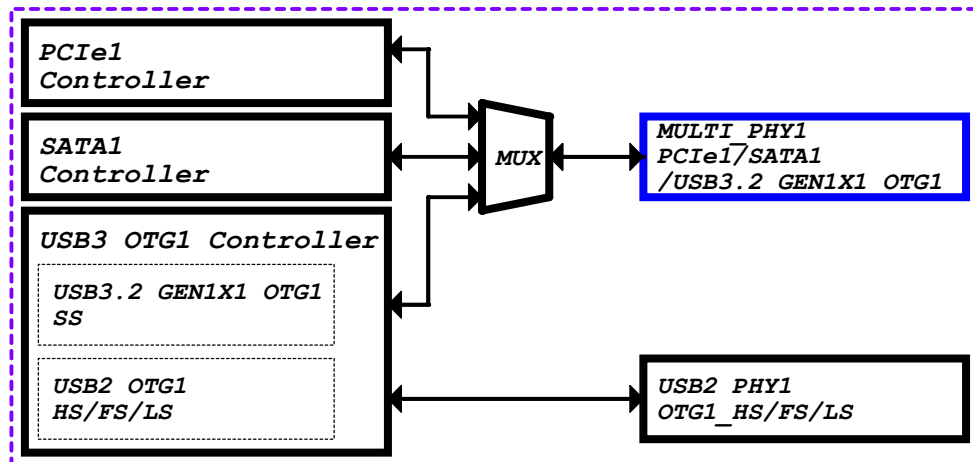
CASE0: PCIE x 1Lane



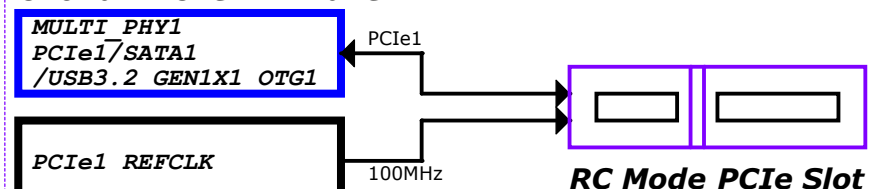
CASE1: SATA



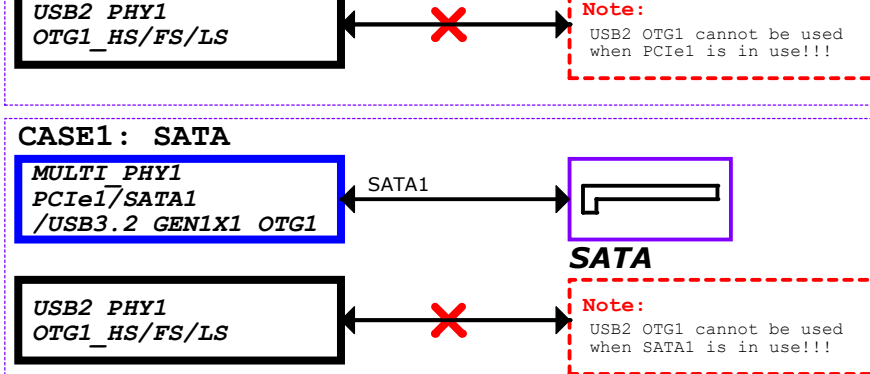
PCIE Combo PHY1--PCIE1/SATA1/USB3.2 GEN1X1 OTG1



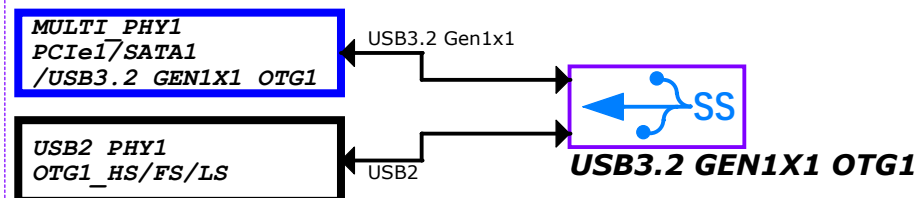
CASE0: PCIE x 1Lane



CASE1: SATA

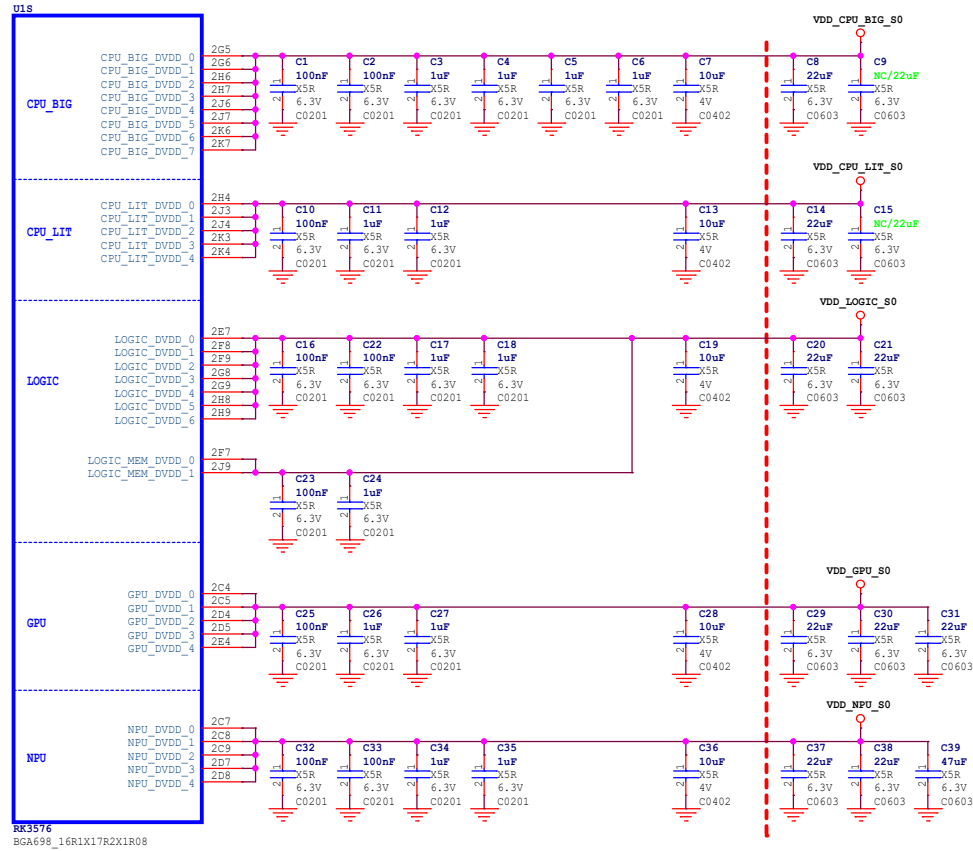


CASE2: USB3.2 GEN1X1 OTG1



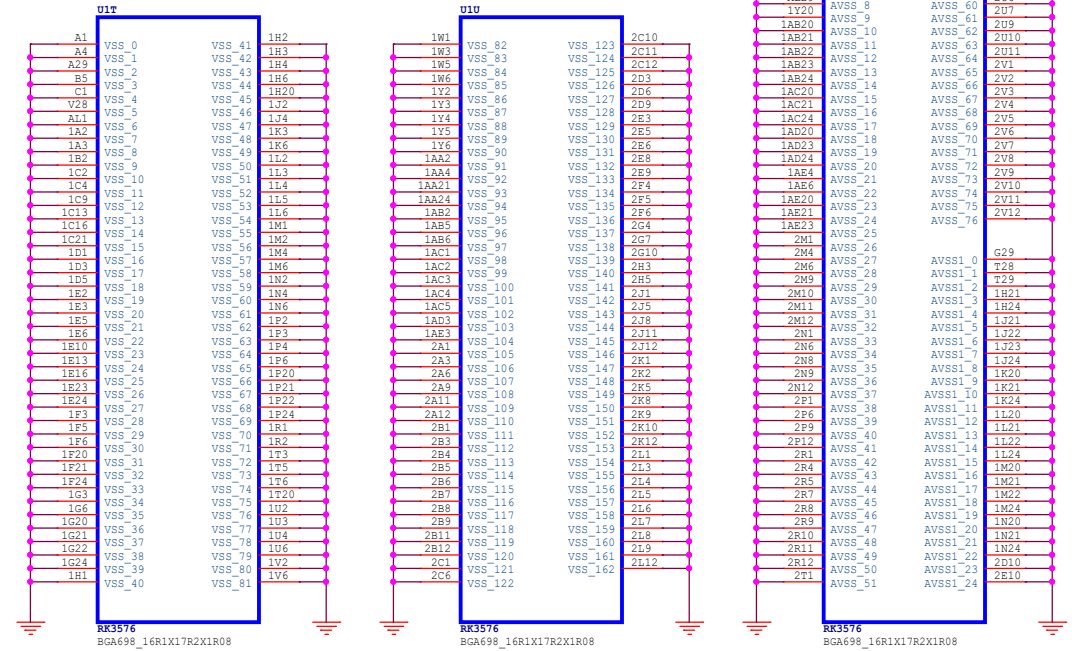
RK3576_S (Power)

RK3576_T/U/V (GND)

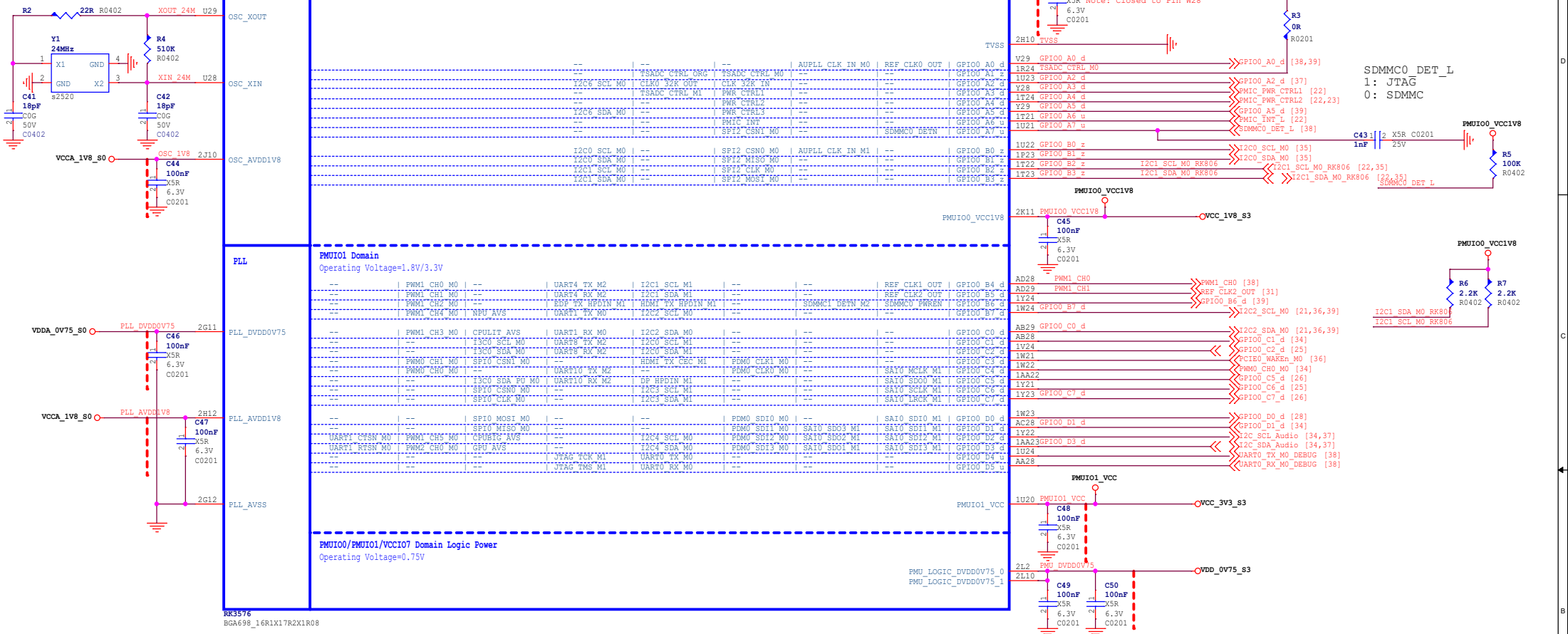


Note:

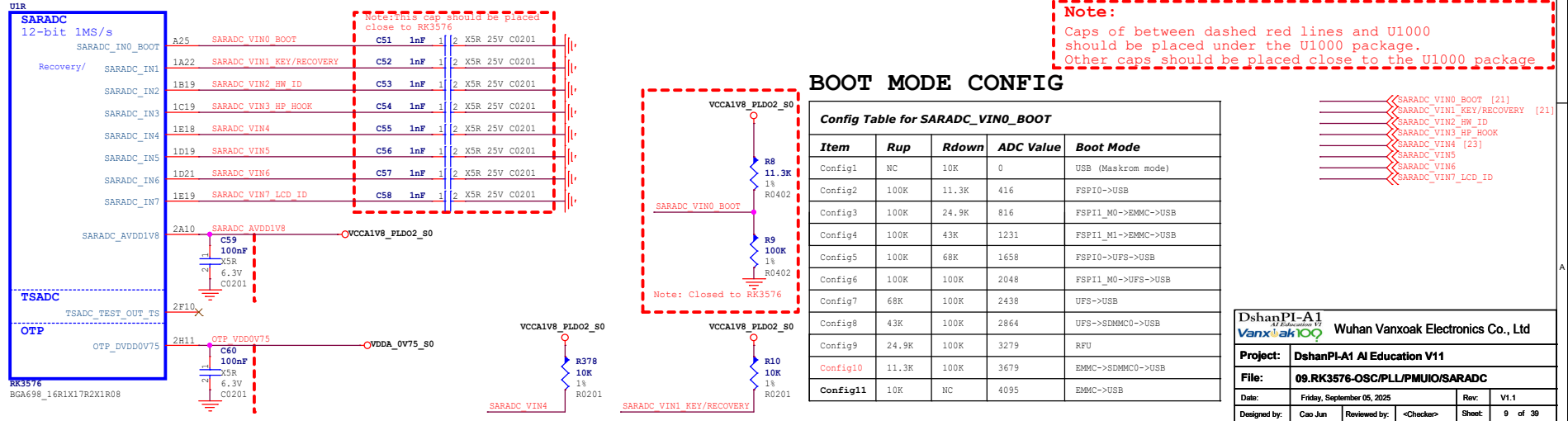
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



RK3576 E
(PMUIO0/1)



RK3576 R
(SARADC)



D



4

Resistors in the red line dotted box
should be placed under the U1000 package

1



[illegible]

VCCIO0 Domain												
Operating Voltage=1.8V												
--	--	I2C2_SCL M1	UART7_RTSN M1	--	--	--	SAIO_SCLK M2	FSPIO_D0	EMMC_D0	GPIO1_A0 W	E28	FSPIO_D0/EMMC_D0
--	--	I2C2_SDA M1	UART7_CTSN M1	--	--	--	SAIO_LACK M2	FSPIO_D1	EMMC_D1	GPIO1_A1 W	E29	FSPIO_D1/EMMC_D1
--	--	UART6_RTSN M2	UART6_RX M1	P0M0_SDA1 M1	SAIO_SDA1 M2	SAIO_SDA1 M2	SAIO_SDA1 M2	FSPIO_D2	EMMC_D2	GPIO1_A2 W	I024	FSPIO_D2/EMMC_D2
--	--	UART6_CSN M2	UART6_TX M1	P0M0_SCK1 M1	SAIO_SCK1 M2	SAIO_SCK1 M2	SAIO_SCK1 M2	FSPIO_D3	EMMC_D3	GPIO1_A3 W	F28	FSPIO_D3/EMMC_D3
--	--	--	--	--	SAIO_MCLK M2	SAIO_MCLK M2	SAIO_MCLK M2	--	EMMC_D4	GPIO1_A4 W	I024	FSPIO_D4/EMMC_D4
--	--	I2C9_SCL M0	SP10_MOSI M2	P0M0_SDA2 M1	SAIO_SDA2 M2	SAIO_SDA2 M2	--	--	EMMC_D5	GPIO1_A5 W	G28	FSPIO_D5/EMMC_D5
--	--	I2C9_SDA M0	SP10_MISO M2	P0M0_CLK1 M1	SAIO_LACK M0	SAIO_SDA1 M2	--	--	EMMC_D6	GPIO1_A6 W	D28	FSPIO_D6/EMMC_D6
--	--	--	--	--	--	SAIO_SCK1 M2	SAIO_SCK1 M2	--	EMMC_D7	GPIO1_A7 W	I824	FSPIO_D7/EMMC_D7
--	--	I2C7_SCL M0	UART6_TX M2	--	--	--	FSPIO_CSN1	FSPIO_RSTN	EMMC_CMD	GPIO1_B0 W	1F22	FSPIO_RSTN/EMMC_CMD
PMW2_CH0 M1	--	--	--	P0M0_CLK0 M1	SAIO_SDA1 M2	SAIO_SDA1 M2	FSPIO_CLK	EMMC_CLK	GPIO1_B1 W	OR	I023	FSPIO_CLK/EMMC_CLK
PMW2_CH1 M0	MIPI_TE M3	I2C7_SDA M0	UART6_RX M2	--	--	SAIO_SDA1 M2	SAIO_SDA1 M2	EMMC_STB#	GPIO1_B2 W	OR	E23	FSPIO_Q05/EMMC_STB#
--	--	--	--	--	--	--	FSPIO_CSN0	EMMC_RSTN	GPIO1_B3 W	--	I023	FSPIO_CSN0/EMMC_RSTN

VCCIO1 Domain															
Operating Voltage=1.8V/3.3V															
PWM2_CH2_M0	CAN0_RX_M0	SP10_MOSI_M1	I2C8_SCL_M0	UART7_RX_M2	UART0_RX_M1	--	--	DSM_AUD_LP_M0	FSP11_D0_M0	SDMMC0_D0	GPIO2_A0_0	B24	SDMMC0_D0/CAN0_RX_M0	>>>SDMMC0_D0 [38]	
PWM2_CH3_M0	CAN0_RX_M0	SP10_MISO_M1	I2C8_SDA_M0	UART7_TX_M2	UART0_TX_M1	--	SAT3_MCLK_M3	DSM_AUD_LN_M0	FSP11_D1_M0	SDMMC0_D1	GPIO2_A1_0	B25	SDMMC0_D1/CAN0_TX_M0	>>>SDMMC0_D1 [38]	
I3C1_SCL_M1	CAN1_RX_M0	SP10_CSNI_M1	--	UART5_RTSN_M2	JTAG_TCK_M0	--	SAT3_LRCK_M3	DSM_AUD_RP_M0	FSP11_D2_M0	SDMMC0_D2	GPIO2_A2_0	A23	SDMMC0_D2/JTAG_TCK_M0	>>>SDMMC0_D2 [38]	
I3C1_SDA_M1	CAN1_TX_M0	--	--	UART5_CTSN_M2	JTAG_TMS_M0	--	SAT3_SDI_M3	DSM_AUD_RN_M0	FSP11_D3_M0	SDMMC0_D3	GPIO2_A3_0	B23	SDMMC0_D3/JTAG_TMS_M0	>>>SDMMC0_D3 [38]	
SP10_CSNI_M1	SP10_SDA_M1	SP10_SCK_M1	SP10_CLK_M1	UART5_TX_M2	UART5_RX_M2	TEST_CLK_00V	SAT3_SCK_M3	--	FSP11_CLK_M0	SDMMC0_CLK	GPIO2_A5_0	IA21	SDMMC0_CMD/SDMMC0_CMD	>>>SDMMC0_CMD [38]	
I3C1_SDA_PU_M1	--	SP10_CLK_M1	I2C8_SCL_M0	--	UART5_TX_M2	TEST_CLK_00V	SAT3_SCK_M3	--	FSP11_CLK_M0	SDMMC0_CLK	GPIO2_A5_0	IB21	SDMMC0_CLK	>>>SDMMC0_CLK [38]	

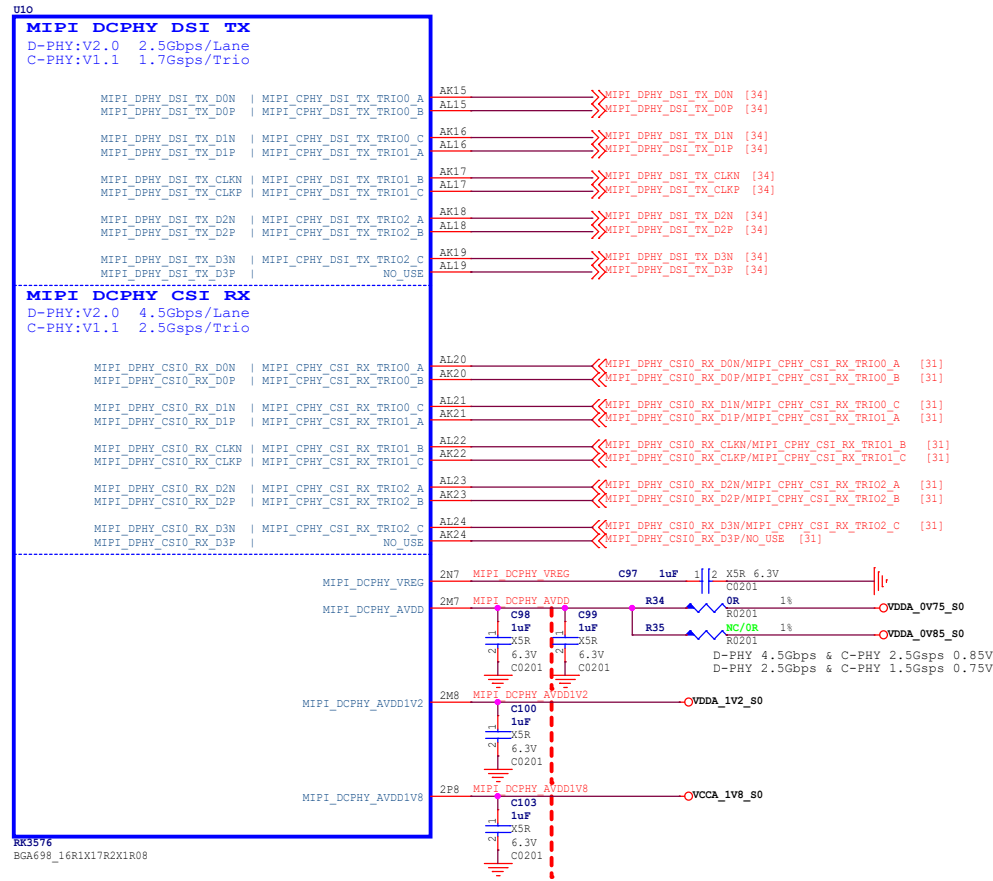
RK3576
 BGA698_16RX17RX18R08

VCCIO1_VCC 2A8 VCCIO1 VCCIO_SD_S0 C83 100nF X5R 6.3V C0201

SDMMC0支持system boot

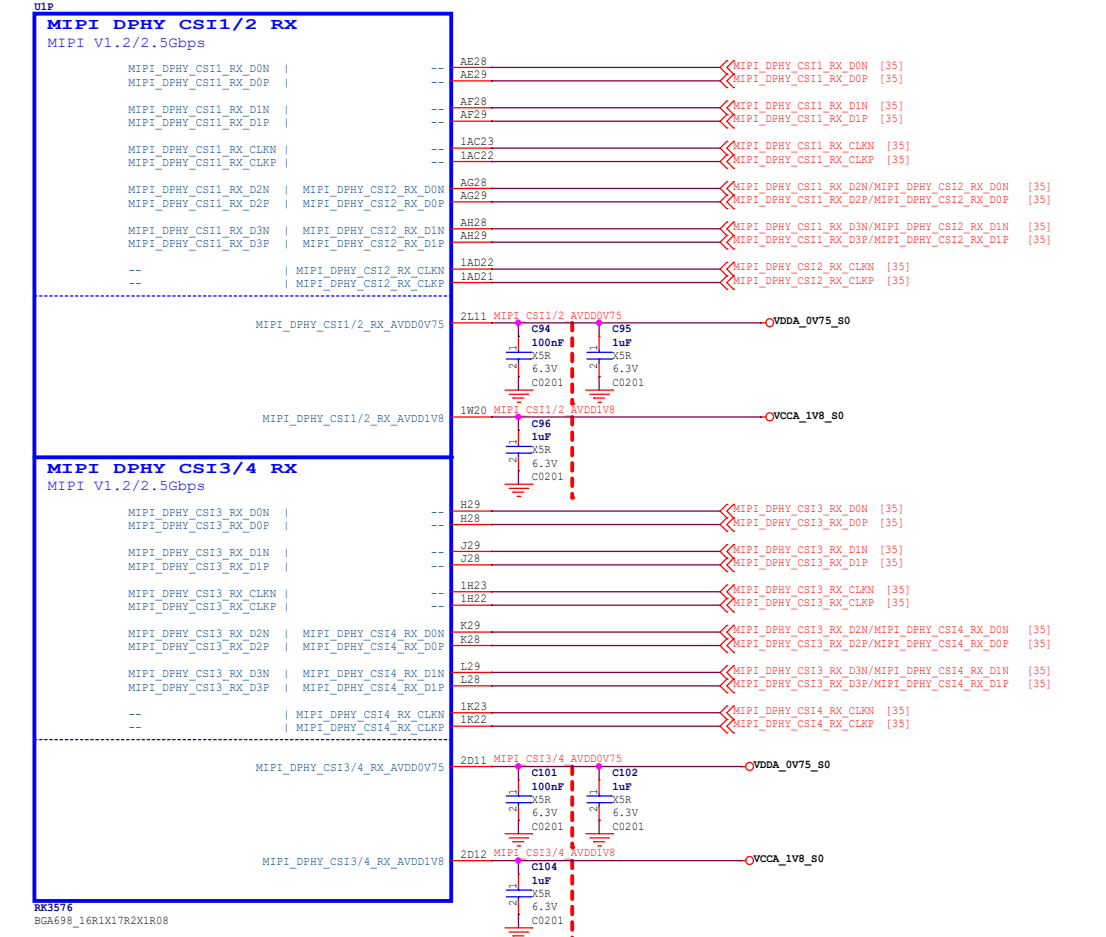
 Wuhan Vanxoak Electronics Co., Ltd			
Project:		DshanPI-A1 AI Education V11	
File:		11.RK3576-eMMC/UFS/SD	
Date:	Friday, September 05, 2025	Rev.	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker> Sheet 11 of 39

RK3576_O (MIPI DCPHY)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

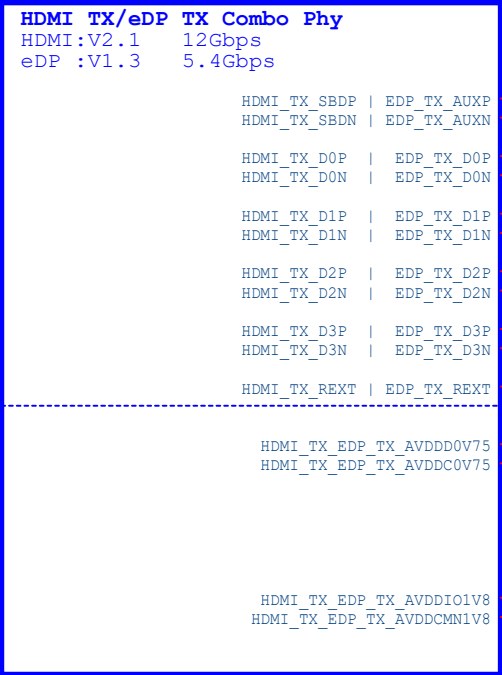
RK3576_P (MIPI DPHY CSI RX)



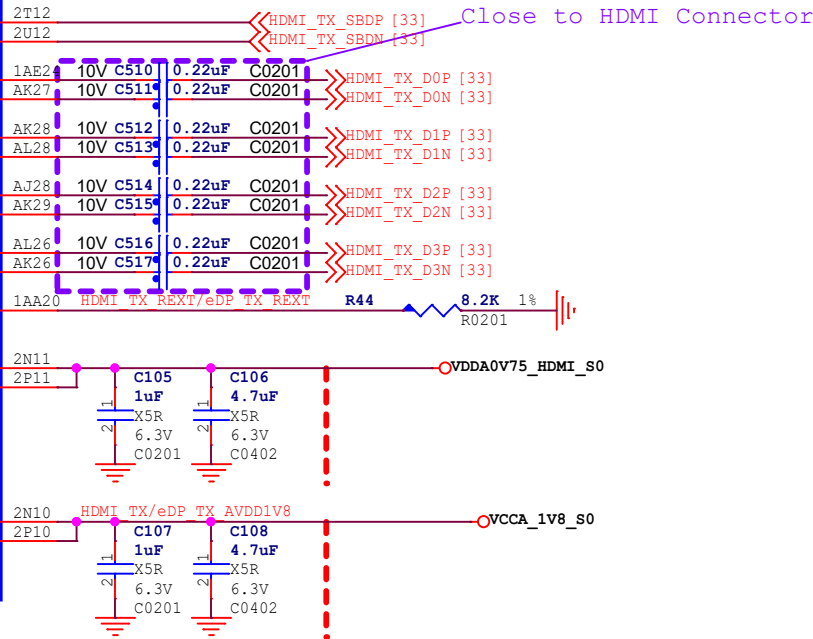
Note:
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Other caps should be placed close to the U1000 package

RK3576_Q (HDMI/eDP)

Note:
HDMI 2.1 supports up to 4Kx2K@120Hz
u10

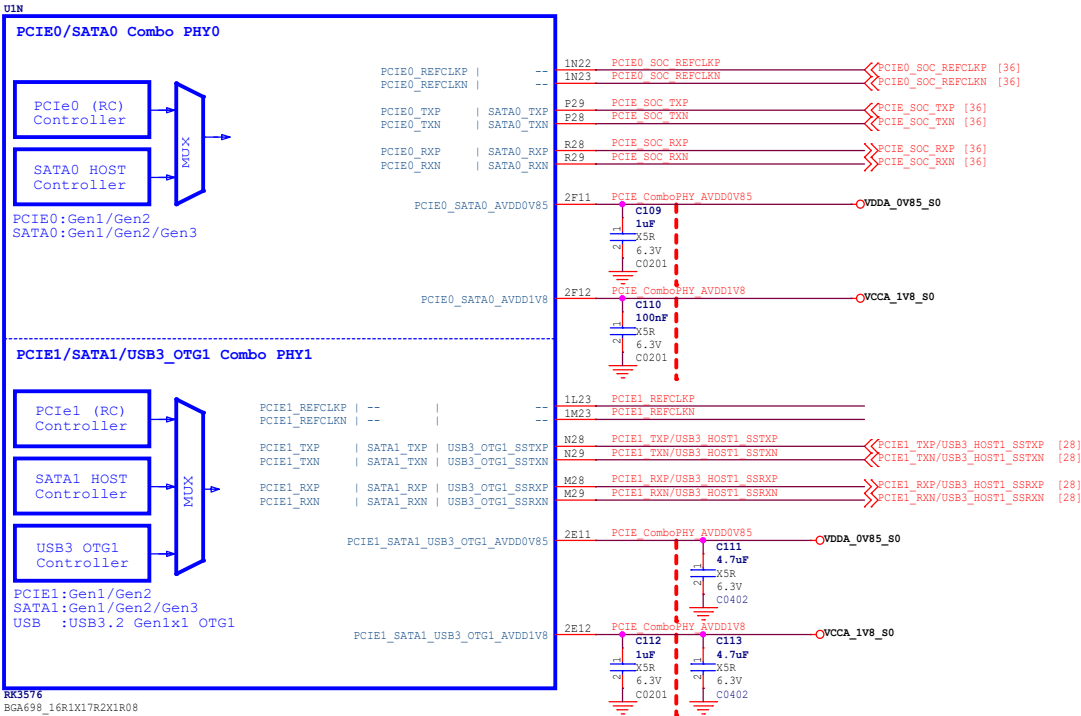


RK3576
BGA698_16R1X17R2X1R08



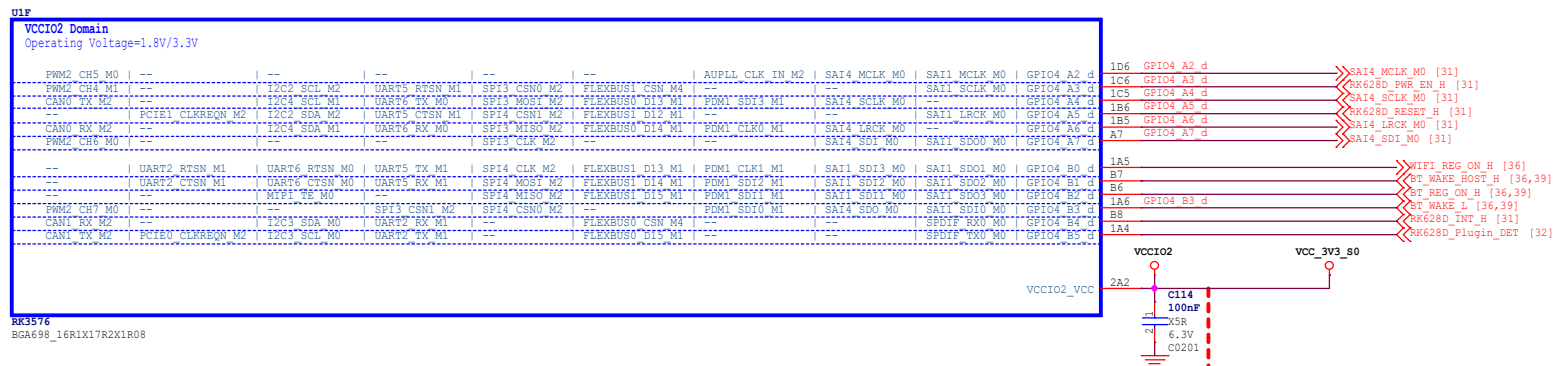
Note:
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RK3576_N (PCIe/SATA/USB3)

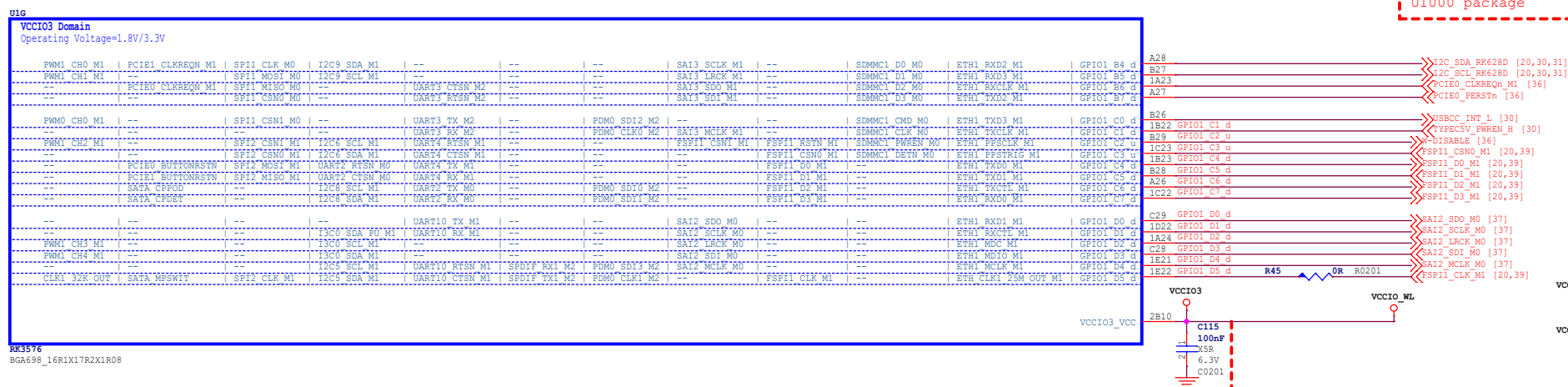


Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3576 F (VCCIO2)

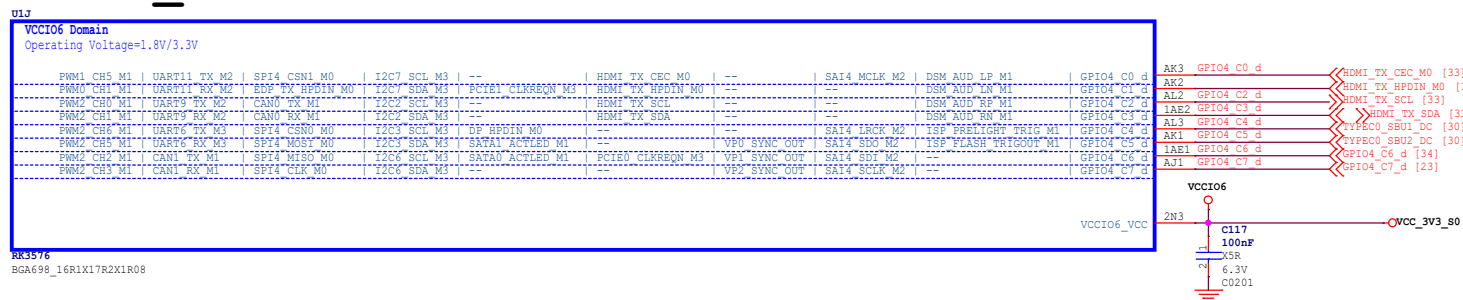


RK3576 G (VCCIO3)



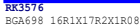
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3576 J (VCCIO6)



U1H

VCCIO4 Domain
Operating Voltage=1.8V/3.3V



U11

VCCI05 Domain
Operating Voltage=1.8V/3.3V



OR	R0201	»	GPIO3_A4_D	[35]
OR	R0201	»	CMAC_MIO0_M0	[25]
		»	CMAC_MDC_M0	[25]
		»	CMAC_RXCTL_M0	[25]
		»	CMAC_RXLNOUT_M0	
		»	CMAC_RXDI_M0	[25]
OR	R0201	»	CMAC_RXDO_M0	[25]
		»	CMAC_TXCTL_M0	[25]
OR	R0201	»	CMAC_TXDI_M0	[25]
OR	R0201	»	CMAC_TXDO_M0	[25]
OR	R0201	»	CMAC_TXCLK_M0	[25]
		»	JART2_RX_M2	[35]
		»	JART2_TX_M2	[35]
OR	R0201	»	LACS_SDA_M3	[39]
OR	R0201	»	CMAC_TXD2_M0	[25]
		»	CMAC_TXD2_M0	[25]
		»	LACS_SCL_M3	[39]
		»	GPIO3_C5_D	[35]
		»	GPIO3_C6_D	[35]
		»	GPIO3_C7_D	[35]
		»	GPIO3_D0_D	[39]
		»	CMAC_RXCLK_M0	[25]
		»	CMAC_RXD3_M0	[25]
		»	CMAC_RXD2_M0	[25]
		»	LACS_SCL_M2	[35]
		»	LACS_SDA_M2	[35]
		»	JART5_CTS_M0	[35]
		»	JART5_CTS_M0	[35]
		»	CAM_CLKO_D0	[35]

eMMC FLASH

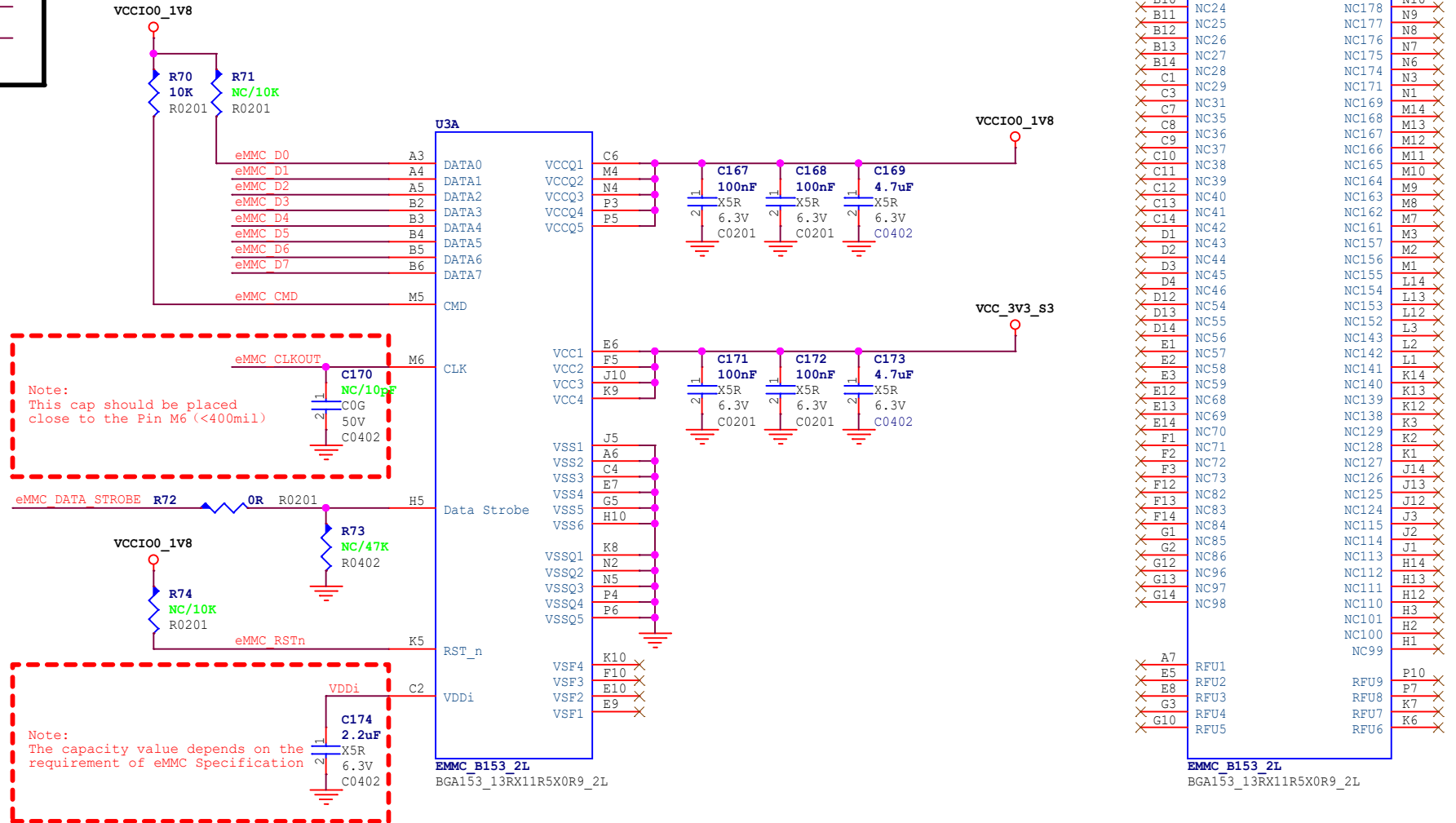
[11] eMMC_D0<<>>
[11] eMMC_D1<<>>
[11] eMMC_D2<<>>
[11] eMMC_D3<<>>
[11] eMMC_D4<<>>
[11] eMMC_D5<<>>
[11] eMMC_D6<<>>
[11] eMMC_D7<<>>

[11] eMMC_CMD<<>>

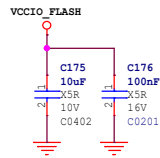
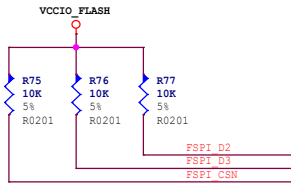
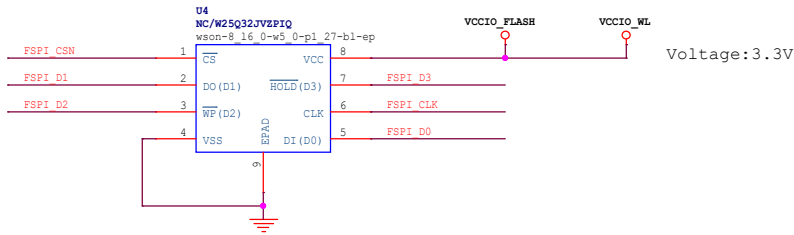
[11] eMMC_CLKOUT<<>>

[11] eMMC_DATA_STROBE<<>>

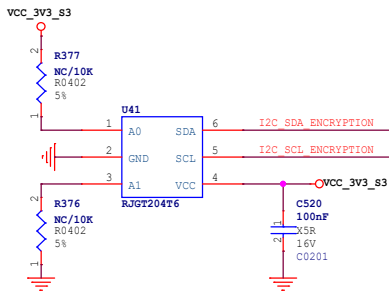
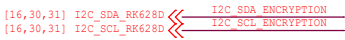
[11] eMMC_RSTn<<>>



SPI Flash



Encryption

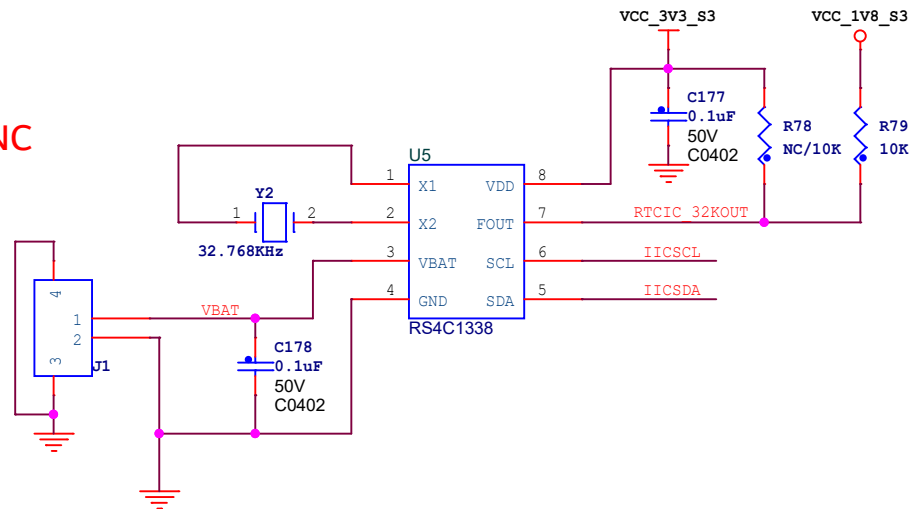


A0	A1	Adress
1	0	0x69
NC	NC	0x68

DshanPI-A1 AI Education V1 VanxoakIQ		Wuhan Vanxoak Electronics Co., Ltd	
Project:	DshanPI-A1 AI Education V11		
File:	20.Flash-SPI Flash/Encryption		
Date:	Friday, September 05, 2025	Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>
		Sheet:	20 of 39

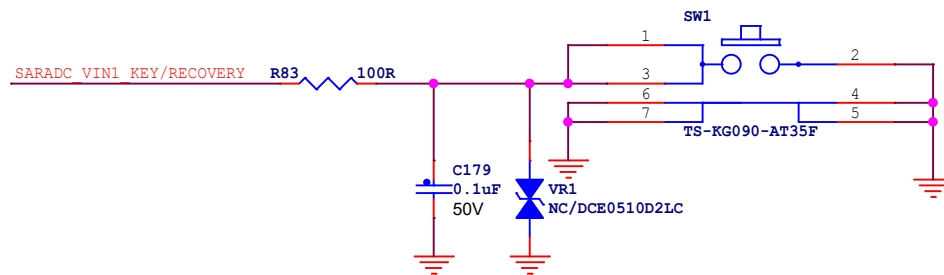
说明:
1) I2C1电平为3.3v
2) 如果I2C多处上拉, R29=R30=NC

[9,36,39] I2C2_SCL_M0<< IIC_SCL
[9,36,39] I2C2_SDA_M0<< IIC_SDA
[36] RTC_32KOUT << R82 22R RTCIC 32KOUT

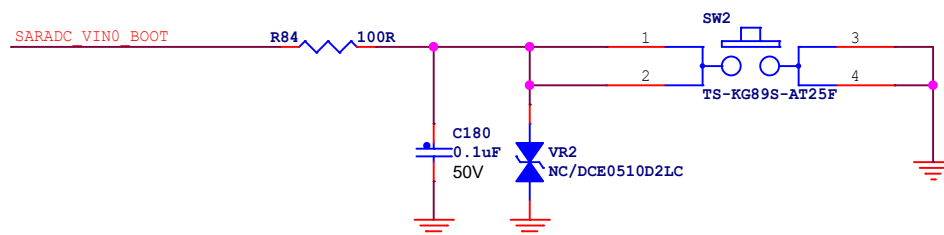


[9] SARADC_VIN1_KEY/RECOVERY<<
[9] SARADC_VIN0_BOOT<<

RECOVERY

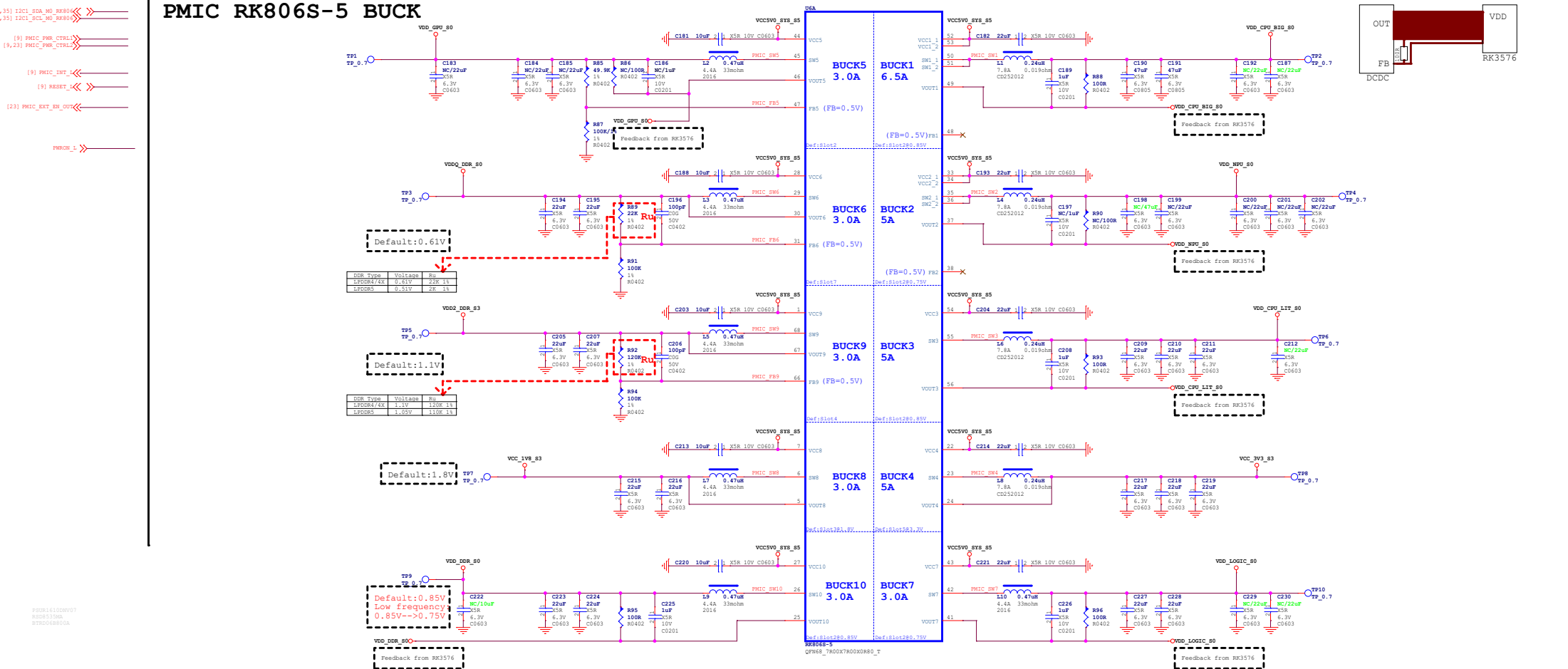


MASKROM



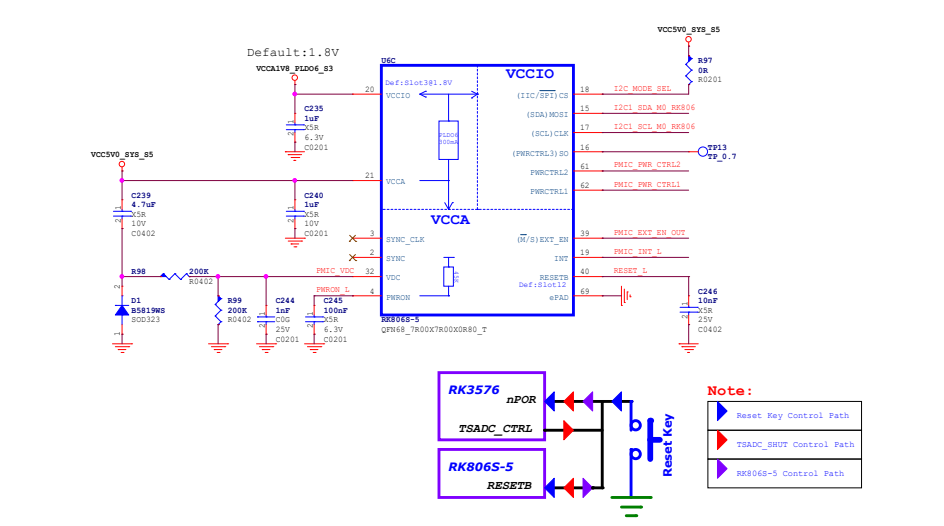
DshanPI-A1 AI Education V1 Vanxoak100		Wuhan Vanxoak Electronics Co., Ltd	
Project:	DshanPI-A1 AI Education V11		
File:	21.RTC/MASKROM/RECOVERY		
Date:	Friday, September 05, 2025	Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>
		Sheet:	21 of 39

PMIC RK806S-5 BUCK

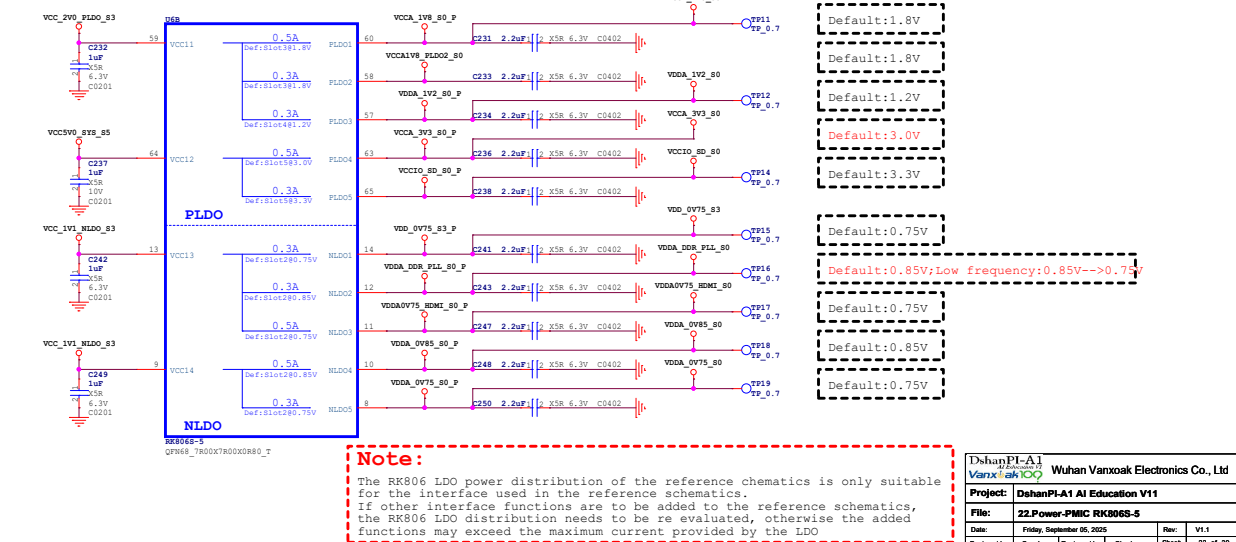


PMIC RK806S-5 Managerment

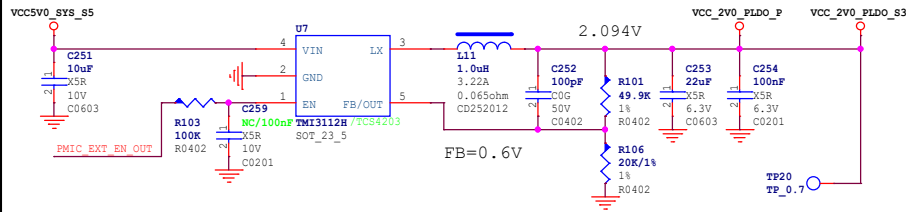
Note:
I2C Mode:CS(pin18) connected to VCCA(pin21);
SPI Mode(Def):CS(pin18) floating or connected to GND;



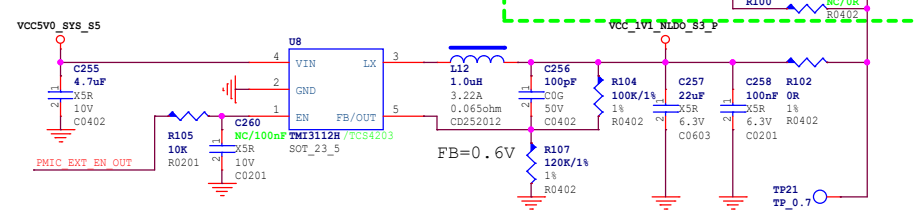
PMIC RK806S-5 LDO



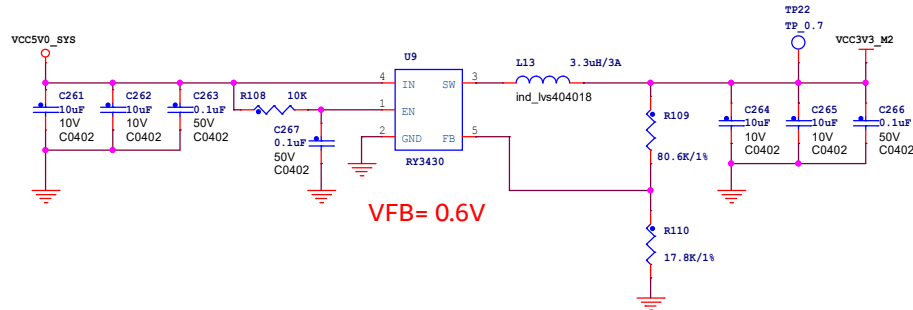
VCC_2V0_PLDO_S3



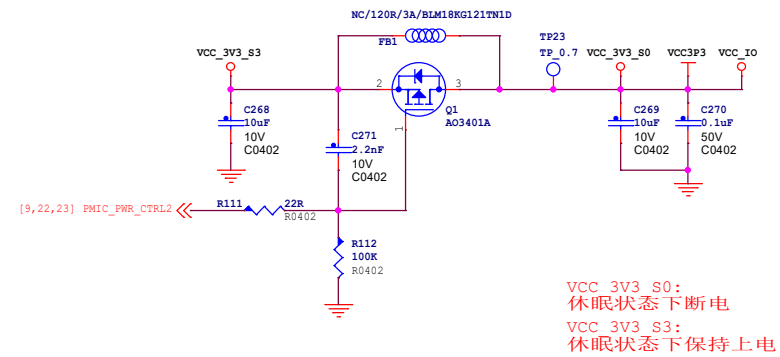
VCC_1V1_NLDO_S3



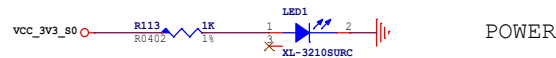
VCC3V3_M2



VCC_3V3_S0

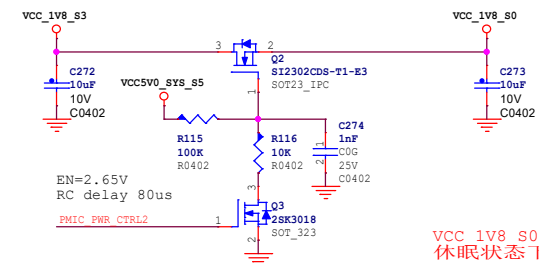


LED

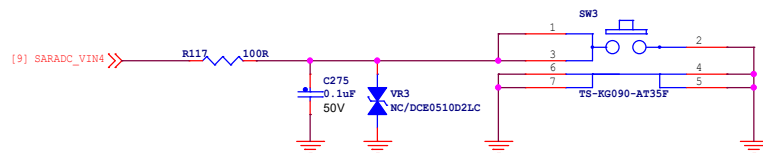


POWER

VCC_1V8_S0



USER KEY




```

[17] GMAC0_TXCTL_M0 << >>
[17] GMAC0_TXCLK_M0 << >>
[17] GMAC0_TXD0_M0 << >>
[17] GMAC0_TXD1_M0 << >>
[17] GMAC0_TXD2_M0 << >>
[17] GMAC0_TXD3_M0 << >>

[17] GMAC0_RXCTL_M0 << >>
[17] GMAC0_RXCLK_M0 << >>
[17] GMAC0_RXD0_M0 << >>
[17] GMAC0_RXD1_M0 << >>
[17] GMAC0_RXD2_M0 << >>
[17] GMAC0_RXD3_M0 << >>

[17] GMAC0_MDIO_M0 << >>

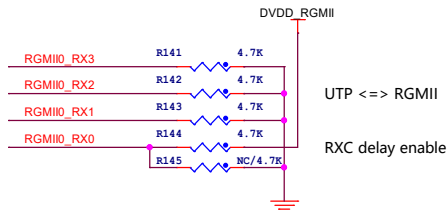
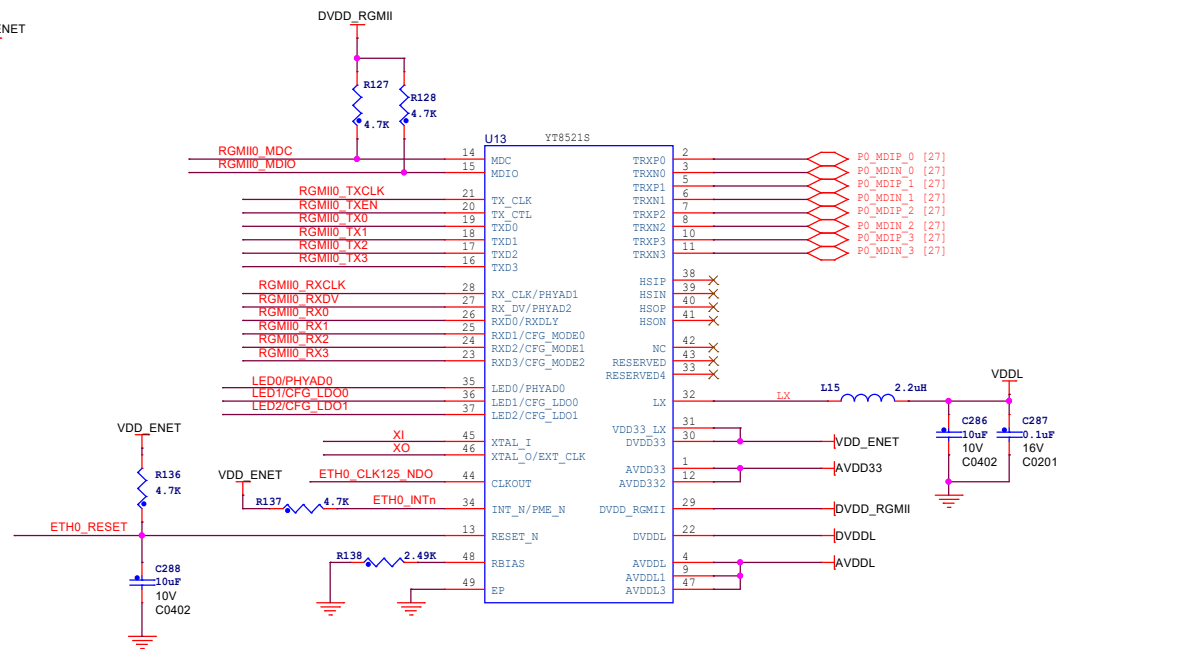
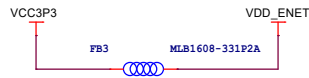
[17] GMAC0_MDC_M0 << >>

[17] GMAC0_MCLINKINOUT_M0 << >>

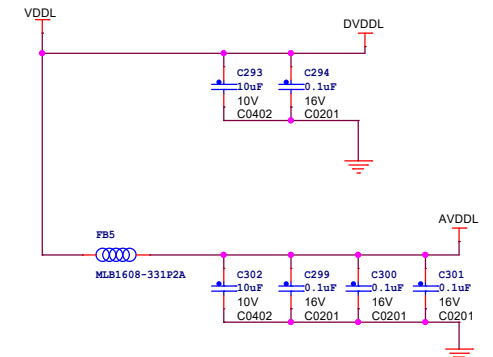
[9] GPIO0_C2_d << >>

[9] GPIO0_C6_d << >>

```



The schematic diagram illustrates the VDD_ENET power plane. The supply rail, labeled VDD_ENET, is connected to a network of decoupling capacitors. The capacitors are arranged in two rows. The top row consists of C290 (10uF, 10V, C0402), C291 (0.1uF, 16V, C0201), and C292 (0.1uF, 16V, C0201). The bottom row consists of C296 (10uF, 10V, C0402), C297 (0.1uF, 16V, C0201), and C298 (0.1uF, 16V, C0201). Additionally, there are two ferrite beads, FB4 and FB6, connected to the supply rail. FB4 is connected to the MLBI608-331P2A component, and FB6 is connected to the NC/MLBI608-331P2A component. The capacitors C303 (10uF, 10V, C0402) and C304 (0.1uF, 16V, C0201) are connected to the supply rail and ground. The ground connection is shown as a common ground plane.



		Wuhan Vanxoak Electronics Co., Ltd	
Project: DshanPI-A1 AI Education V11			
File: 25.Ethernet RGM10			
Date: Friday, September 05, 2025		Rev: V1.1	
Designed by: Cao Jun	Reviewed by: <Checker>	Sheet: 25	of 39

RGMI I1

[17] GMAC1_TXCTL_M0 << RGMIH1_TXEN
 [17] GMAC1_TXCLK_M0 << RGMIH1_TXCLK
 [17] GMAC1_TXD0_M0 << RGMIH1_TX0
 [17] GMAC1_TXD1_M0 << RGMIH1_TX1
 [17] GMAC1_TXD2_M0 << RGMIH1_TX2
 [17] GMAC1_TXD3_M0 << RGMIH1_TX3

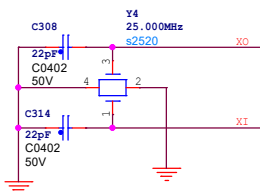
[17] GMAC1_RXCTL_M0 << R158 << 22R RGMIH1_RXDV
 [17] GMAC1_RXCLK_M0 << R159 << 22R RGMIH1_RXCLK
 [17] GMAC1_RXD0_M0 << R160 << 22R RGMIH1_RX0
 [17] GMAC1_RXD1_M0 << R161 << 22R RGMIH1_RX1
 [17] GMAC1_RXD2_M0 << R162 << 22R RGMIH1_RX2
 [17] GMAC1_RXD3_M0 << R163 << 22R RGMIH1_RX3

[17] GMAC1_MDIO_M0 << RGMIH1_MDIO
 [17] GMAC1_MDC_M0 << RGMIH1_MDC

[17] GMAC1_MCLKINOUT_M0 << R164 << 22R ETH1_CLK125_NDO

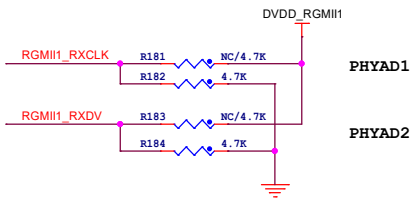
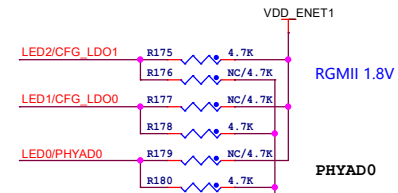
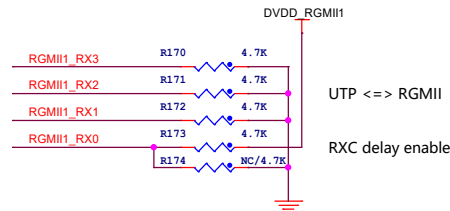
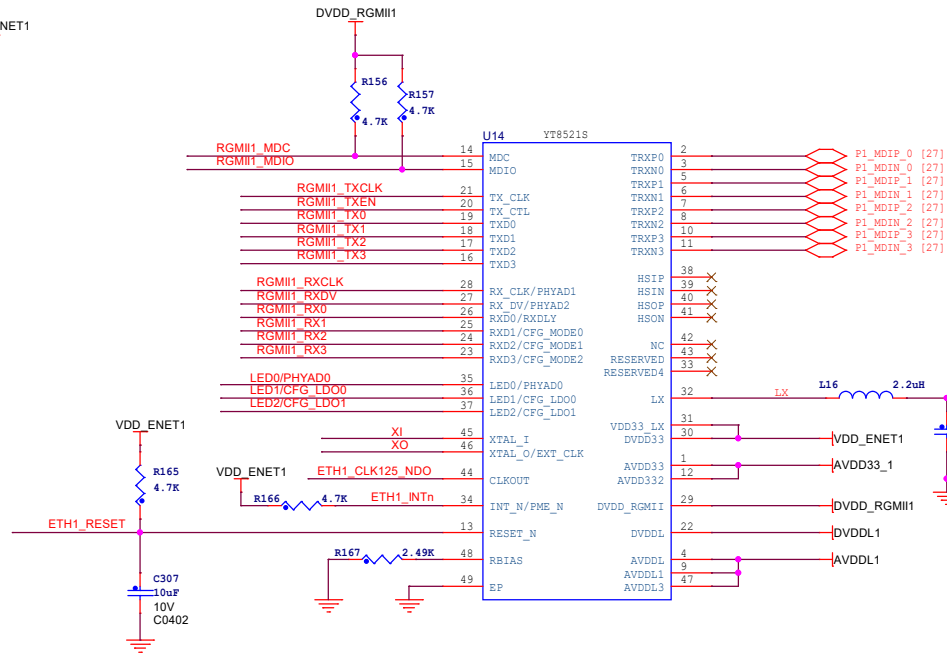
[9] GPIO0_C5_d << R168 << 100R ETH1_RESET

[9] GPIO0_C7_d << R169 << 22R ETH1_INTn

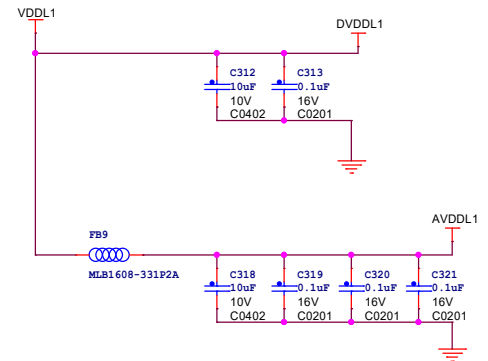
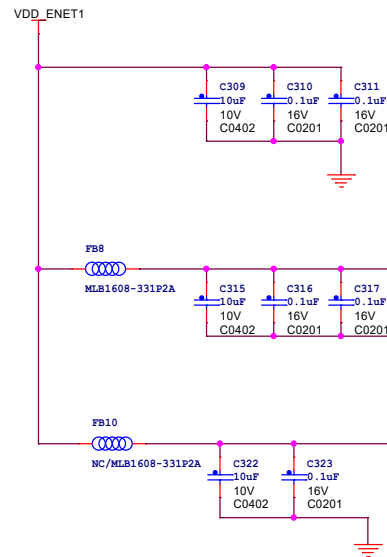


RXD[3:1]	Operation Mode
3'b000	UTP <=> RGMII
3'b001	FIBER <=> RGMII
3'b010	UTP/FIBER <=> RGMII
3'b011	UTP <=> SGMII
3'b100	SGMII (PHY) <=> RGMII
3'b101	SGMII (MAC) <=> RGMII
3'b110	UTP <=> FIBER (AUTO)
3'b111	UTP <=> FIBER (FORCE)

CFG_LDO[1:0]	RGMII Voltage Selection
2'b00	External 3.3V
2'b01	Internal 2.5V
2'b10	Internal 1.8V
2'b11	Not Available



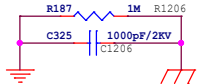
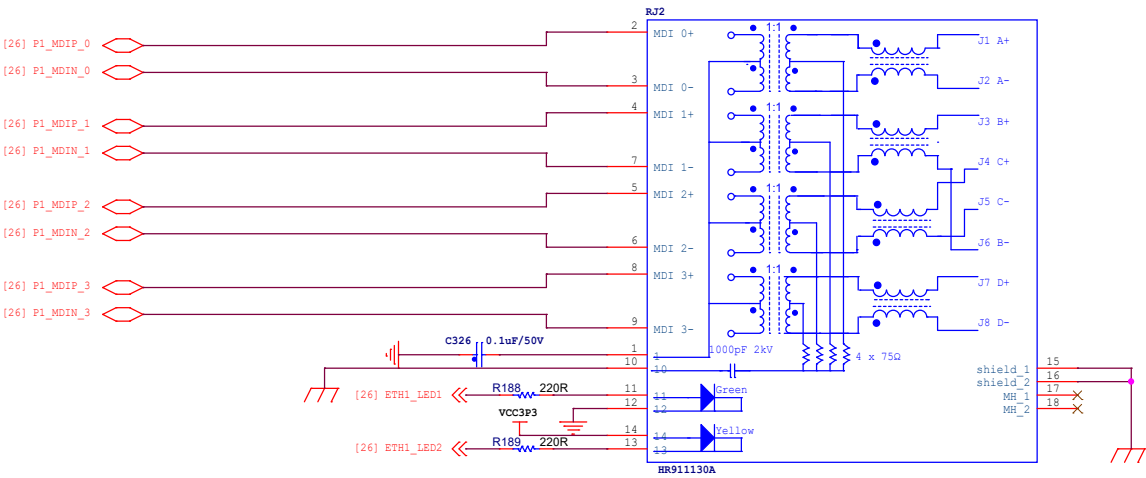
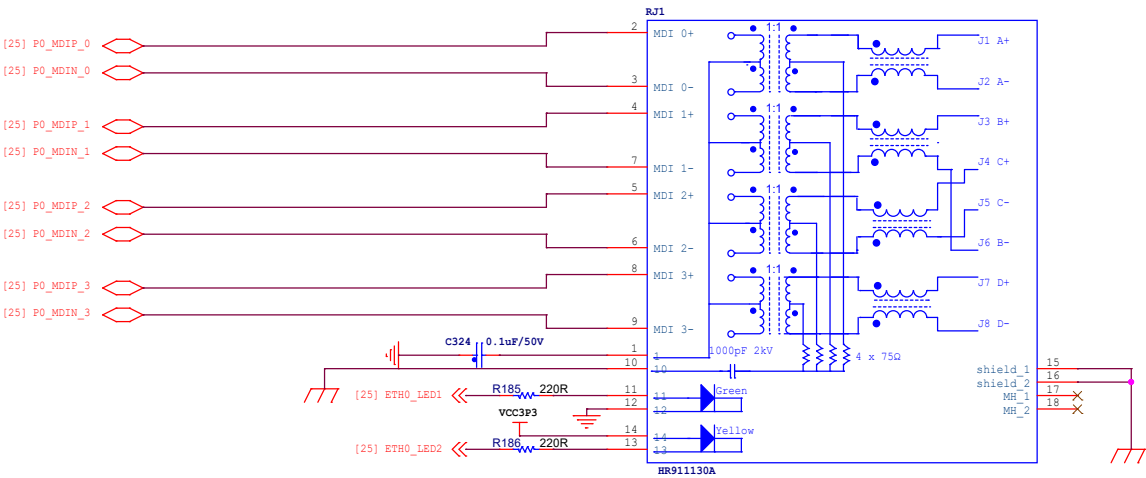
DEFAULT PHYADDR = 00000

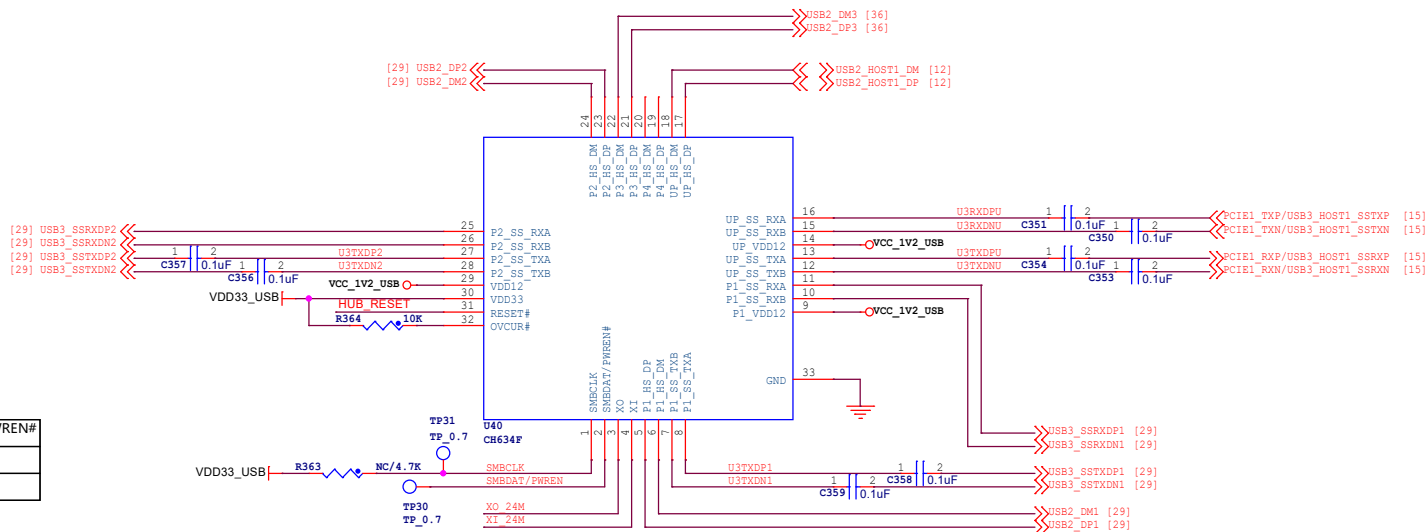
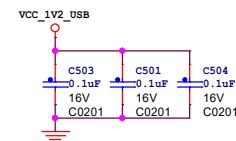


100M << LED1/CFG_LDO0 << ETH1_LED1 [27]
 1000M << LED2/CFG_LDO1 << ETH1_LED2 [27]

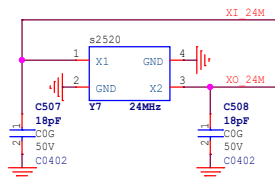
DshanPI-A1 V1.0 Education V1 Vanxak IOQ			
Wuhan Vanxoak Electronics Co., Ltd			
Project:	DshanPI-A1 AI Education V11		
File:	26.Ethernet RGMII1		
Date:	Friday, September 05, 2025	Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>
Sheet:	26	of	30

RJ45 x2

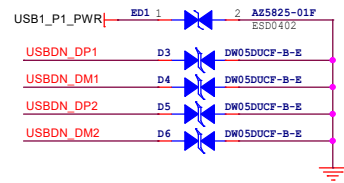
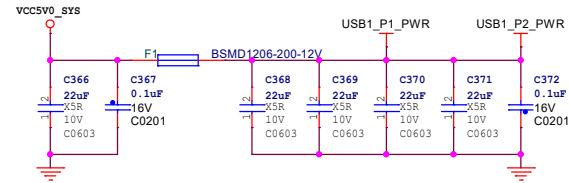
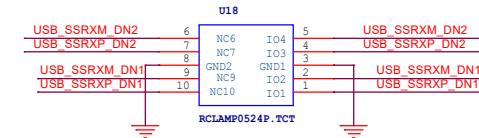
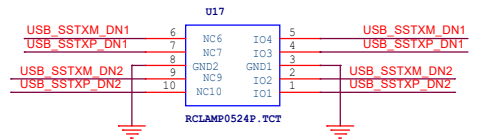
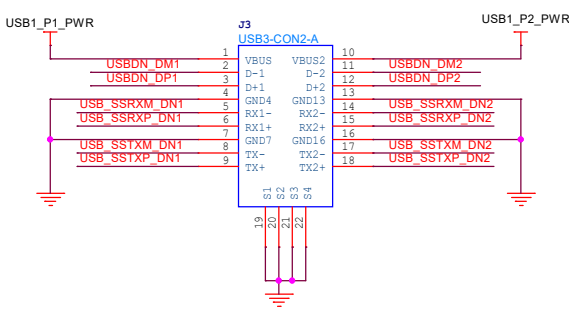
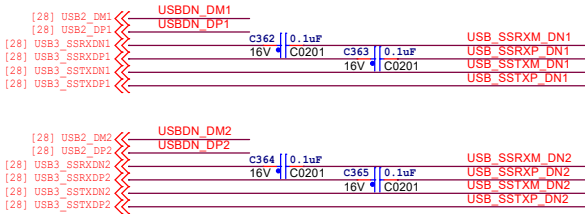




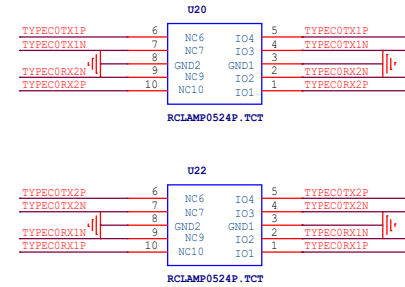
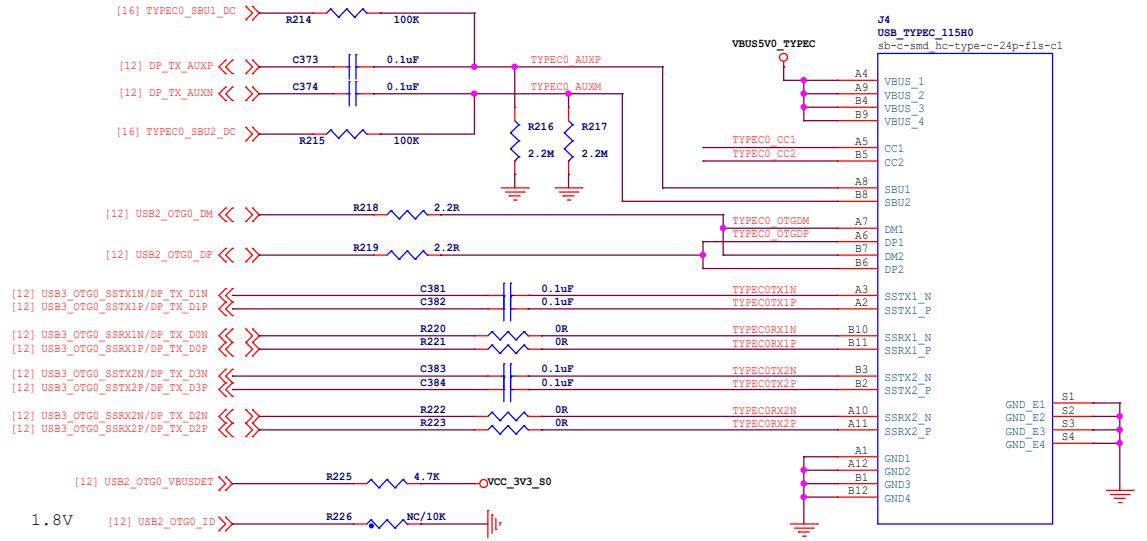
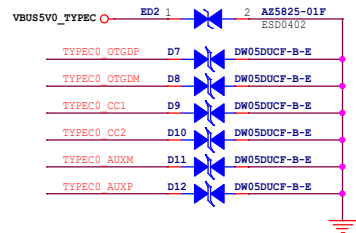
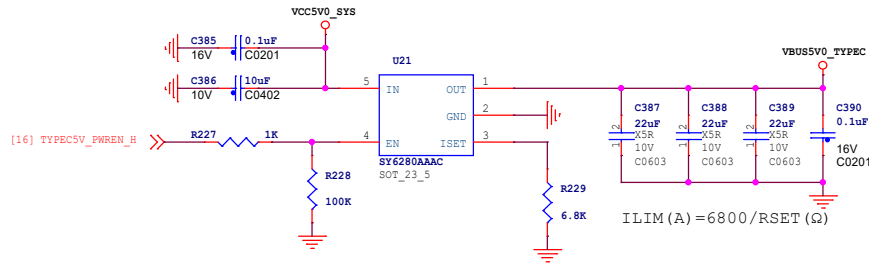
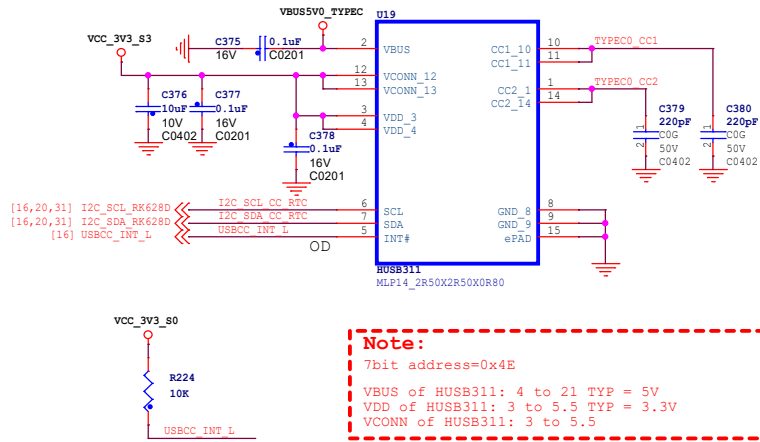
SMBCLK	SMBDAT/PWREN#
Pull up 4.7K	SMBDAT
Leave floating	PWREN



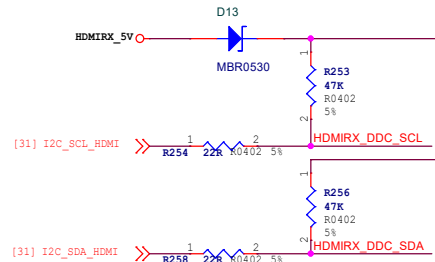
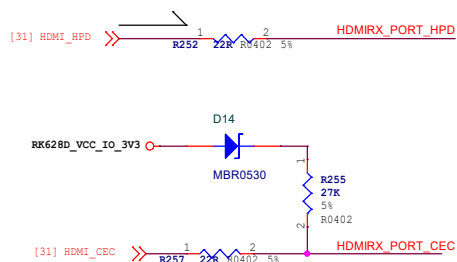
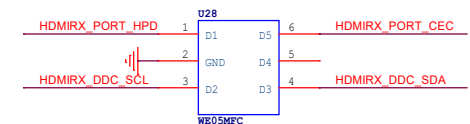
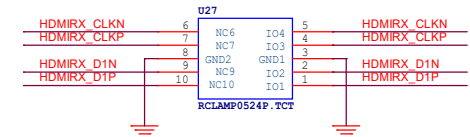
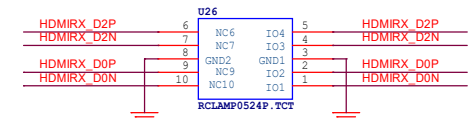
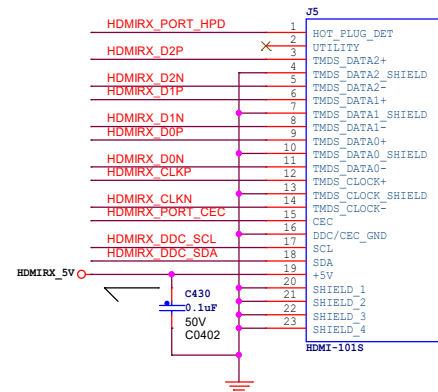
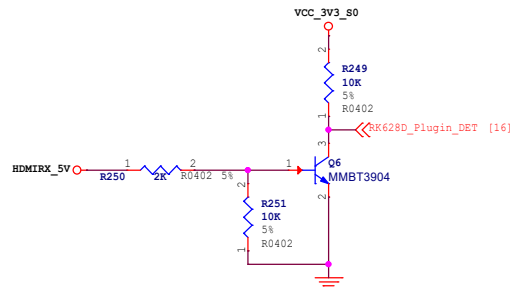
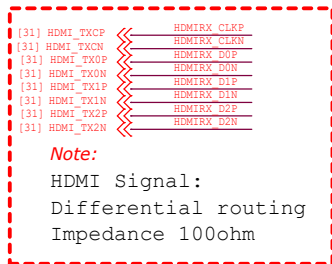
USB3.0 x2



Type-C

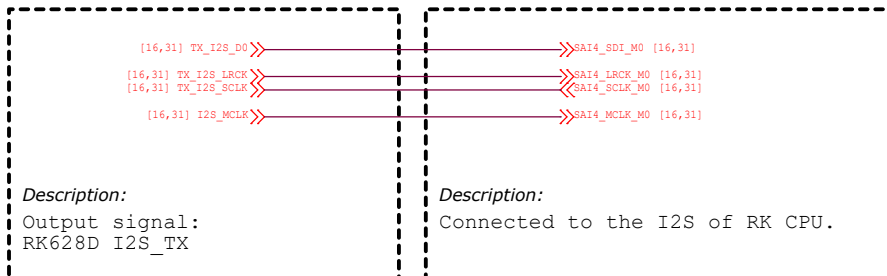
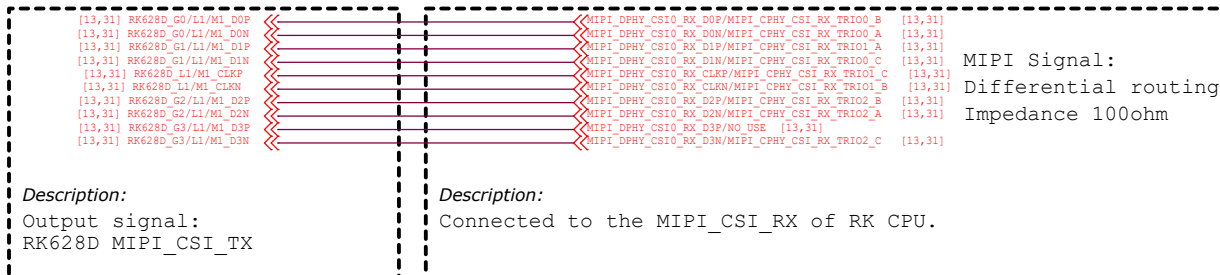


HDMI IN Function

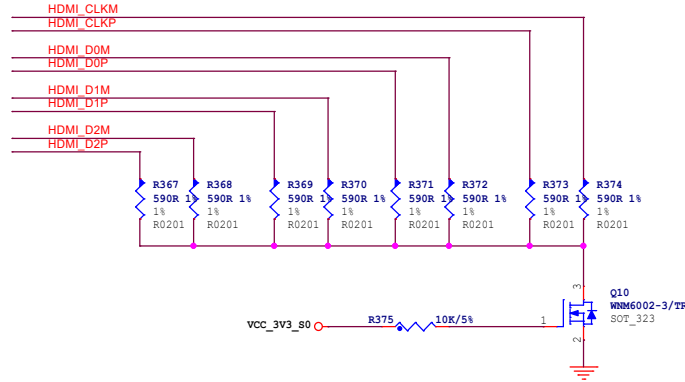
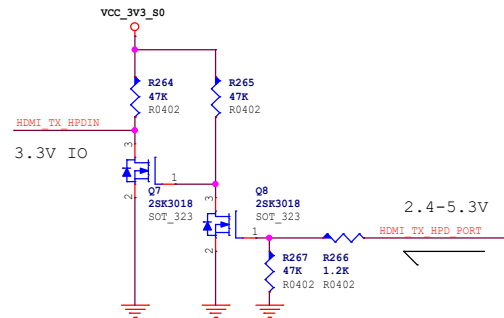
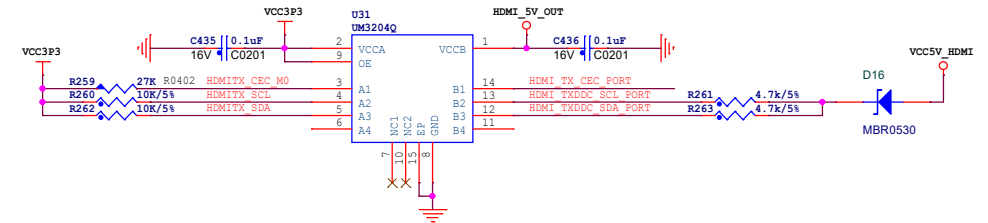
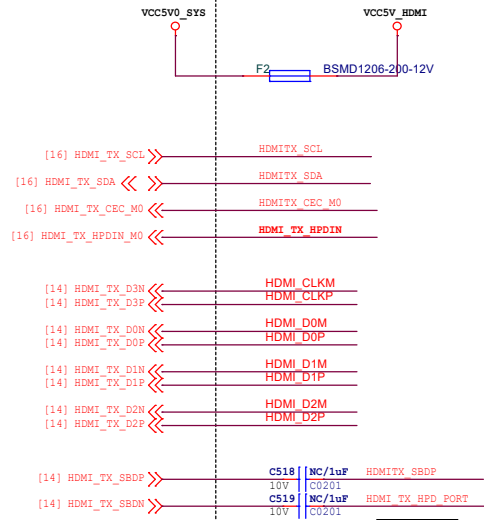
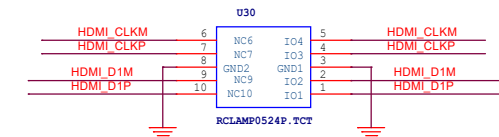
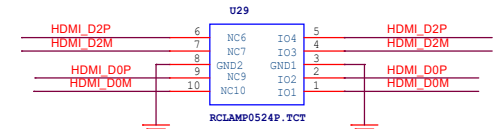
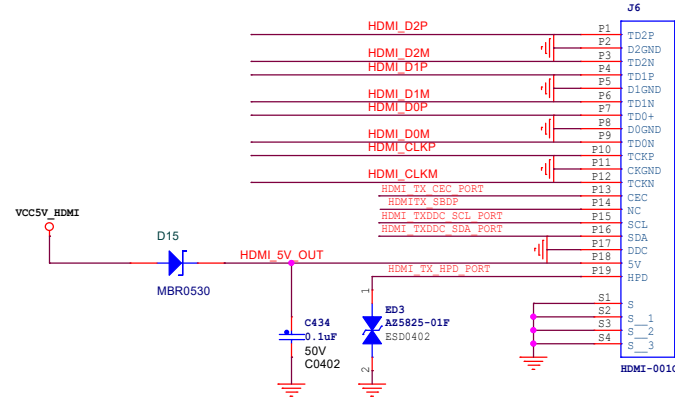
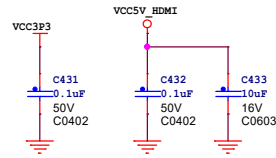


Description:
Default state:HDMI_RX_HPD =0, RK628D_Plugin_DET=1.
When connecting the HDMI cable, RK628D_Plugin_DET will be pulled down(RK628D_Plugin_DET=0).
The RK CPU will detect low level(RK628D_Plugin_DET=0), then RK CPU control RK628D by I2C signal,HDMI_RX_HPD/HDMI_RX_PORT_HPD will be set to 1.

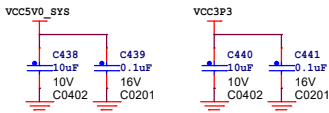
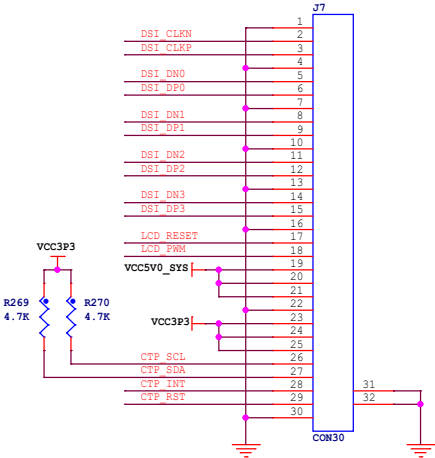
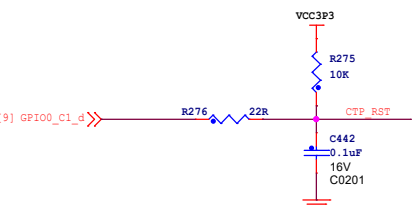
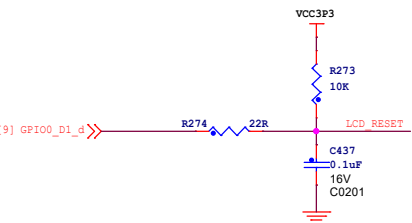
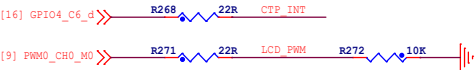
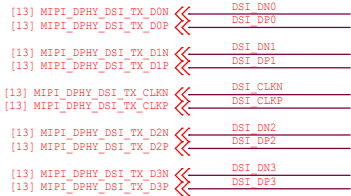
MIPI_CSI_TX & I2S_TX



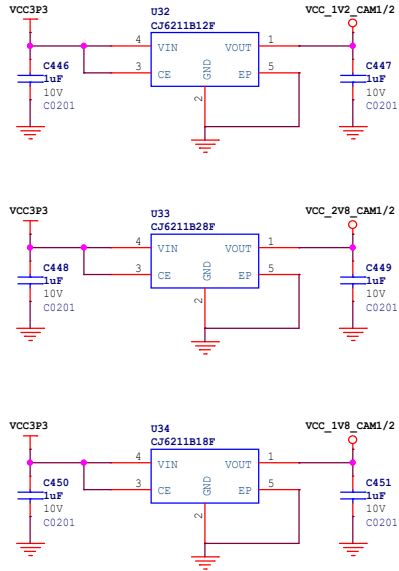
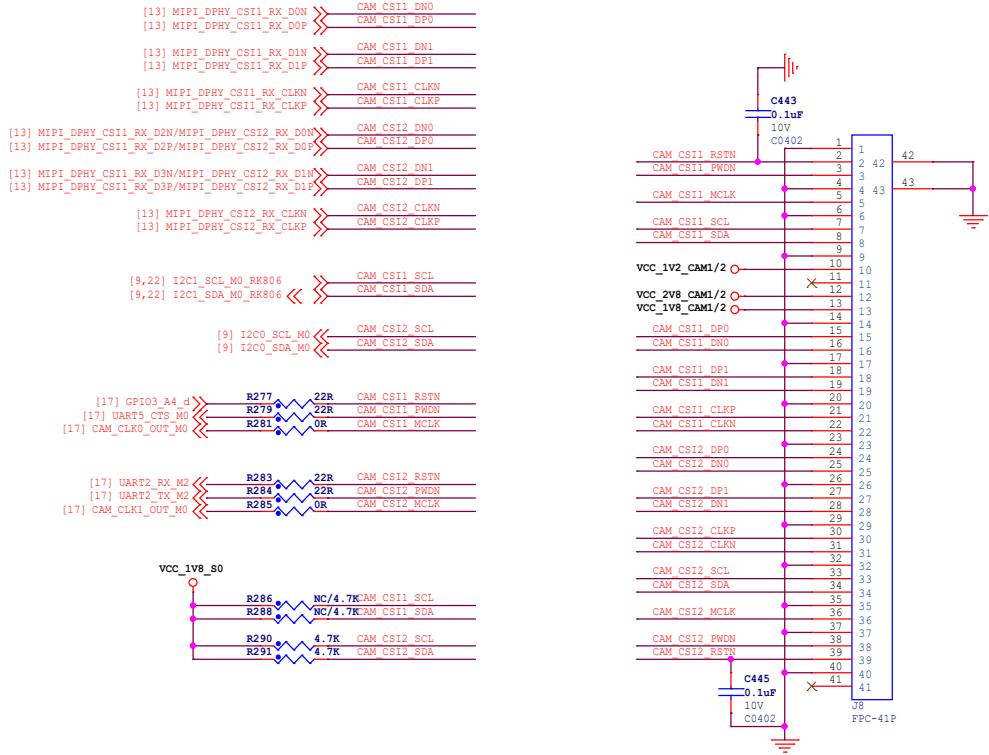
HDMI 2.0



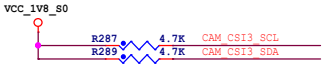
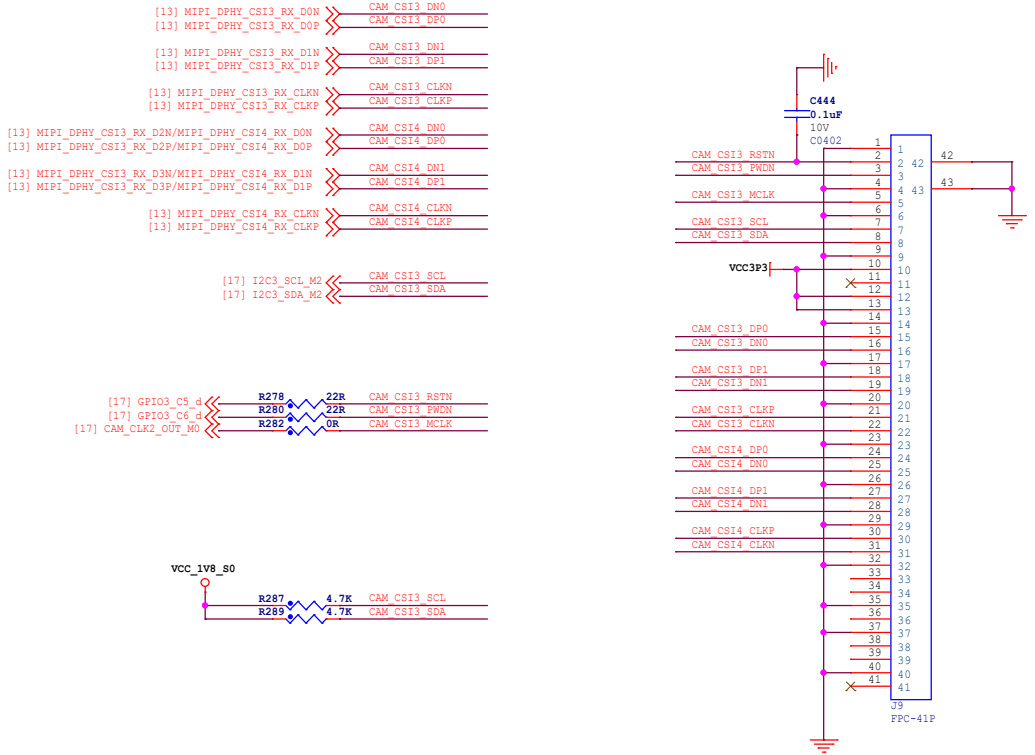
MIPI DSI



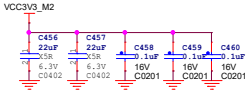
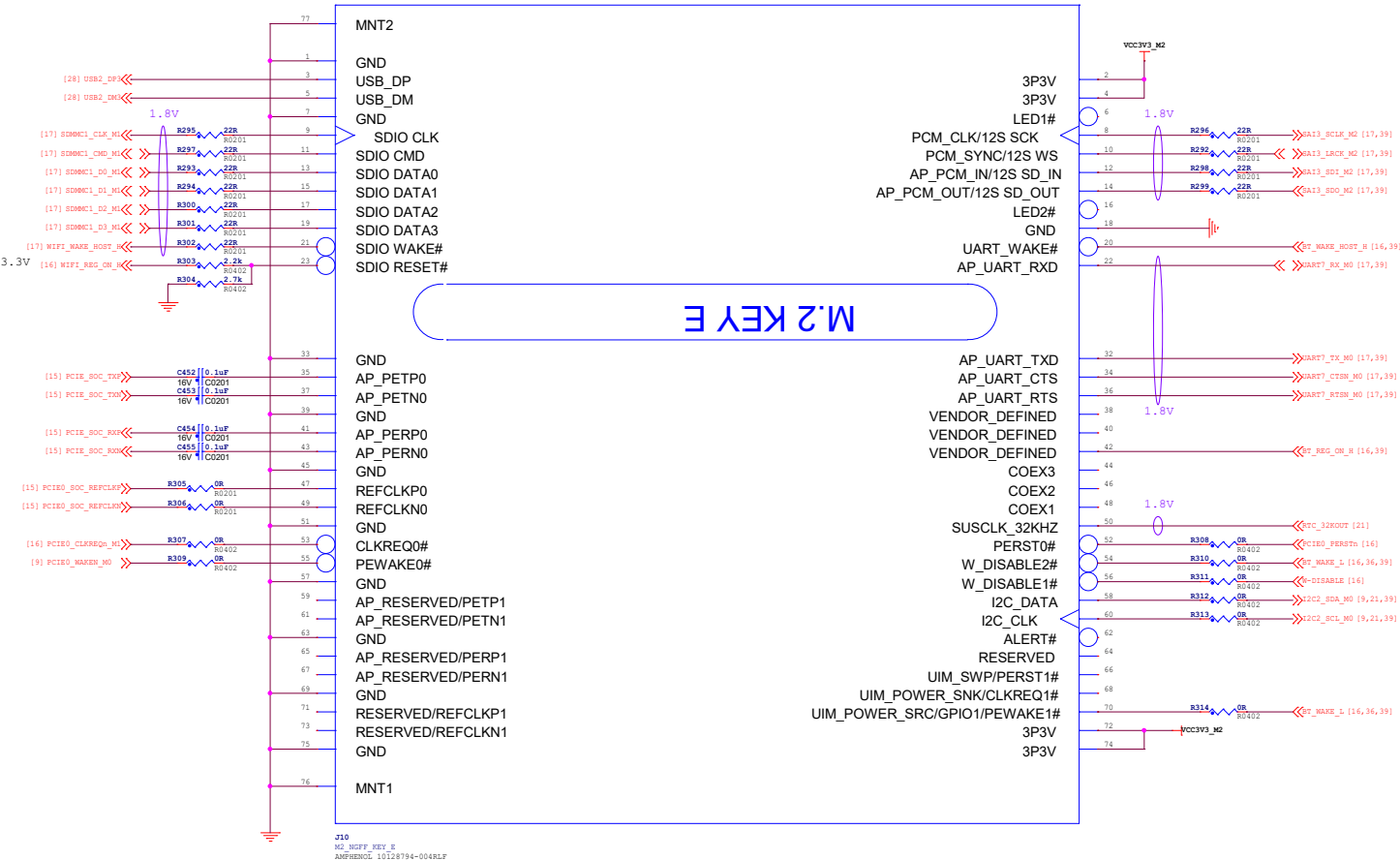
MIPI CSI1/2



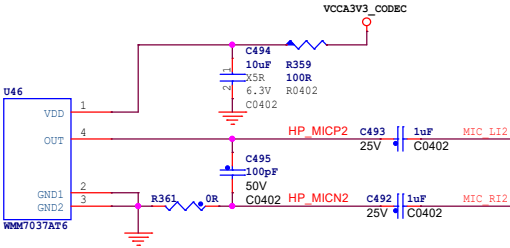
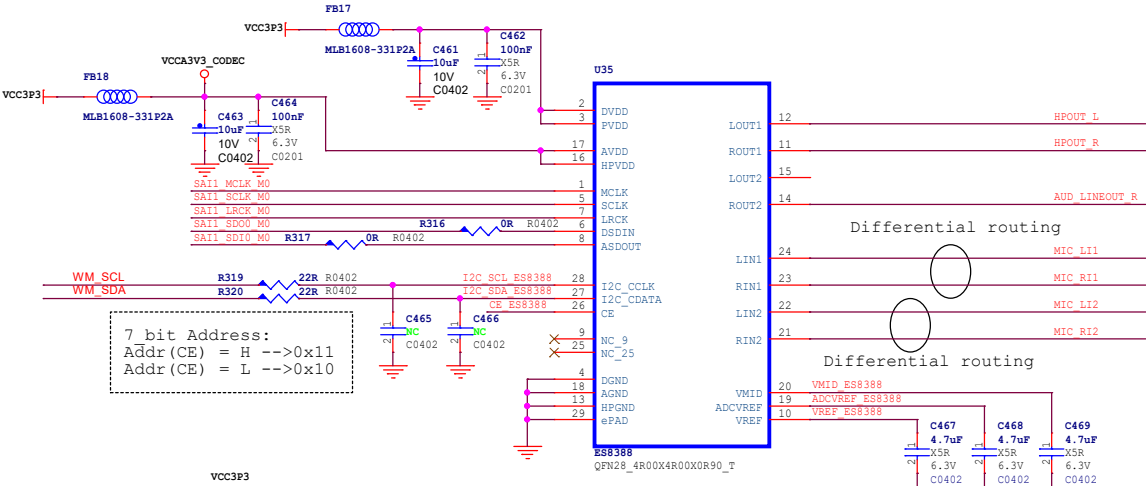
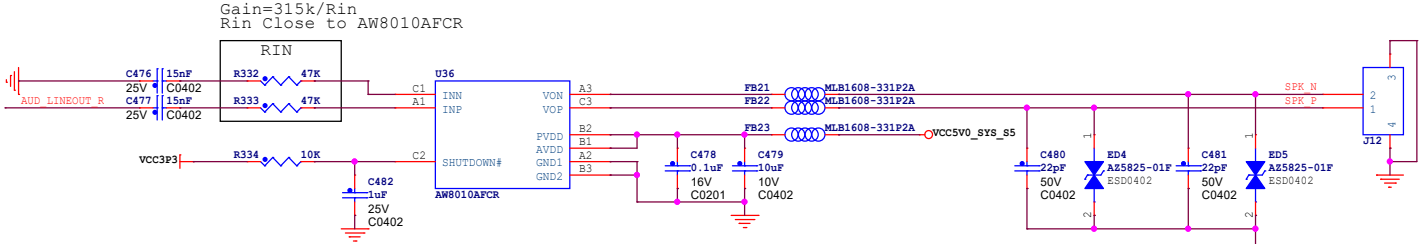
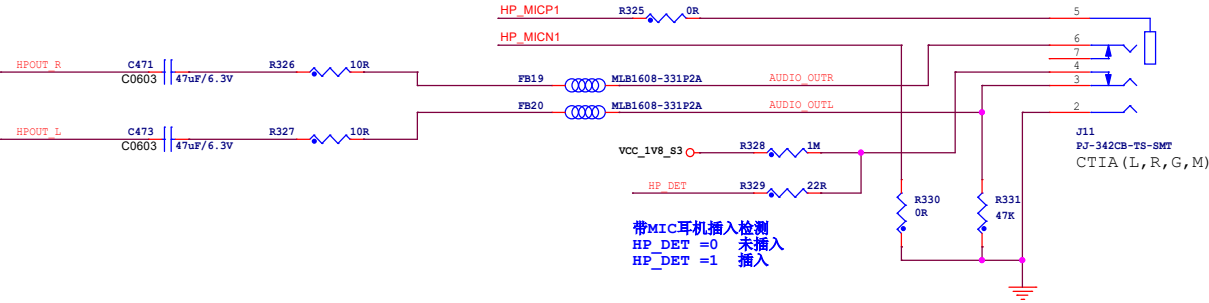
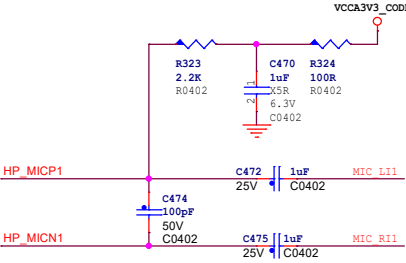
MIPI CSI3/4



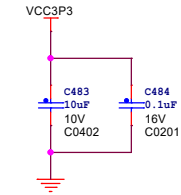
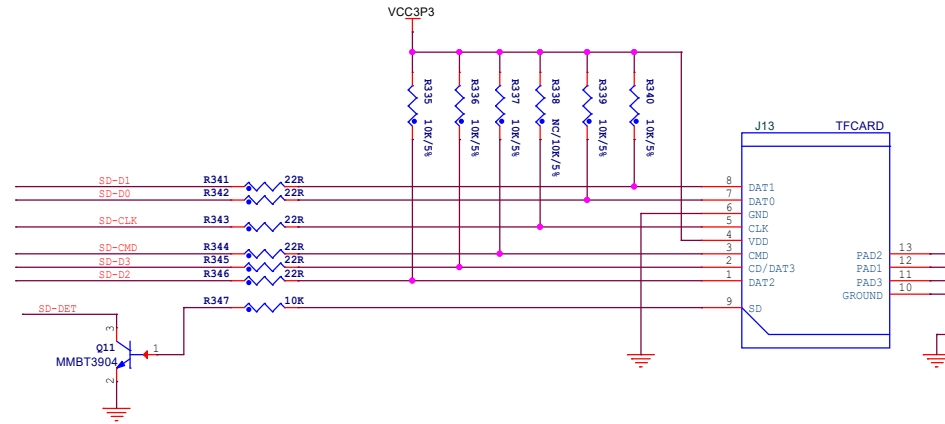
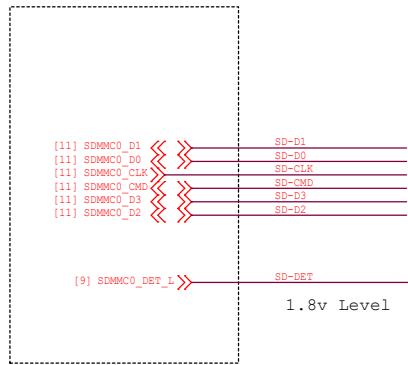
M.2-E Key



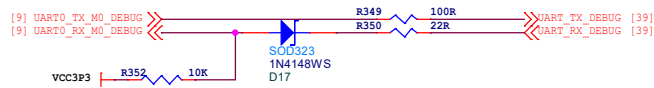
Audio Codec



TF CARD

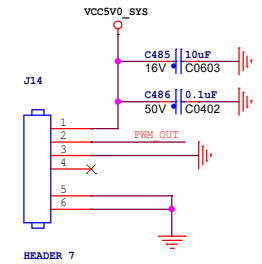
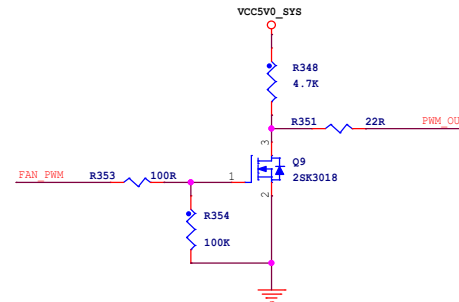
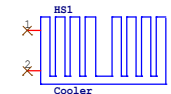


UART DEBUG

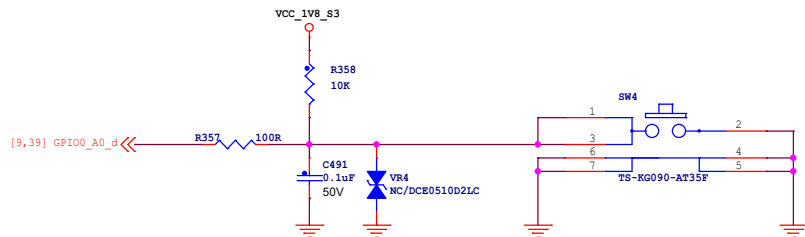


FAN

[9] PWM1_CH0 << FAN_PWM



KEY



DshanPI-A1		Wuhan Vanxoak Electronics Co., Ltd	
Project:		DshanPI-A1 AI Education V11	
File:		38.TF Card/Debug/FAN/KEY	
Date:	Friday, September 05, 2025	Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>
		Sheet:	38 of 39

Expansion Interface

