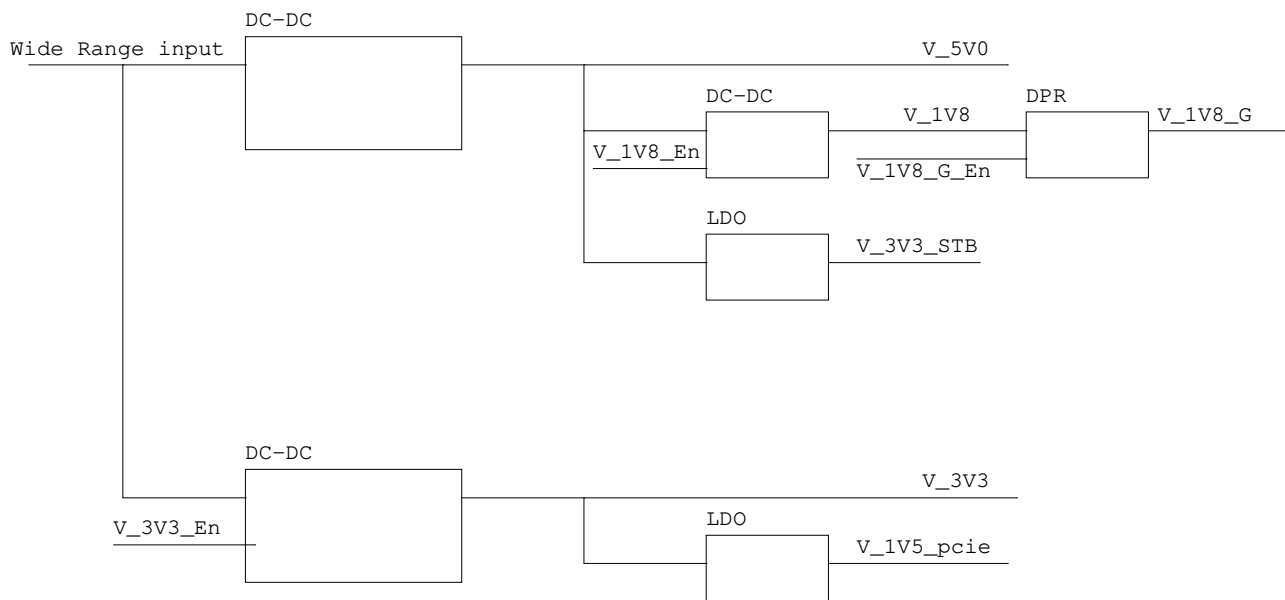
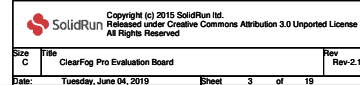
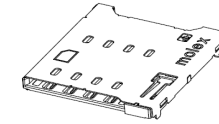
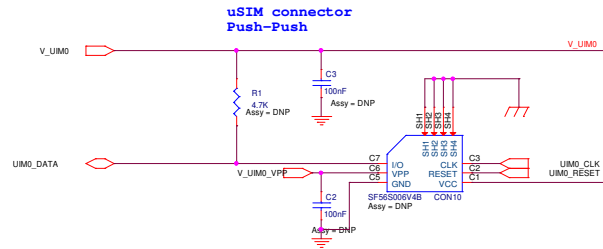


To Extract BOM:

Item\tQuantity\tAssemblyOption\tPart\tPCB Footprint\tDescription\tDataSheet\tManufacturer\tManufacturer P/N\tSolidRun P/N\tReference
{Item}\t{Quantity}\t{ASSY}\t{Value}\t{PCB Footprint}\t{DESCRIPTION}\t{Datasheet}\t{Manufacturer}\t{Manufacturer P/N}\t{SolidRun P/N}\t{Reference}

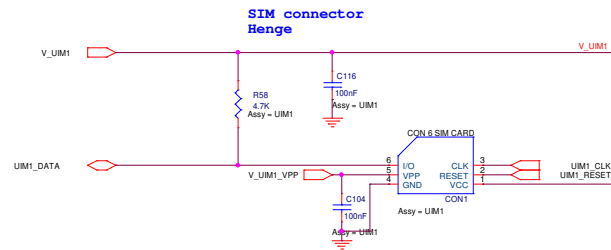


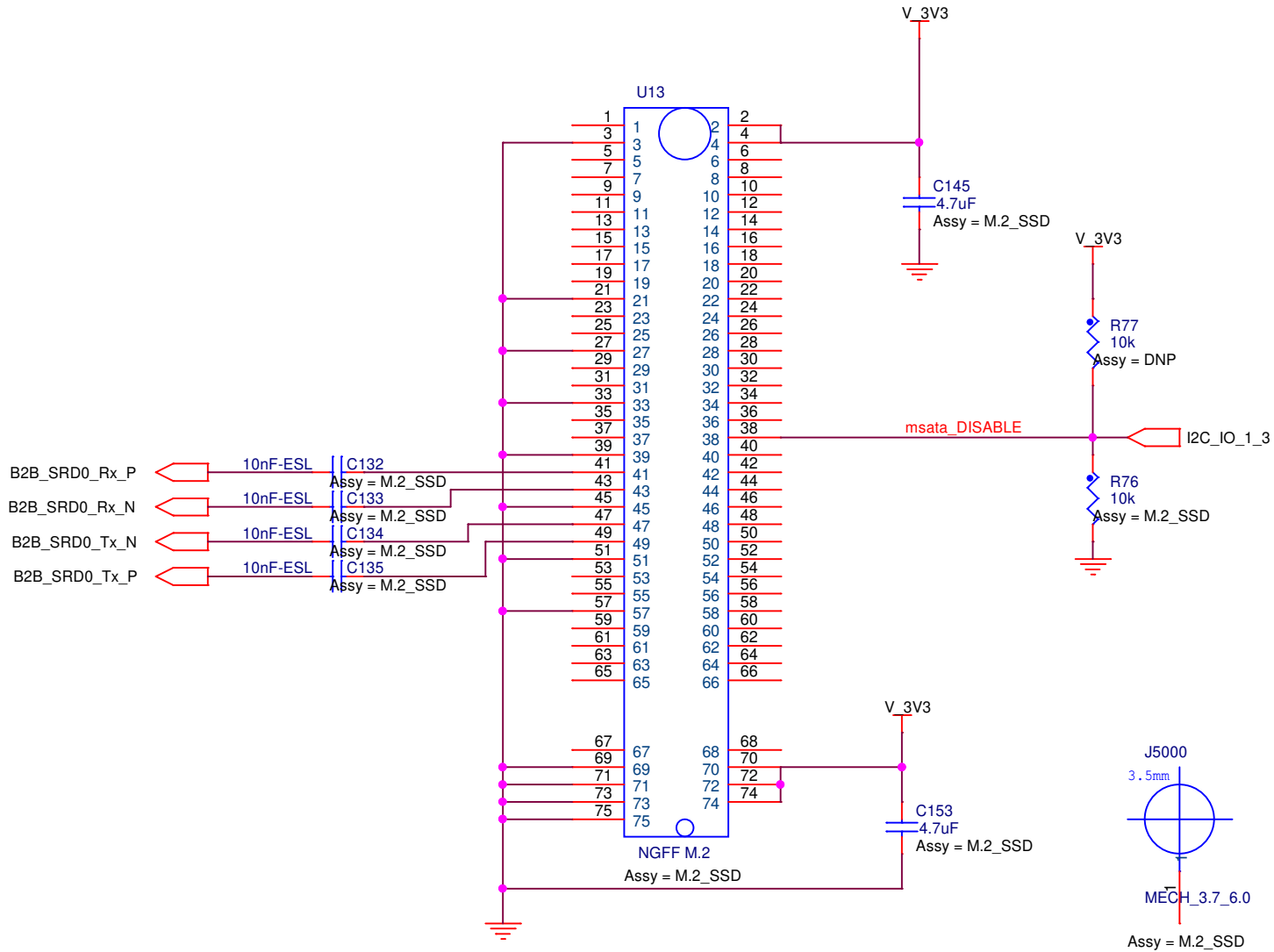




[SIM CARD PIN-MAP]

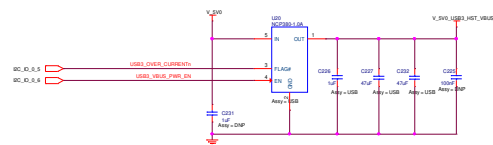
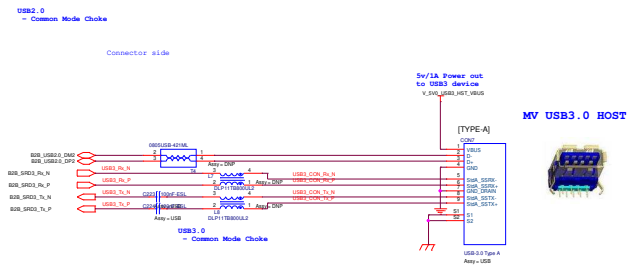
PIN NO.	DESCRIPTION
#1	Vcc(Supply V)
#2	RST(Reset)
#3	CLK(Clock)
#4	Reserved
#5	GND
#6	Vpp(Program V)
#7	I/O
#8	Reserved
G1-G6	GND
Detect	Card Detector
Switch	Common/GND
Card Insertion Condition	DETECT SWITCH
Without Card	Open (OFF)
Card Insertion	Close ION



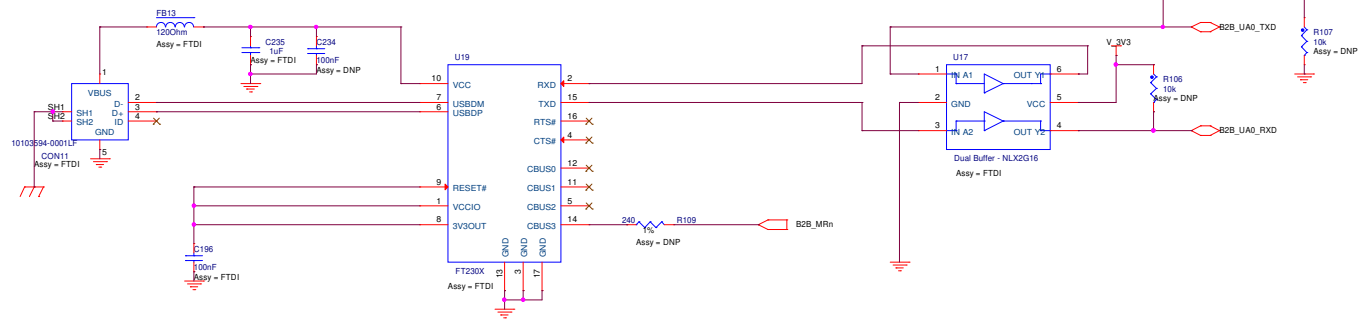


Copyright (c) 2015 SolidRun Ltd.
Released under Creative Commons Attribution 3.0 Unported License
All Rights Reserved

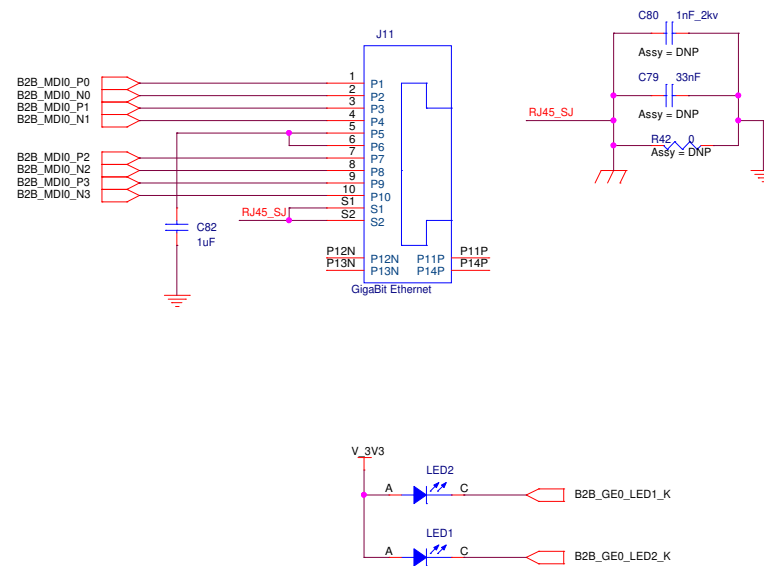
Size	Title	Rev
A	ClearFog Pro Evaluation Board	Rev-2.1
Date:	Wednesday, October 28, 2015	Sheet 5 of 19



microUSB to UART



GE0: RJ45 Connector

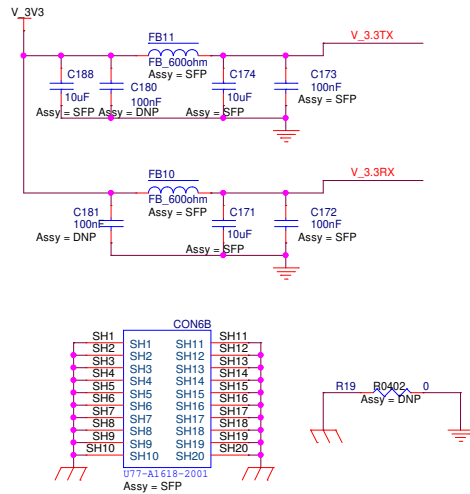


Copyright (c) 2015 SolidRun Ltd.
Released under Creative Commons Attribution 3.0 Unported License
All Rights Reserved

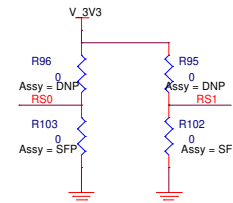
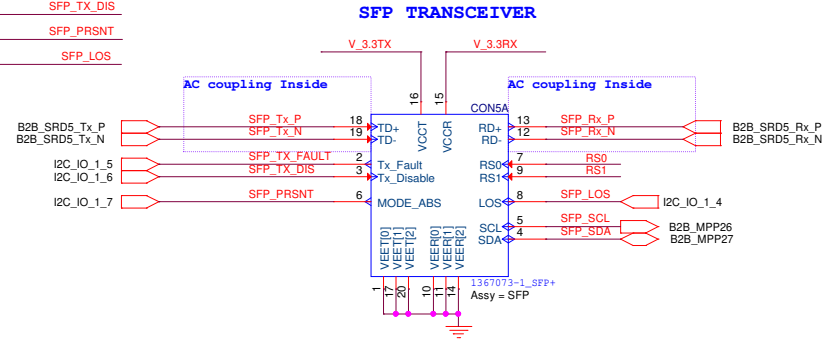
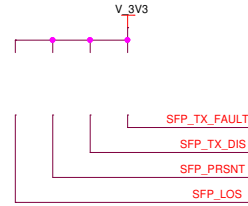
Size	Title	Rev
B	ClearFog Pro Evaluation Board	Rev-2.1
Date:	Wednesday, October 28, 2015	Sheet 8 of 19

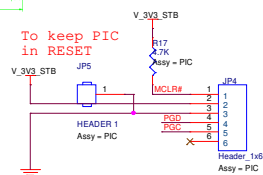
SFP + defines maximum current withdraw from V_3.3TX and V_3.3RX as 300mA each.

SFP TRANSCEIVER Power

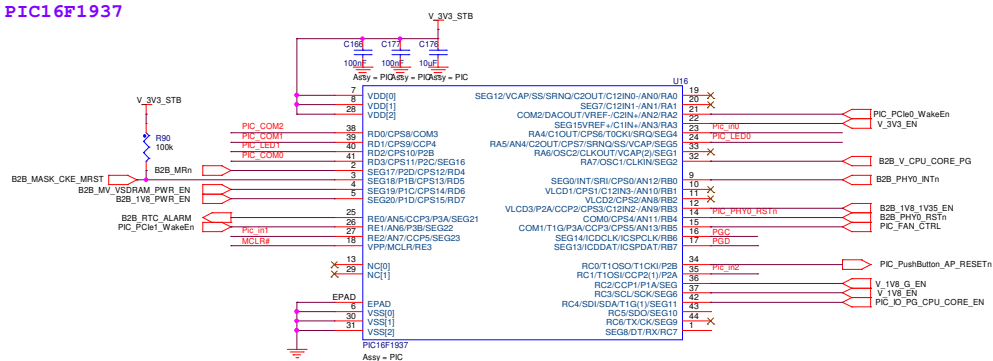


Replaced/Removed pullups with I2C_IO expander's pullups.

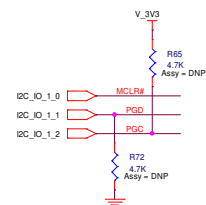
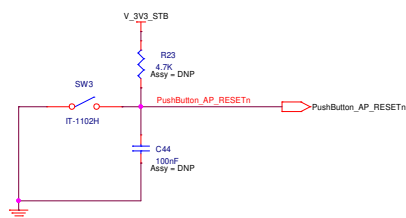




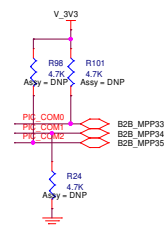
PIC16F1937



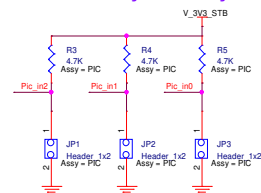
AP Reset Switch (GPIO)



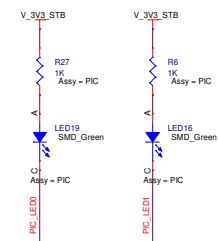
COM with MV Device



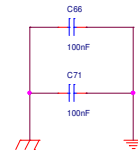
For SW Configuration Usage



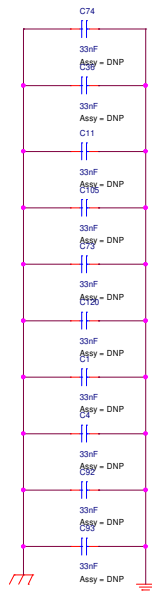
LEDs



Bypass capacitors for MDIO
passing underneath GNDC



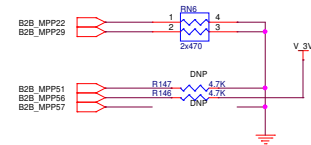
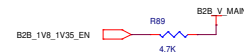
Bypass capacitors between GNDC and GND



B2B_SYSRST_INn B2B_SYSRST_OUTn

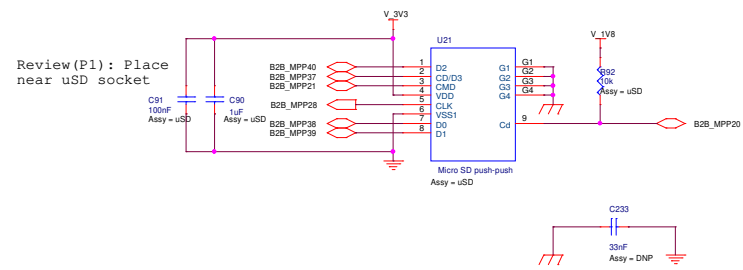
Carrier DC-DC PGOOD Signals will enable CPU DC-DC
on uSom. Signal is pulled up on uSom.

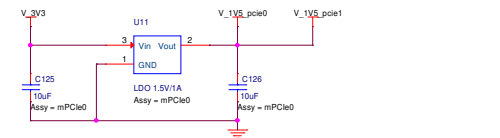
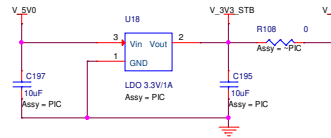
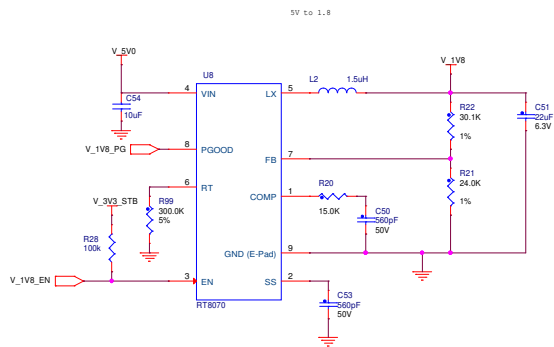
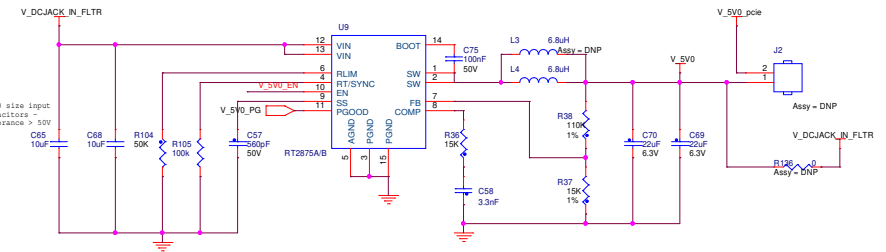
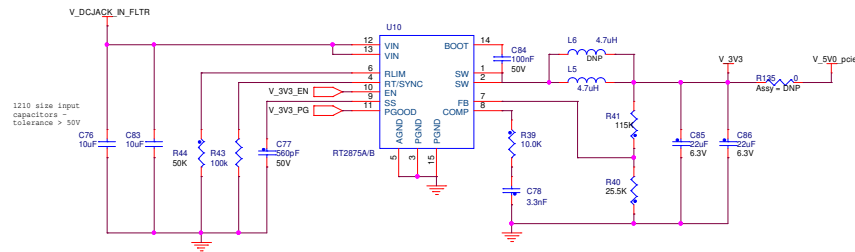
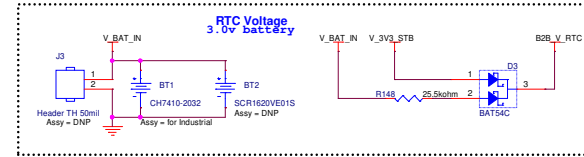
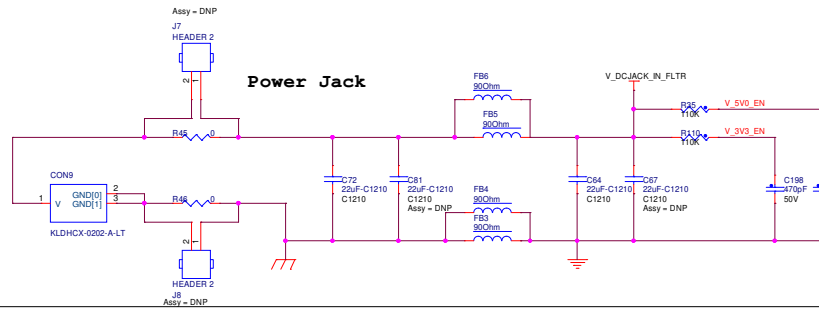
V_5V0_PG B2B_OD_3V3_PG
V_3V3_PG PIC_IO_PG_CPU_CORE_EN
V_1V8_PG



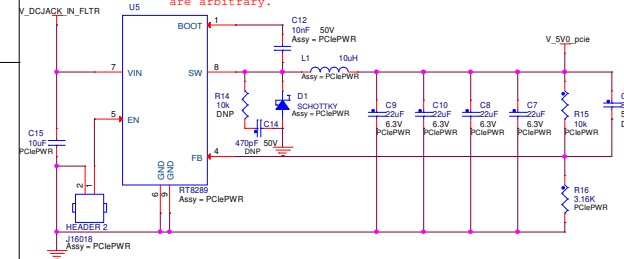
PushButton_AP_RESETrn PIC_PushButton_AP_RESETrn
FAN_CTRLn PIC_FAN_CTRLn
Assy = PIC

FAN_CTRL B2B_MPP35
PushButton_AP_RESETrn B2B_MPP34
Assy = PIC

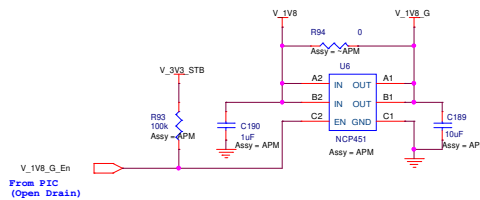
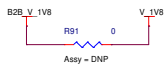




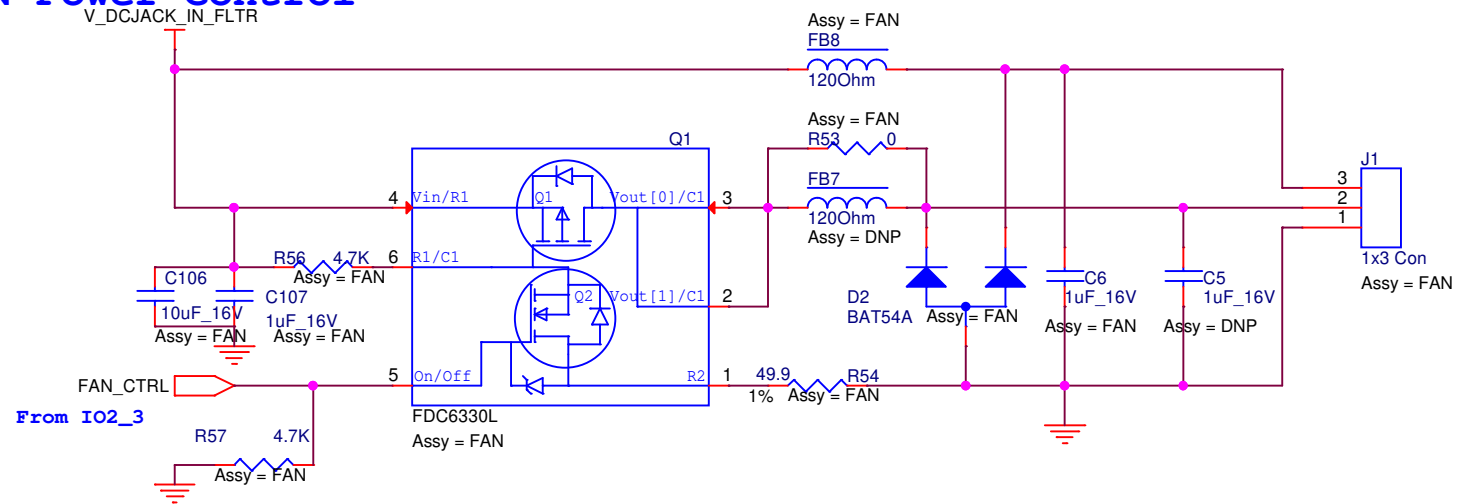
Snubber filter to be used for EMI suppression only if needed. Values need to be changed. Current values are arbitrary.



To be used if uSoM can power the carrier 1.8V domain.



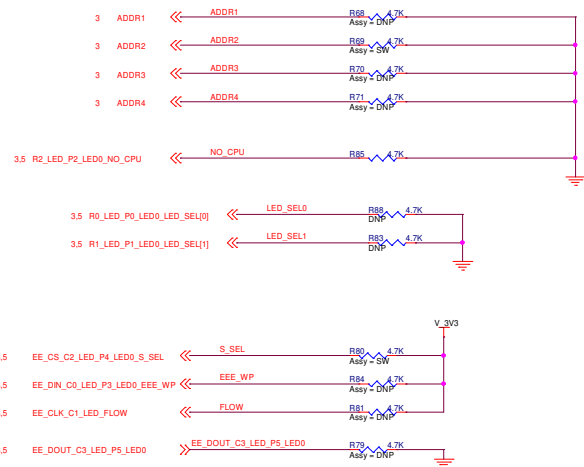
FAN Power Control



Copyright (c) 2015 SolidRun Ltd.
Released under Creative Commons Attribution 3.0 Unported License
All Rights Reserved

Size A	Title ClearFog Pro Evaluation Board	Rev Rev-2.1
Date:	Wednesday, October 28, 2015	Sheet 15 of 19

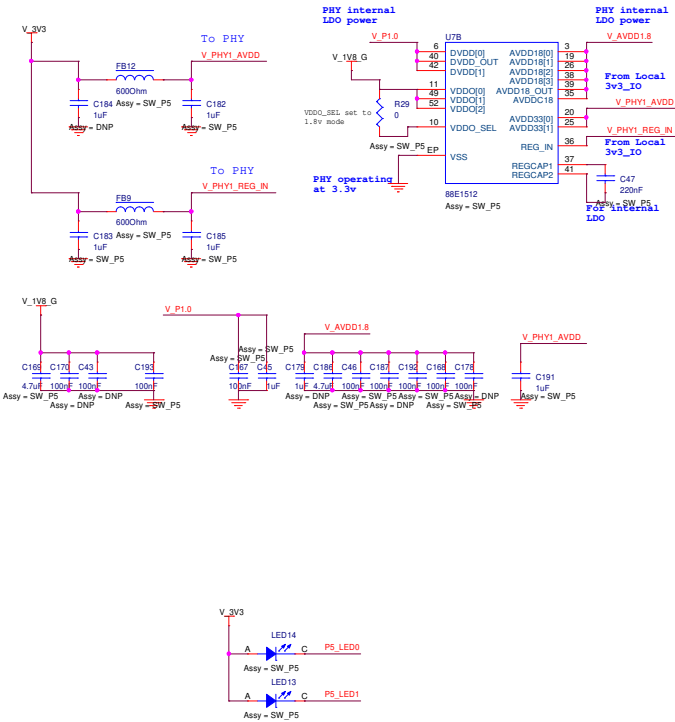
ADDR0 = alway 0x0
SMI ADDRESS is the inverted value = 0x4



Pin	Name	Functionality	Default	Jumper/ DPR
35	NO_CPU	CPU ATTACHED	PU	PD.NC
34	LED_SEL[1]	LED Functionality	PU	PD.NC
33	LED_SEL[0]	LED Functionality	PU	PD.NC
39	S_SEL	Connect serdes to port 4 or 5	PD	PU
38	FLOW	Advertise auto-neg flow control	PD	PU
36	EEE_WP	Enable energy efficient Ethernet	PD	PU.NC
70	P5_VDDOS[0]	Port 5 power rail select	PU	PD
66,68,69	P5_VDDOS[1]	Port 5 power rail select	PU	PU
94	P6_VDDOS[0]	Port 6 power rail select	PU	PD
90	P6_VDDOS[1]	Port 6 power rail select	PU	PU
91,92,93	P6_OUTD[2:0]	0x7 = RGMII	PU	No option
85,86,87,88	ADDR[4:1]n	SMI ADDRESS	PU	0x2

PHY Power configurations

88E1512 power configurations:
1. using internal lv8 and lv0 regulators.
2. VDDO_SEL config VDDO to operate at 2v3/3v3.



PHYADD configuration

88E1512 PHY configuration options:
PHY_address=1

Table 53: Configuration Mapping

Pin	CONFIG Bit	CONFIG Bit 5	Value Assignment
CONFIS	0	0	PHYADD[0] = 0 VDDO_LEVEL[1] = 3.3V
CONFIS	1	1	PHYADD[0] = 1 VDDO_LEVEL[1] = 3.3V
CONFIS	1	0	PHYADD[0] = 0 VDDO_LEVEL[1] = 2.5V
CONFIS	0	1	PHYADD[0] = 1 VDDO_LEVEL[1] = 2.5V

1. This is valid only for 88E1512/88E1512. For 88E1512, the VDDO_LEVEL[1] is forced at 1.8V, hence the bit mapping for VDDO_LEVEL[1] is ignored.

1. PHYADD=1
2. VDDO=3.3v

