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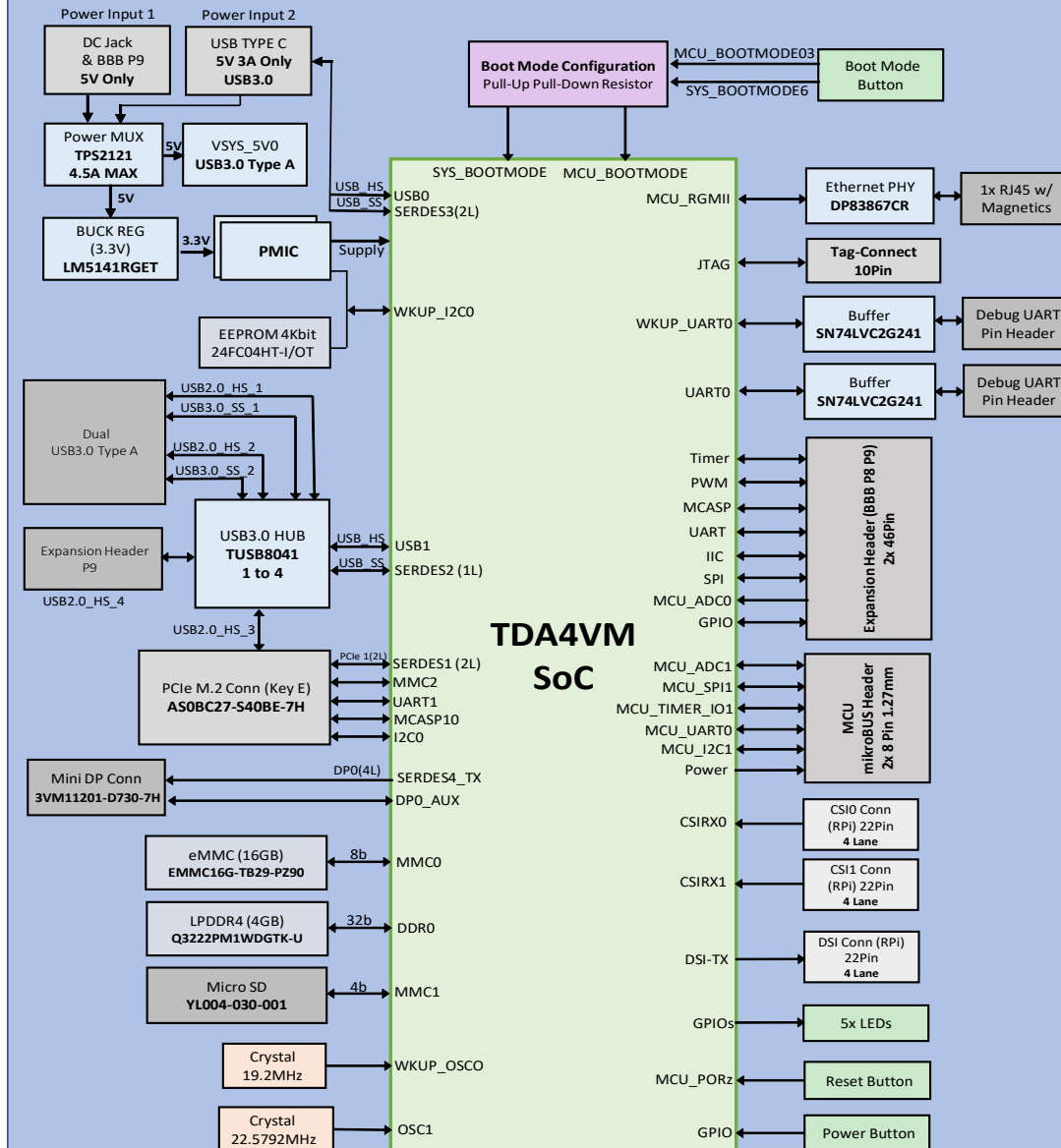
[illegible]

REVISION HISTORY

DATE	REVISION	DESCRIPTION OF CHANGES	AUTHOR
21 Dec 2021	BeagleBone AI-64_SCH_Rev B_211221	1. Initial Production Release, 425PCS PCBA. 2. The PCB Revision for this board is Rev B.	Junqing.Xin
02 Jun 2022	BeagleBone AI-64_SCH_Rev B1_220602	1. There is no changes in SCH, but only updated the PCB Footprint for production. 2. The PCB Revision for this board is Rev B1.	Junqing.Xin

SYSTEM BLOCK DIAGRAM

BeagleBone AI -64



<Variant Name>

3-Phase DUAL PMIC PDN Recommended for New Designs (3-Phase Buck supplying VDD_CPU)

DRA829/TDA4VM 3-Phase Dual Leo2.0 PDN-0C (Power Rail & GPIO Mapping Overview)

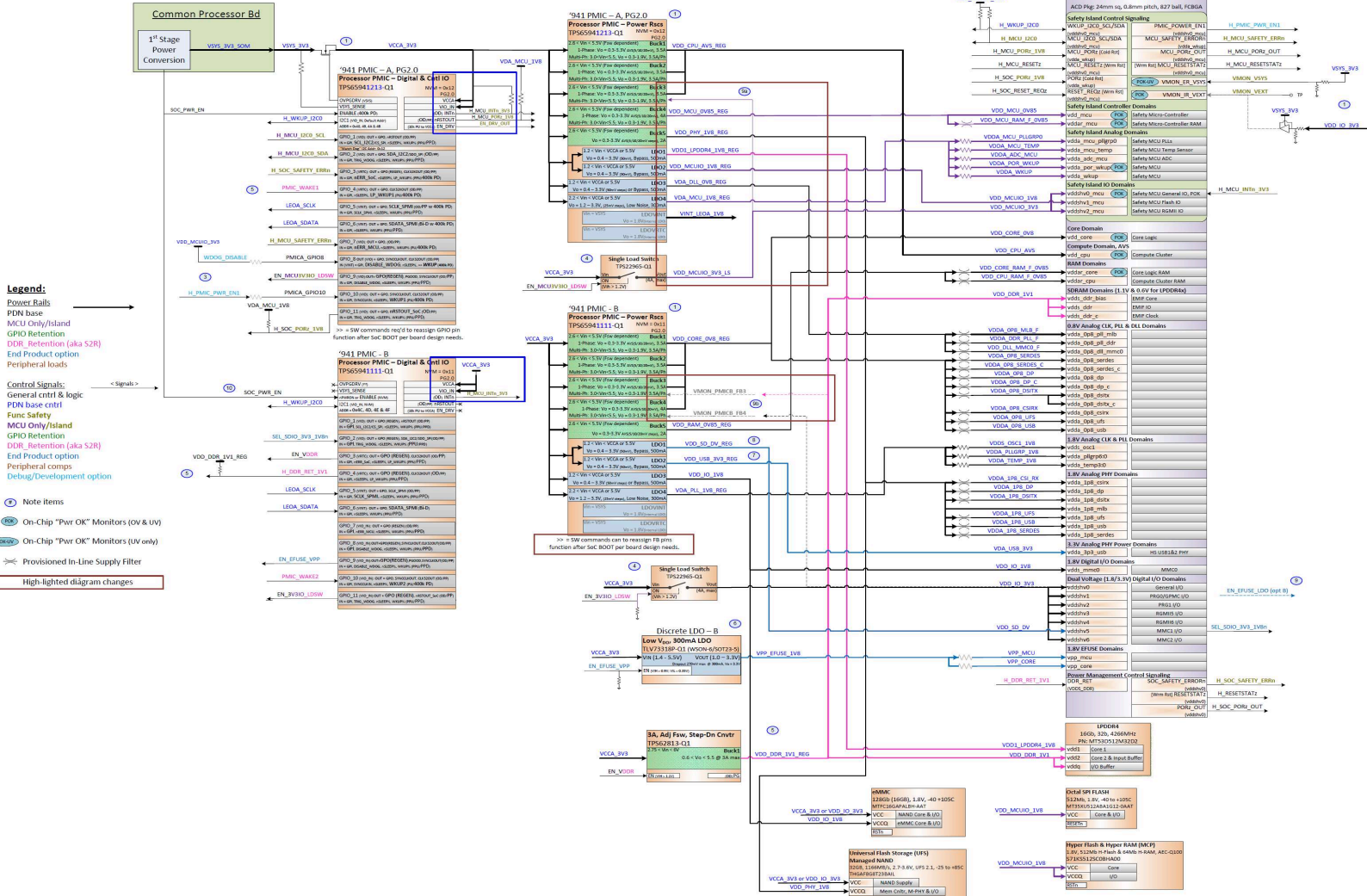
Leo PMIC-A, PN TP565941213RWERQ1 (TI PN ID = 1, MP Buck Rails = 2, NVM ID = 13, PG2.0)
Leo PMIC-B, PN TP565941111RWERQ1 (TI PN ID = 1, MP Buck Rails = 2, NVM ID = 12, PG2.0)

Features Supported (EVM Max Features):

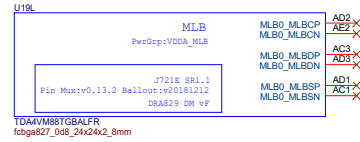
- SoC performance: Max 2.0GHz clock with SERDES interfaces operational
- Functional Safety: ASIL-D capable system with independent MCU & Main power for FFI
- SDRAM: 32Gb, 4-Die, 32b, 4266MT/s, LPDDR4 mode
- Boot & Mass Flash: Octal SPI or Hyperflash (SR1.1 only) & eMMC, UFS
- Low power modes: MCU Only & **DDR Retention**

- Signaling Levels: MCU & Main Dual VIO
- End Product Options:
 - Compliant high-speed SD Card
 - Compliant USB 2.0 data eye
 - HS Soc Efuse programming on-board

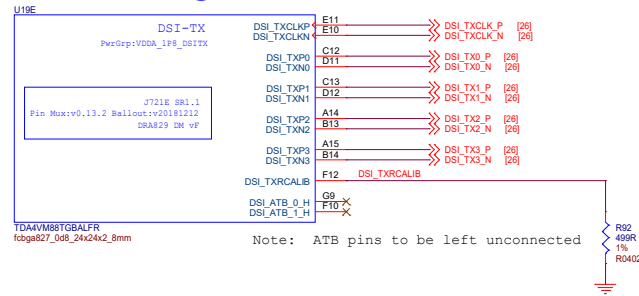
- V0.14 1/27/2021
- Added example of VDD_IO_V3V3 ON/OFF monitoring by Soc's VMON_IR_VEXT input connection option to voltage buffer & voltage R-div needed to interface with Soc's internal R-div network optimized for monitoring 1.8V power rails.
 - Added 2x ext voltage monitoring inputs options for ON/OFF monitoring by Hera PMIC of any safety critical system power rails. Hera's quad buck config can reassign remote sense feedback inputs (FB3 & FB4) for power rail monitoring.
 - Updated notes 1 & 9 accordingly.
- V0.15 2/13/2021
- Following final PMIC NVM review for defining new common PM ("1213") for Leo PG2.0 used in PDN-0C & -1A:
- Update notes
 - Changed PMIC-A FB3 VMON input to be connected to VCCA_V3V3 since VDD_MCUIO_V3V3 rail is not supported, see note 9a.
 - Added PMIC-B FB3 & FB4 FB4 assignment for VMON by SW after Soc boot for ext power rail monitoring options, see note 9b.
- V0.16 3/2/2021
- Removing discrete load switch from supplying PMIC's VIO, in since PG2.0 PMICs validation testing confirms no excessive glitches on GPIO or reset signals during of NVM initialization. Related "Note #2" has been removed.



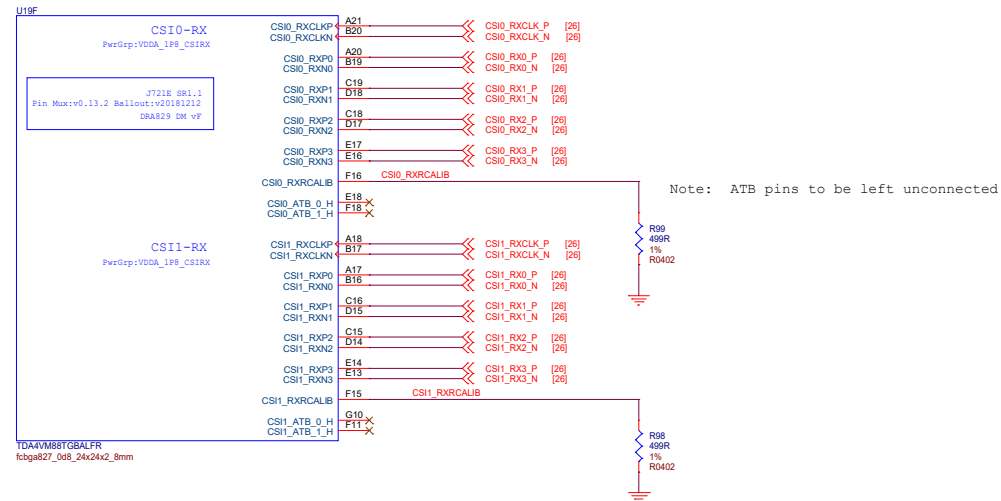
MLB



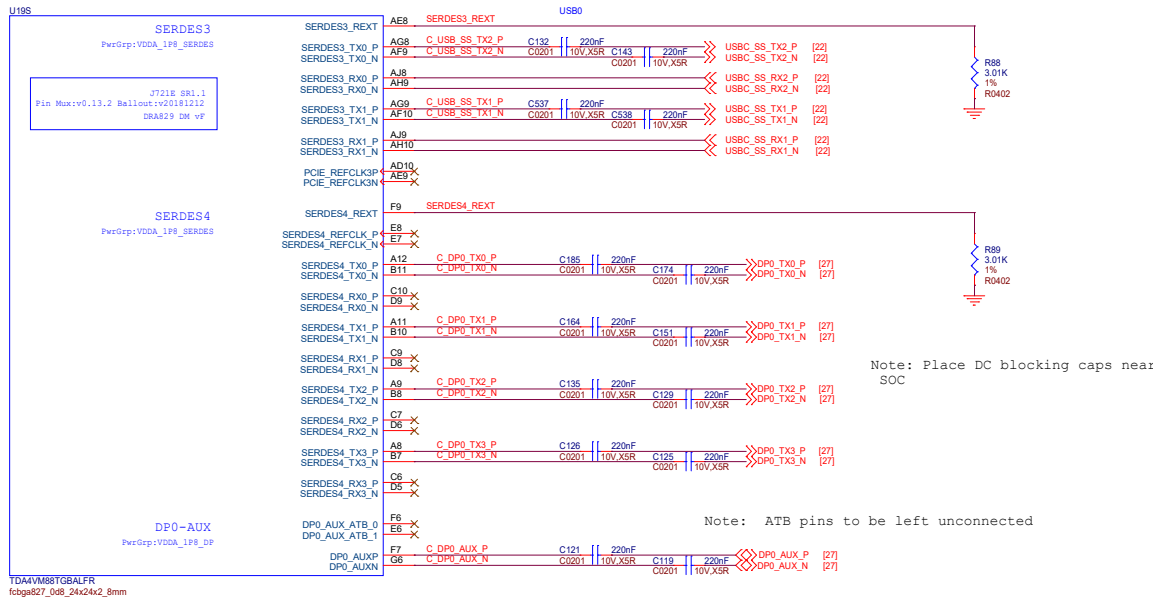
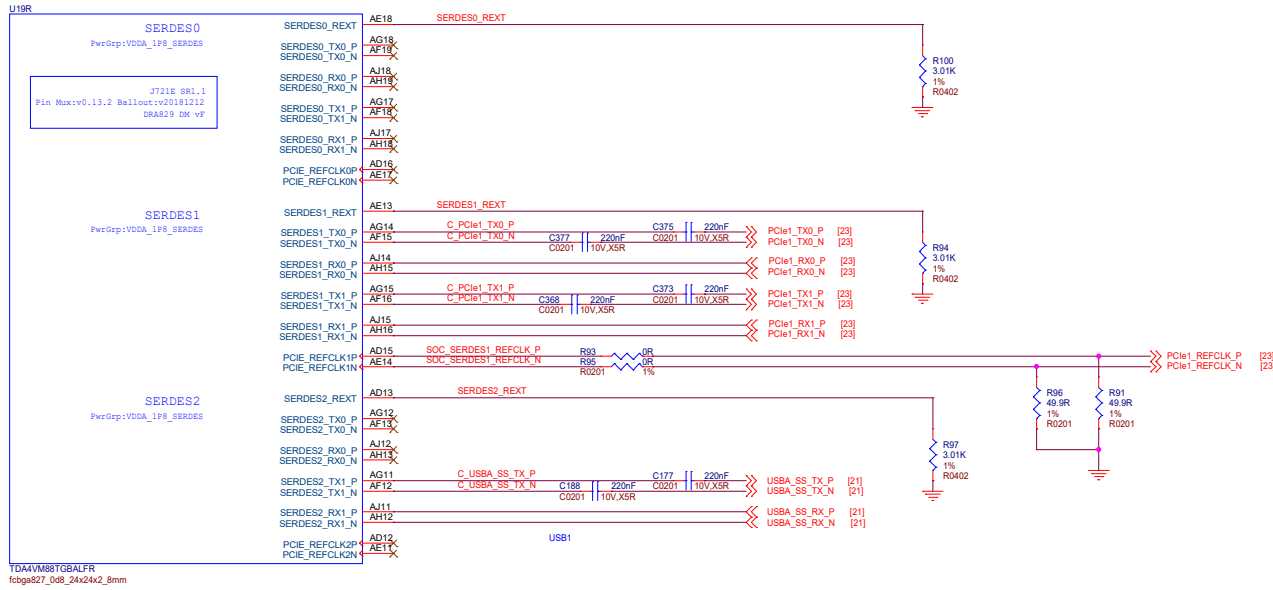
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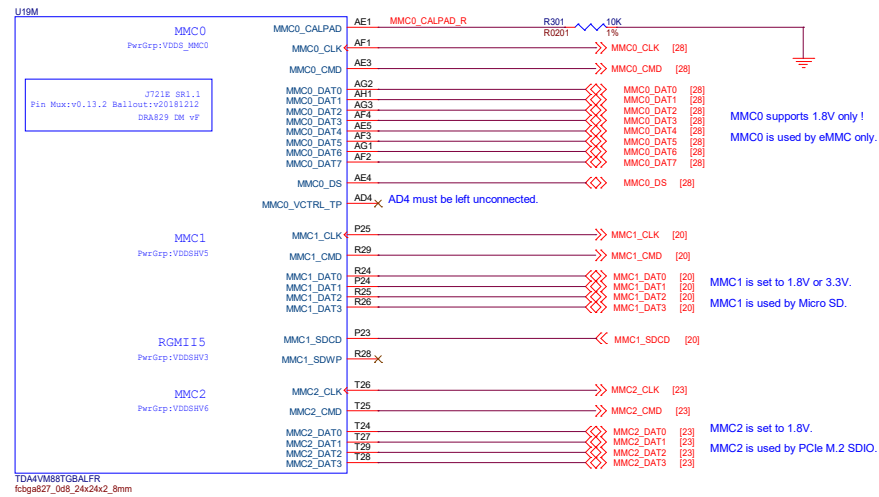
CSI Interface



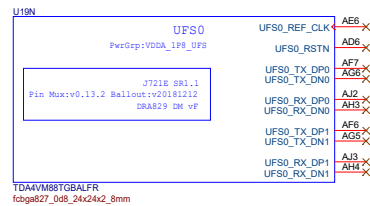
SERDES

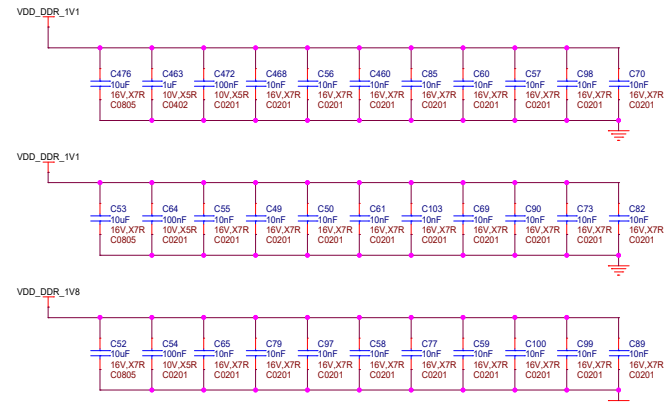
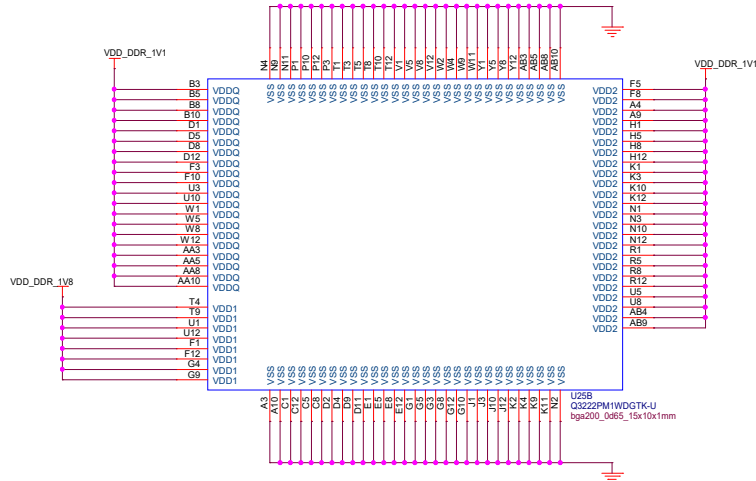
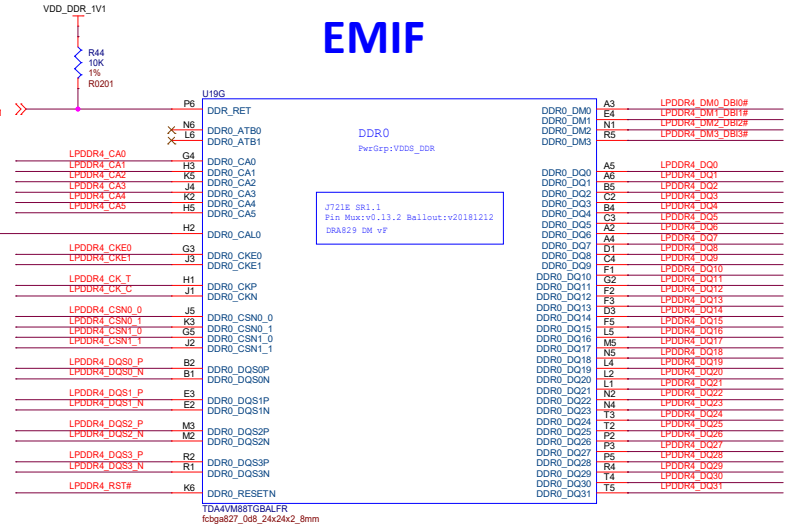
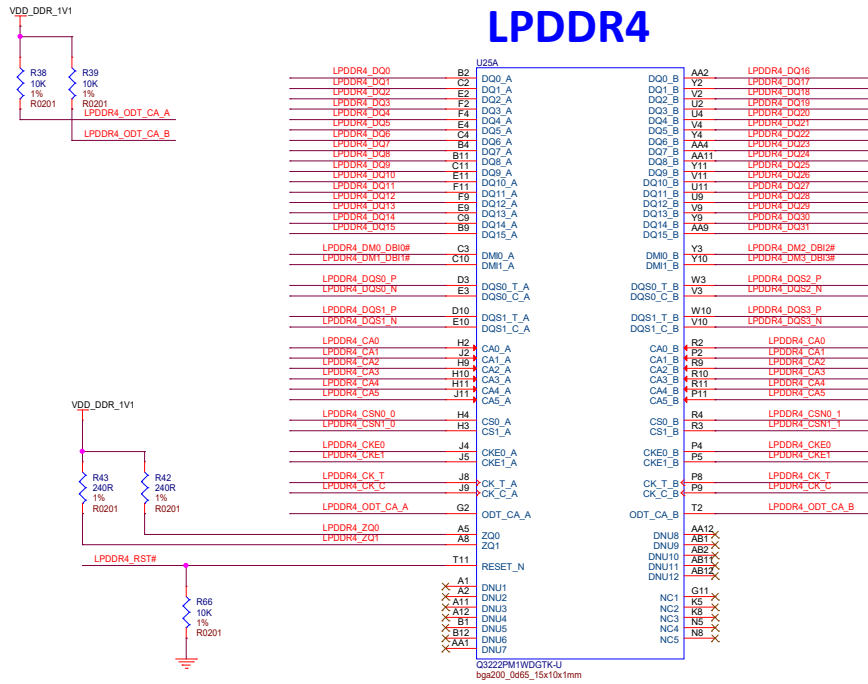


MMC Interface

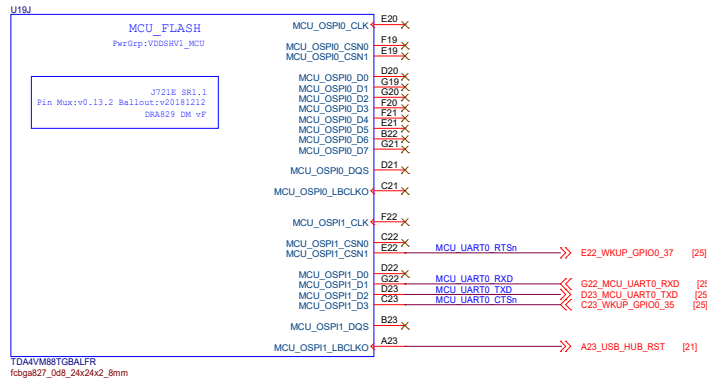


UFS Interface

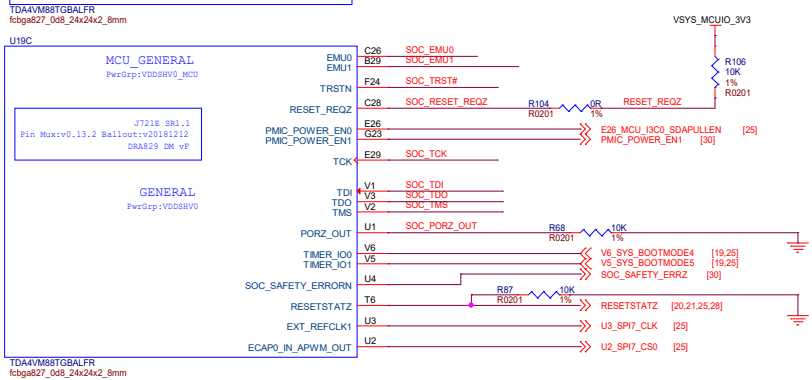
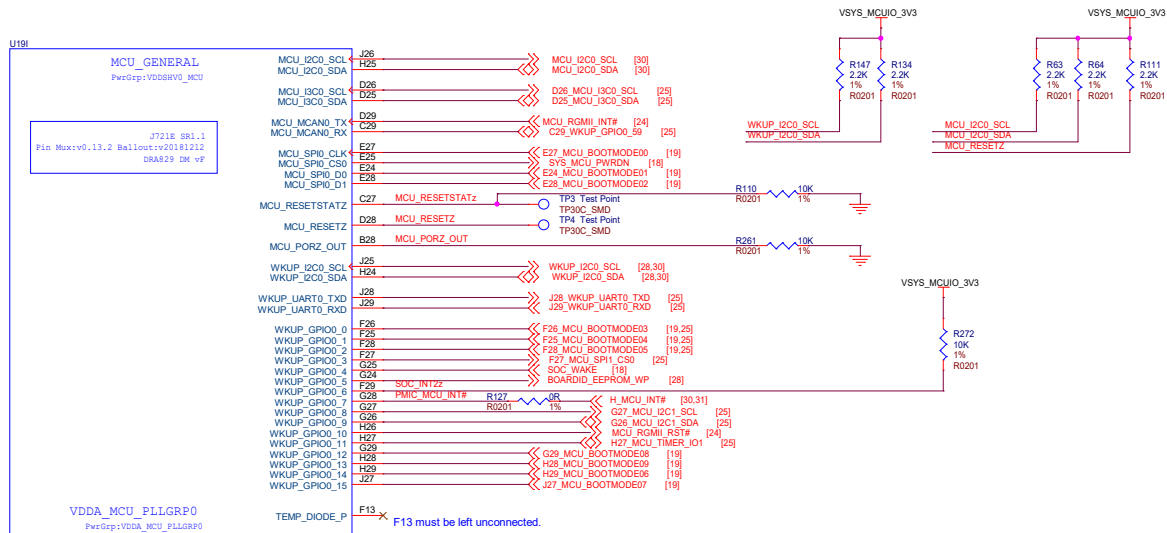




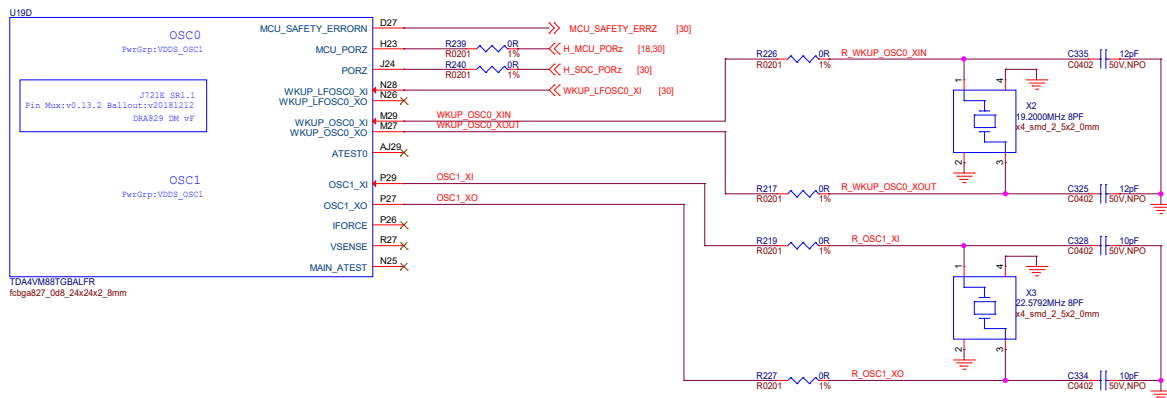
MCU OSPI



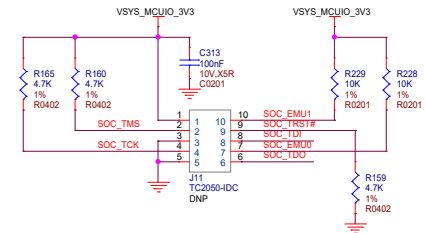
MCU & MAIN GENERAL IO, OSC CLKS



OSC

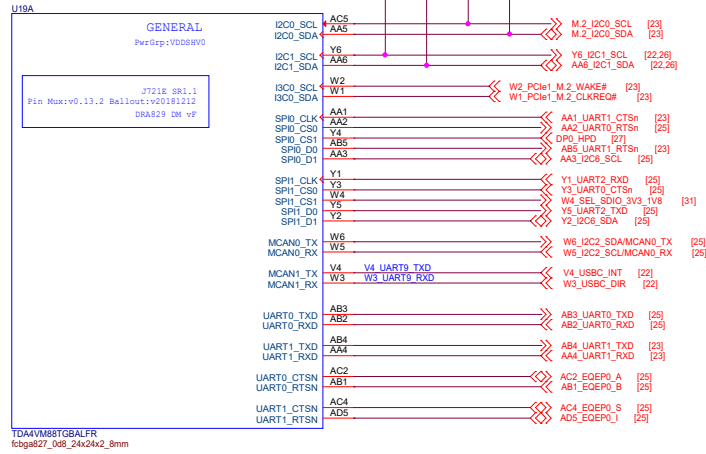


Tag-Connect

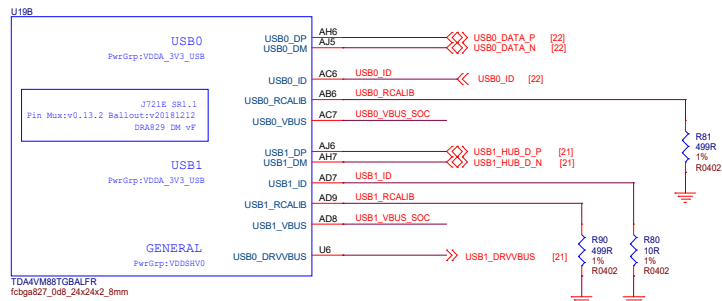


CLKS

GENERAL



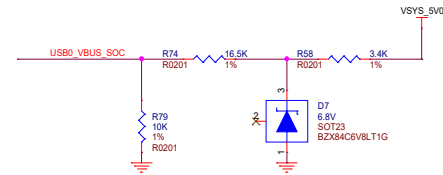
USB



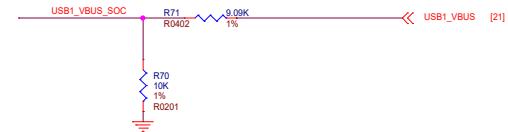
USB1_ID Pulled low. J7 SoC in Host Mode.

USB VBUS Resistor divider circuit

Note: Recommended VBUS circuit for USB connector. Supports 5V VBUS

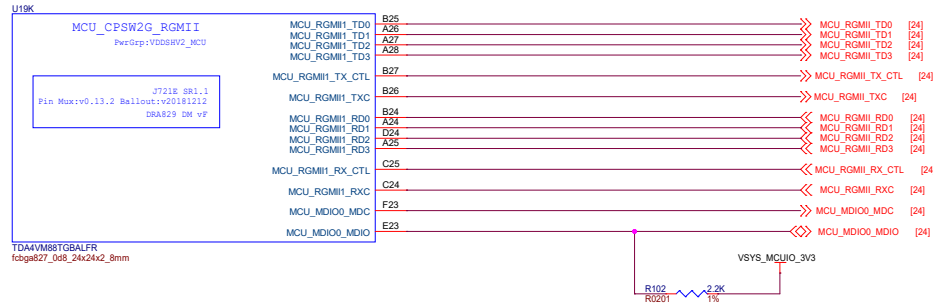


Note: Recommended VBUS circuit for embedded Hub

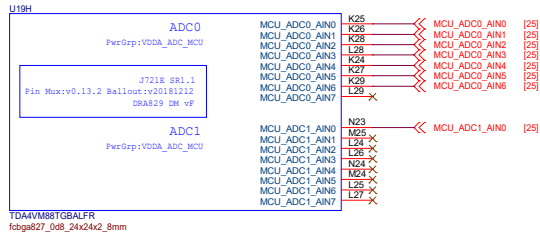


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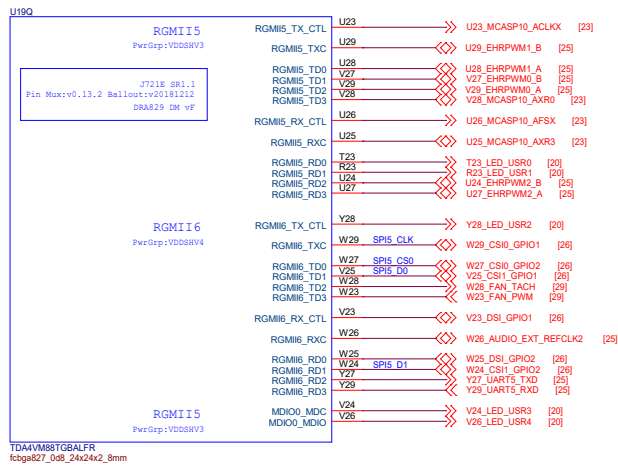
MCU_RGMII



MCU ADCs

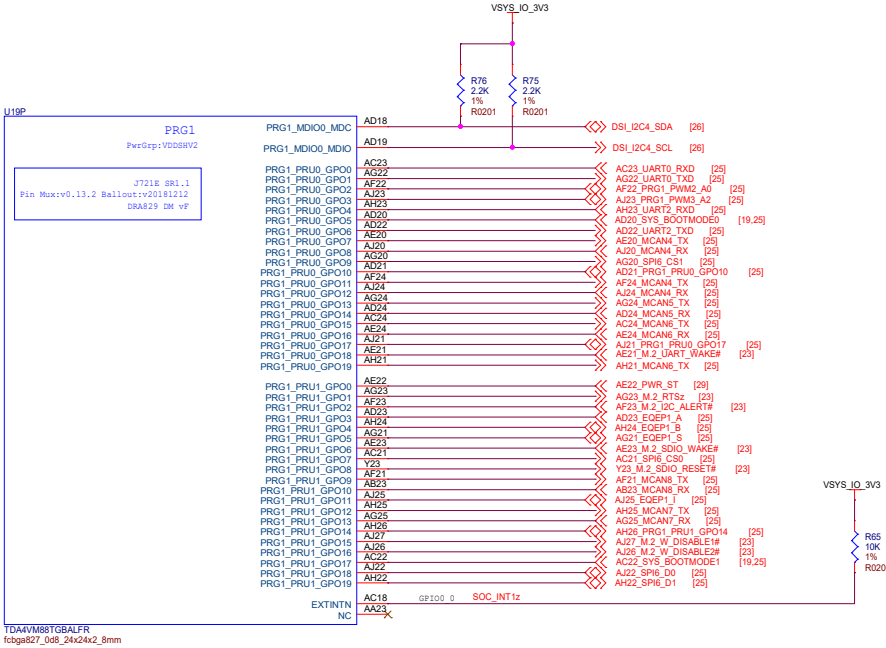
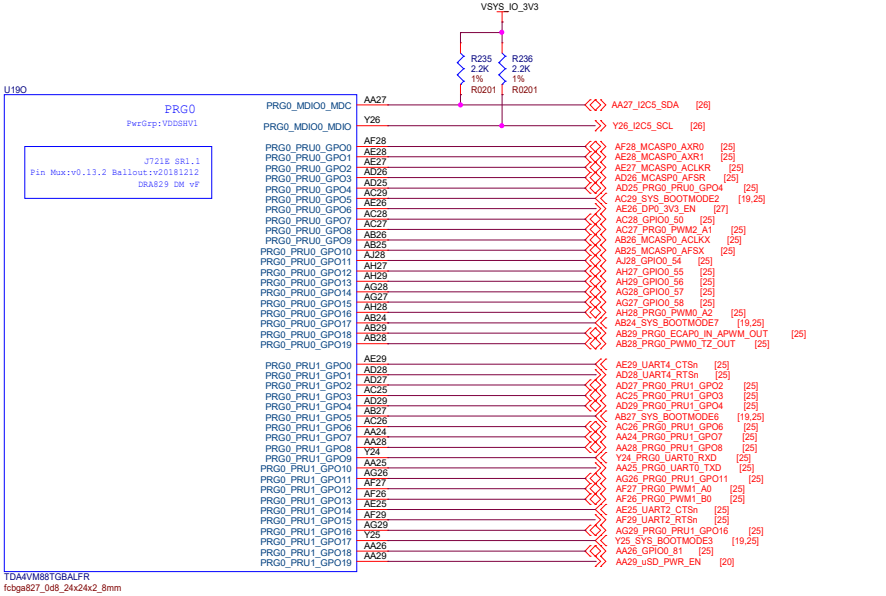


MAIN RGMII

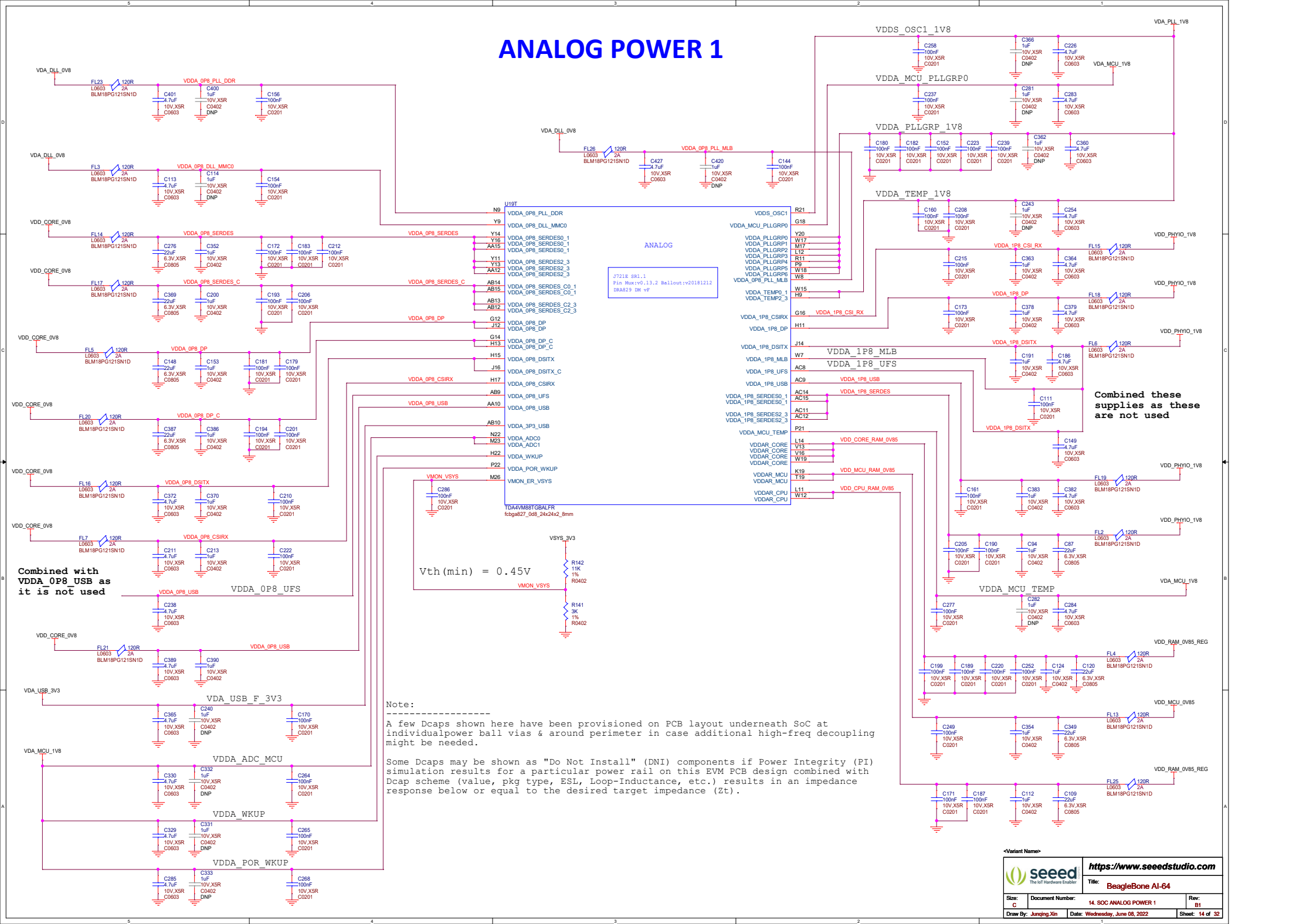


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PRG0 & PRG1

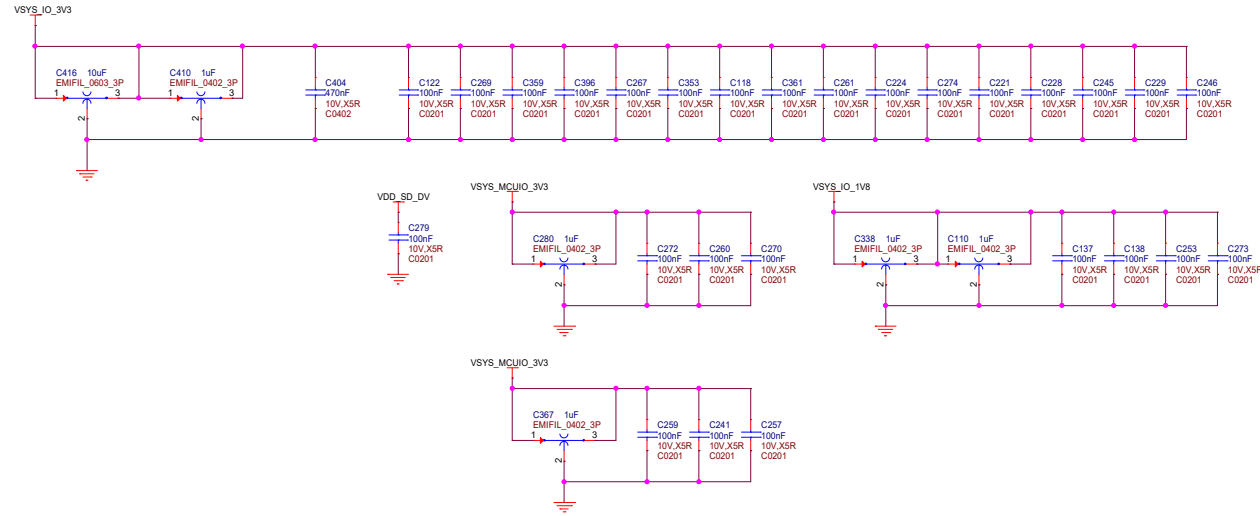
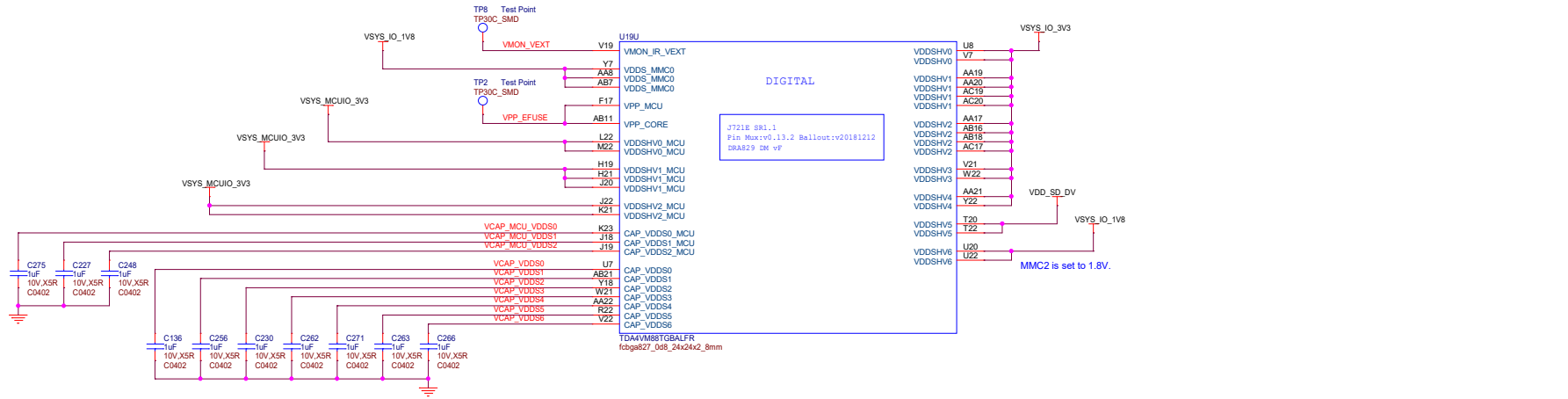


ANALOG POWER 1



DIGITAL POWER 2

Review Note:
MMCQ(eMMC), VDDSD_MMCQ=1.8V Only !!!



Note:

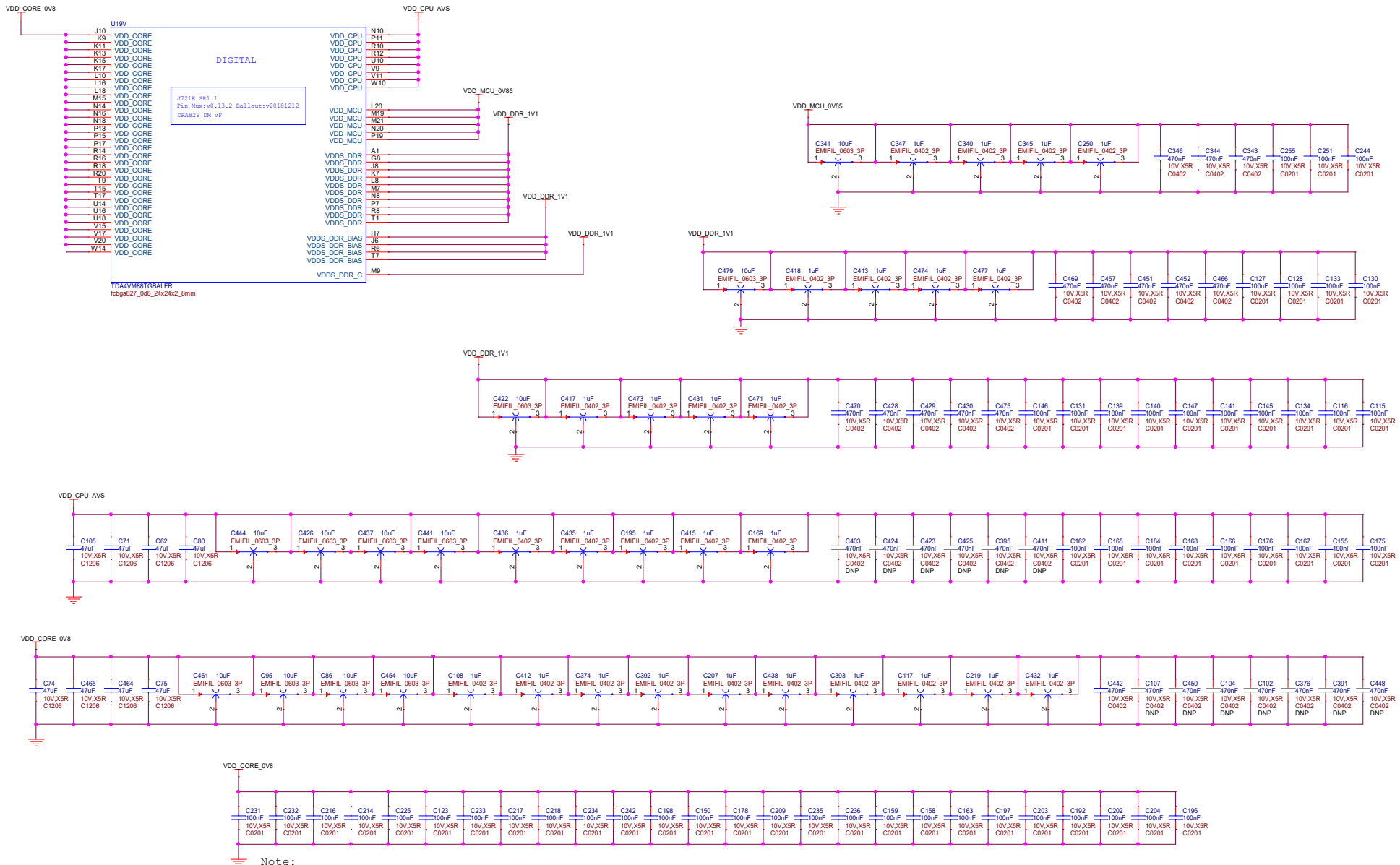
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Z_t).

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Document Number: 15. SOC DIGITAL POWER 2		Rev: B1	
Draw By: Junjing.Xin		Date: Wednesday, June 08, 2022	
		Sheet: 15 of 32	

DIGITAL POWER 3

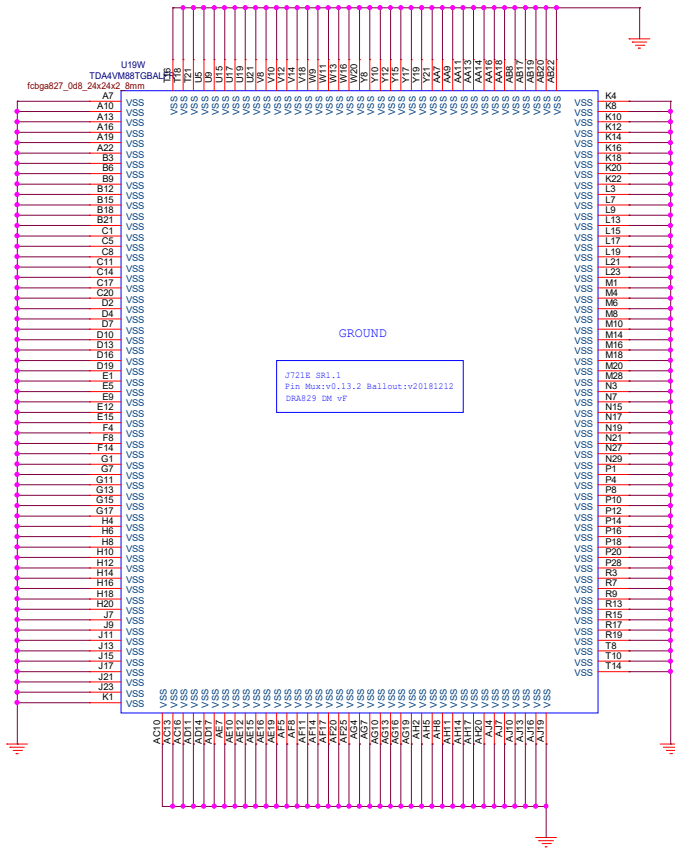


Note:

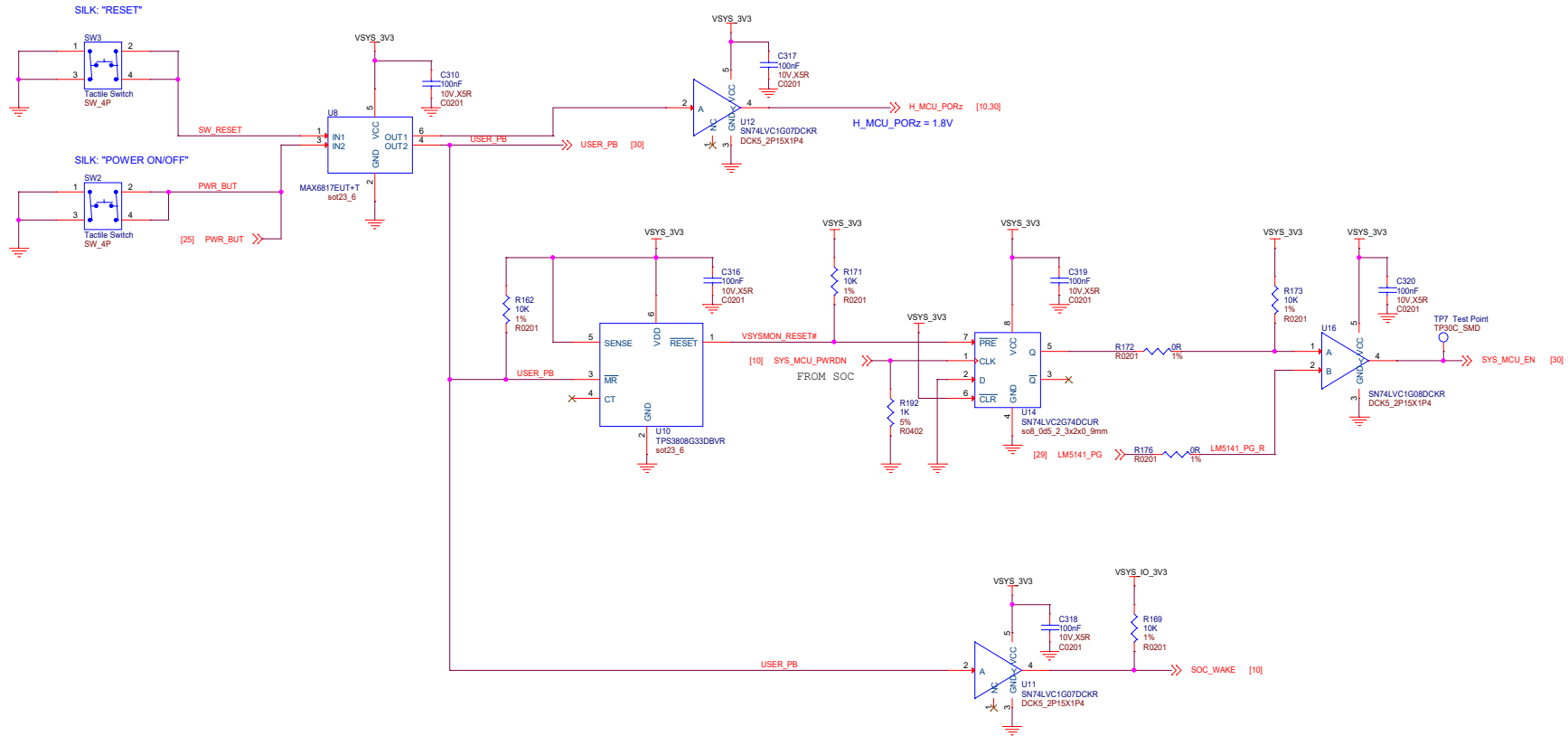
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

SOC GROUND

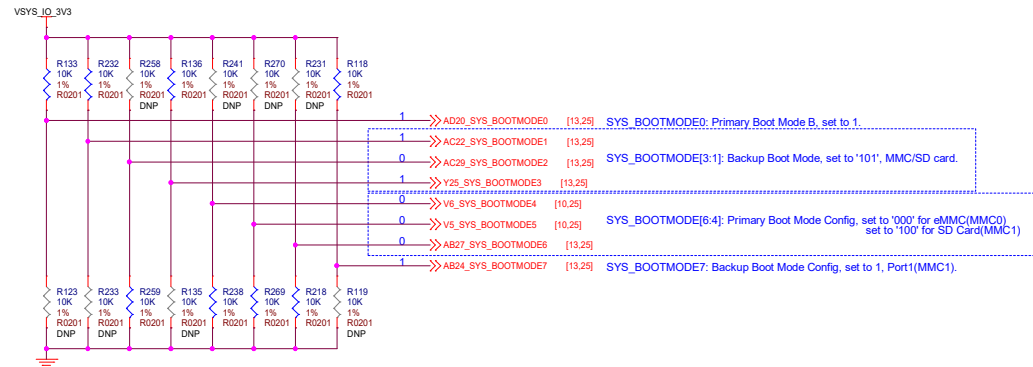
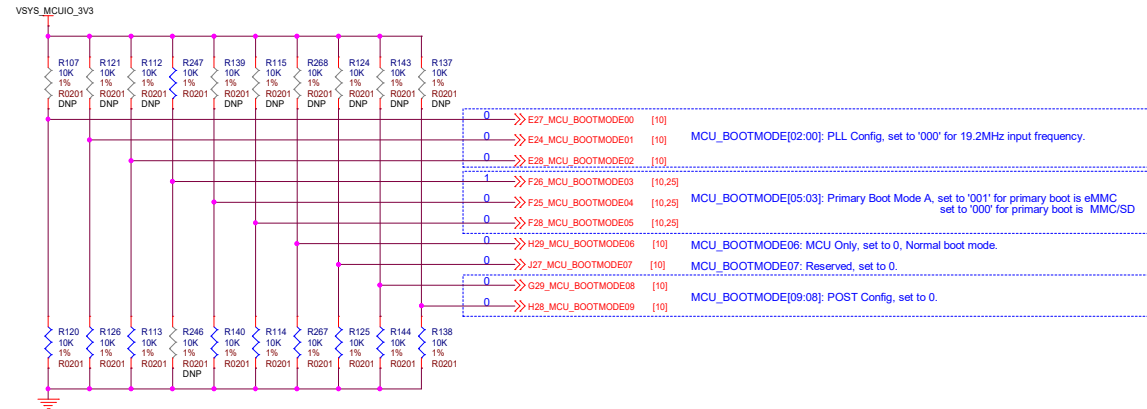


RESET, POWER ON/OFF BUTTONs

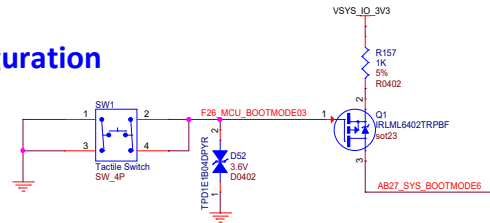


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Draw By: Junjing.Xin		Date: Wednesday, June 08, 2022	
		Sheet: 18 of 32	



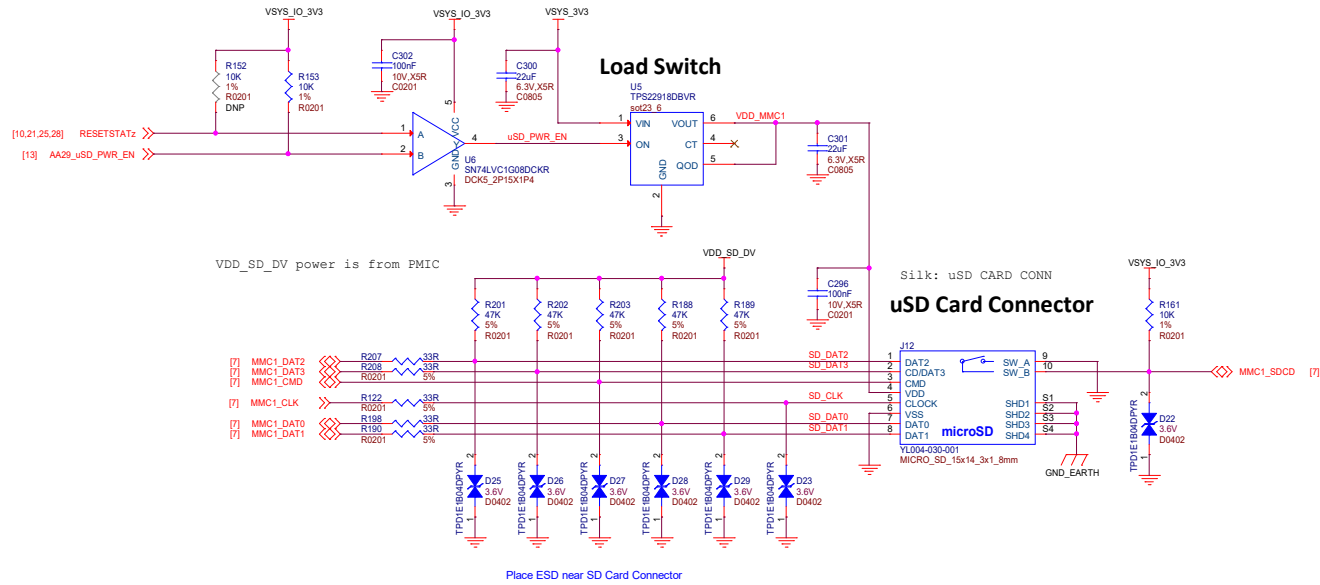
Boot Mode Configuration



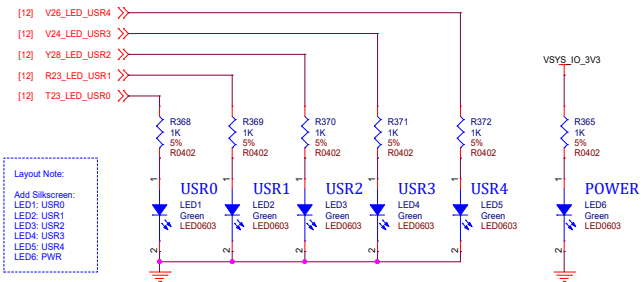
Push-button SW1	Primary Boot Mode	Backup Boot Mode	MCU_BOOTMODE05	MCU_BOOTMODE04	MCU_BOOTMODE03	SYS_BOOTMODE6	SYS_BOOTMODE5	SYS_BOOTMODE4
Open	eMMC(MMC0)	SD Card(MMC1)	0	0	1	0 (Port 0)	0 (8-bit)	0 (1.8V)
Closed	SD Card(MMC1)	SD Card(MMC1)	0	0	0	1 (Port 1)	0 (4-bit)	0 (Filesystem mode)

Primary boot with BOOT normal-open push-button selecting eMMC port 0 (open) or MMC/SD port 1 (closed).

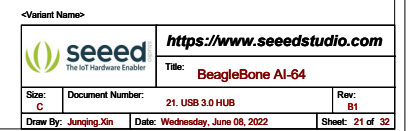
Micro SD CARD INTERFACE



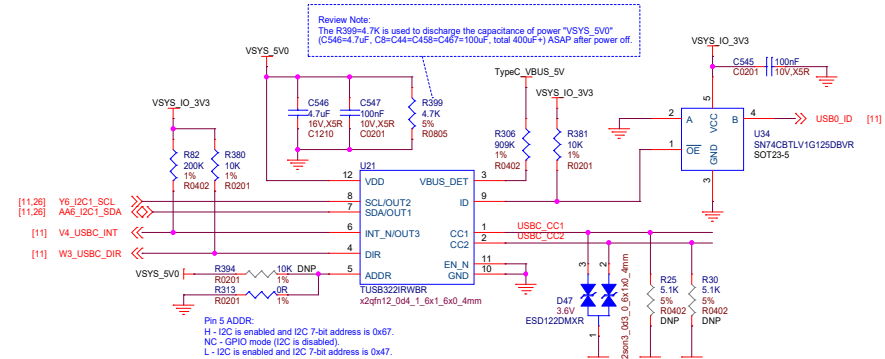
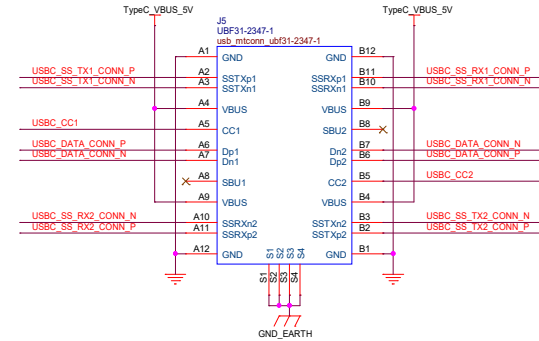
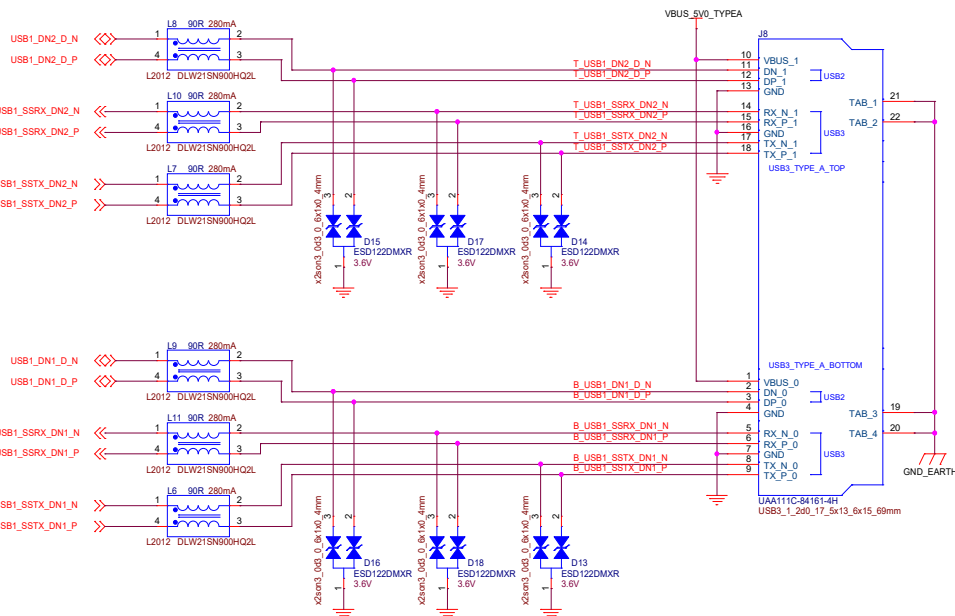
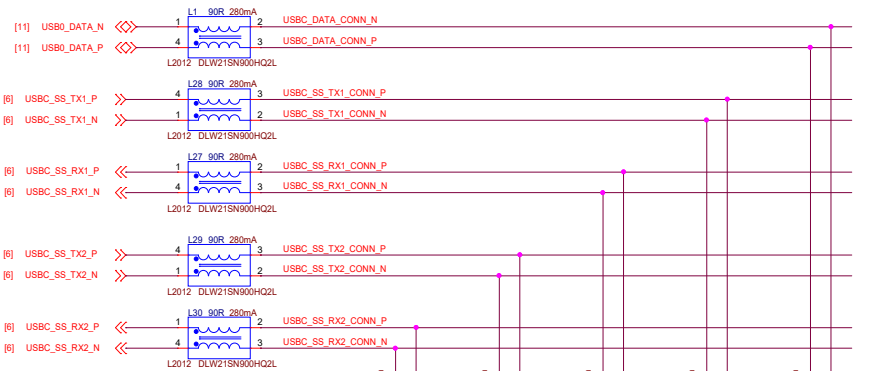
LEDs



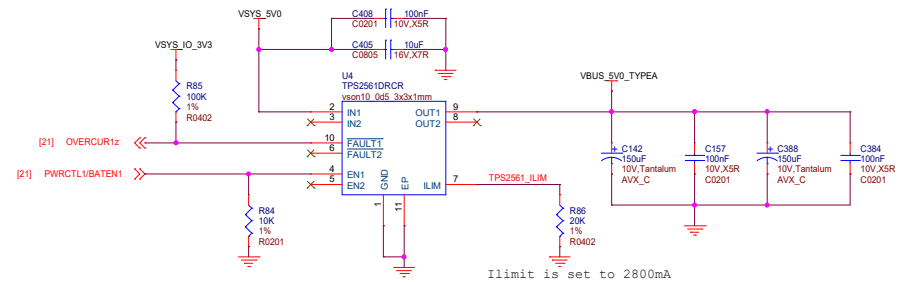
MIN=0.99V, TYP=1.1V, MAX=1.26V
3.0 host / 2 SS Devices in U0 and 2 HS Devices: 554mA



TYPE-C USB 3.0 Sink Application (UFP) Default



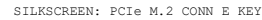
USB 3.0 DUAL TYPE-A



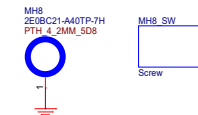
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		Sheet: 22 of 32	

Key E

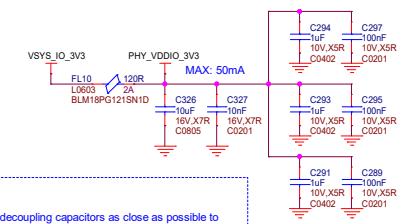
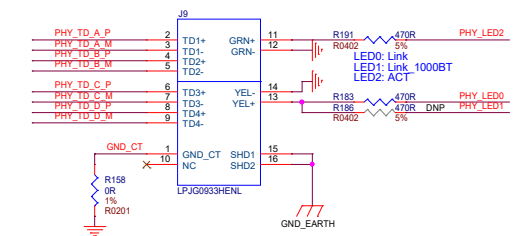
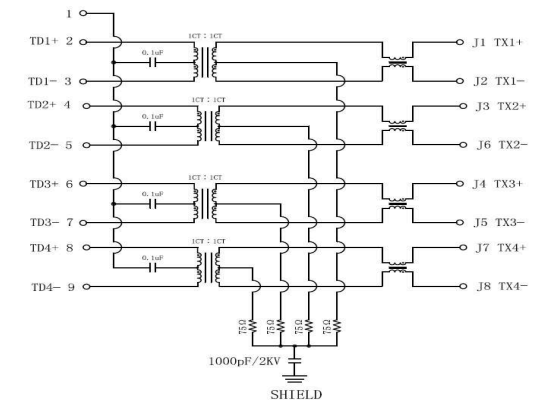
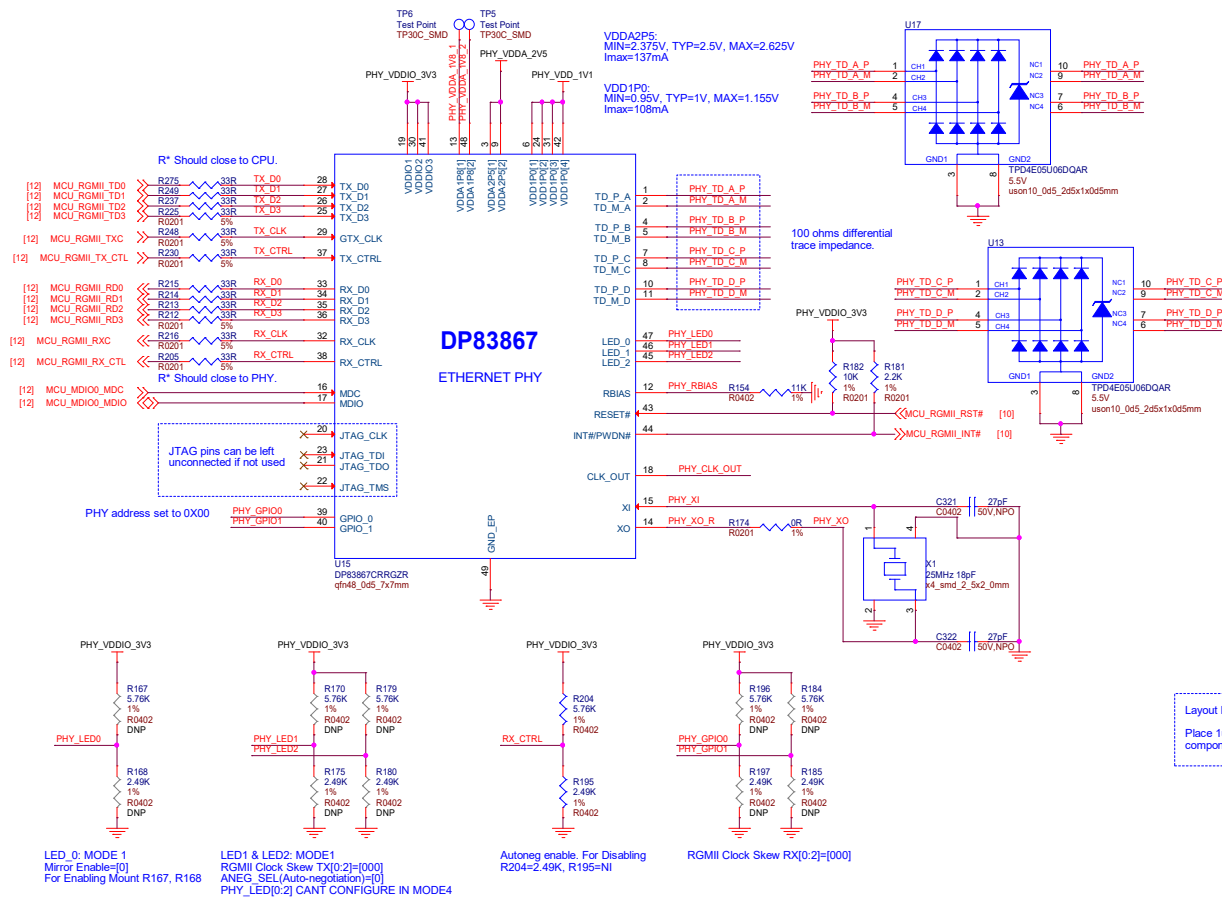


3.3V To 1V8 Level translator



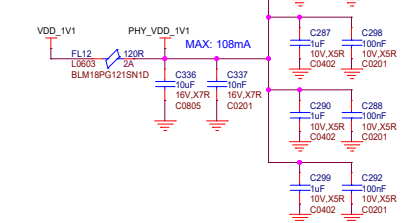
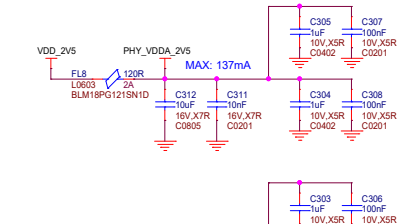
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Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022	Sheet: 23 of 32

GB ETHERNET



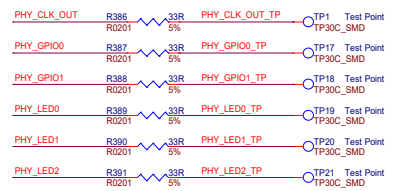
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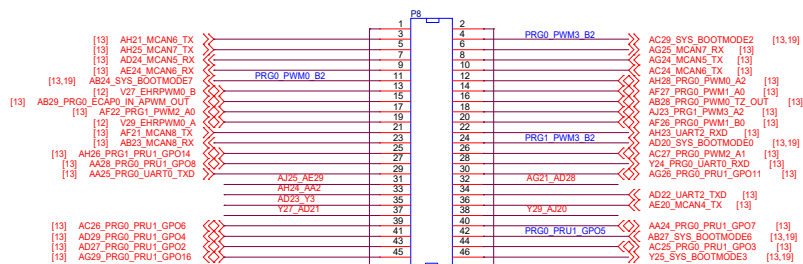
Place 1uF and 0.1uF decoupling capacitors as close as possible to component VDD pins, placing the 0.1uF capacitor closest to the pin.



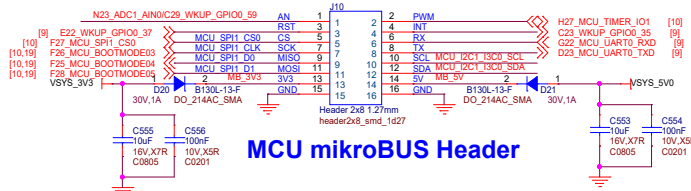
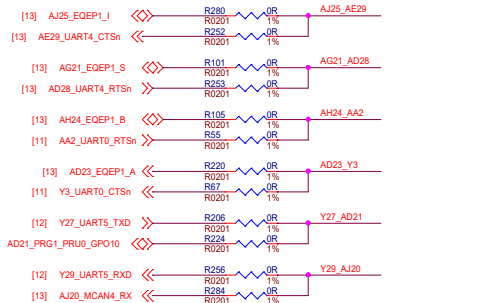
Review Note:

These test points are used for TI testing only!

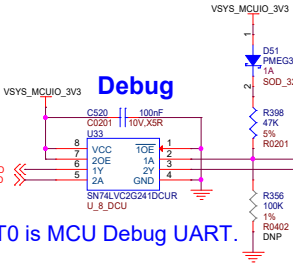
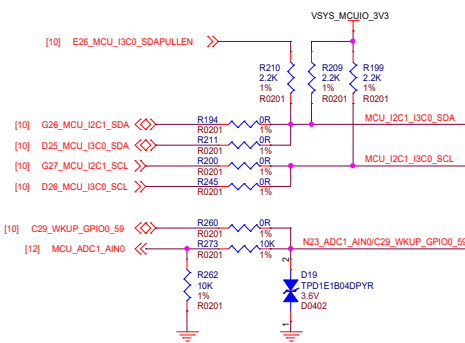




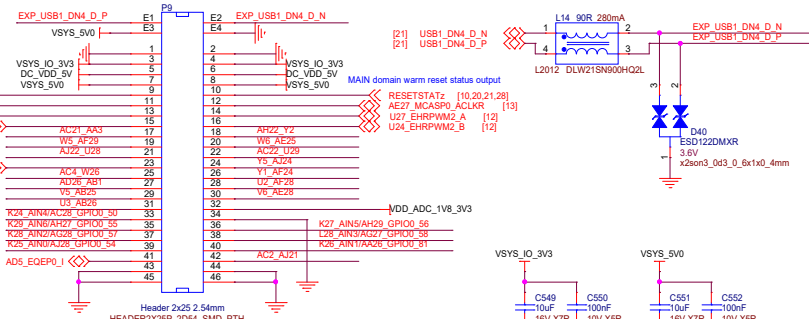
EXPANSION HEADER P8



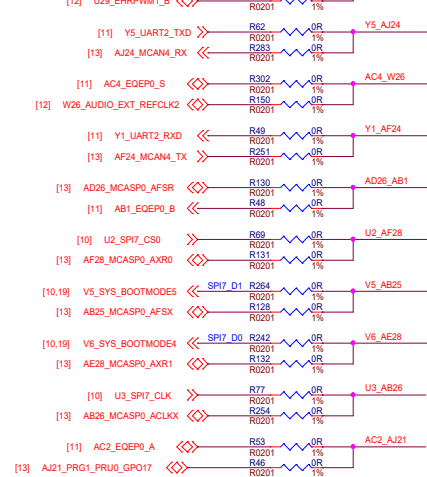
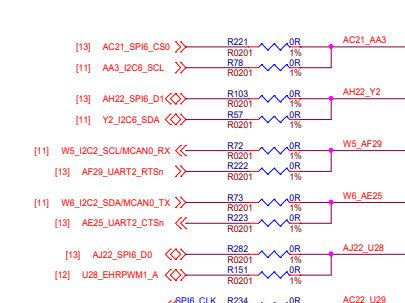
MCU mikroBUS Header



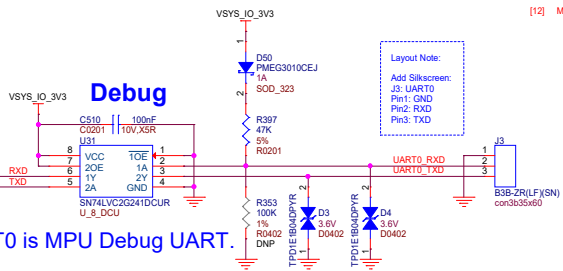
WKUP_UART0 is MCU Debug UART.



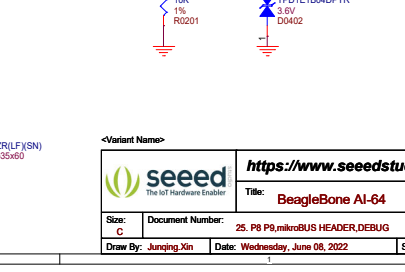
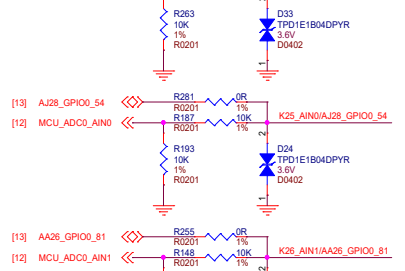
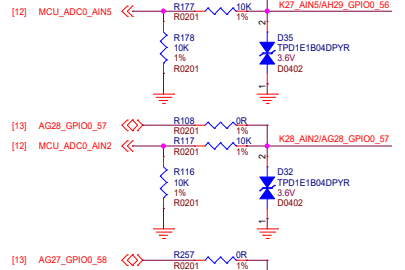
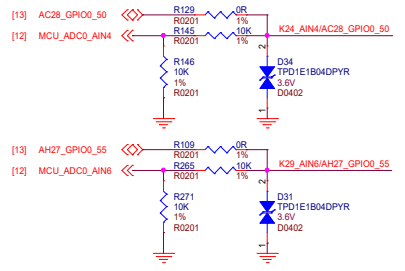
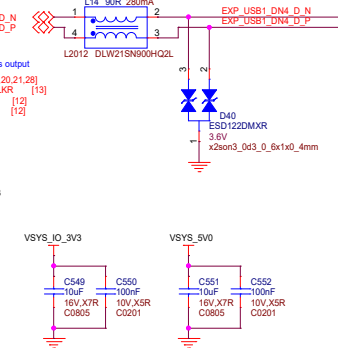
EXPANSION HEADER P9



Note: AB3_SPI7_CS1 is replaced by AJ21_PRG1_PRU0_GPIO17 (PRG1_PWM0_B2).

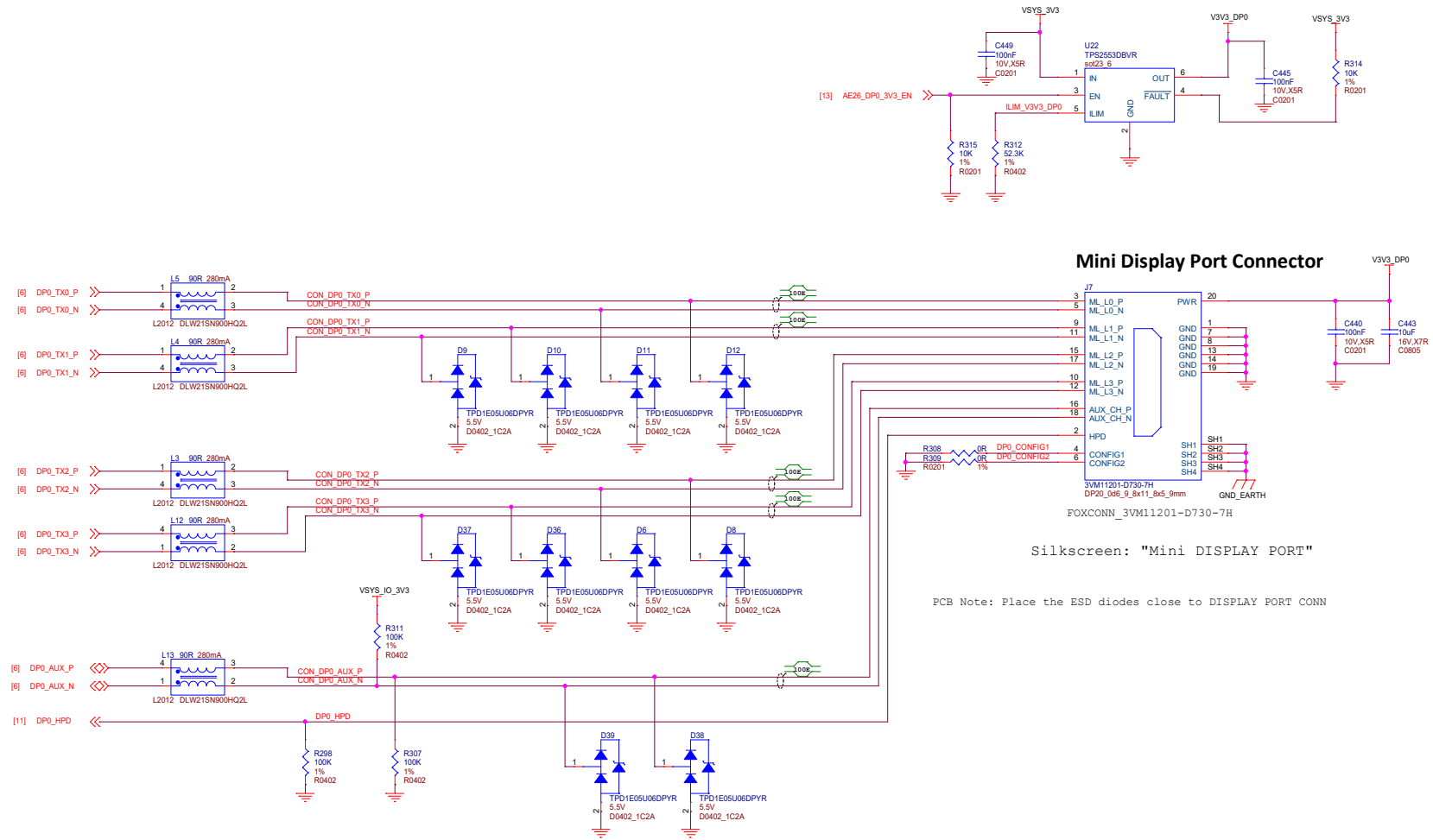


UART0 is MPU Debug UART.



		https://www.seeedstudio.com	
Variant Name		Title	
Size		Document Number	
Draw By		Date	
Rev		Sheet	

Mini DISPLAY PORT INTERFACE



USB Type C



POWER SUPPLY

3.3V GENERATION



TI WEBENCH Simulation Inputs:
Vin (min) = 4.5V Vin (max) = 5.5V
Vout1 = 3.3V@8A
Ta = 25 deg

EVM's 3-Phase DUAL PMIC Power Distribution Network (PDN)

(3-Phase Buck supplying VDD_CPU)

"PCB Notes:

For multi-phase Buck converter configs, route remote sense feedback as follows:

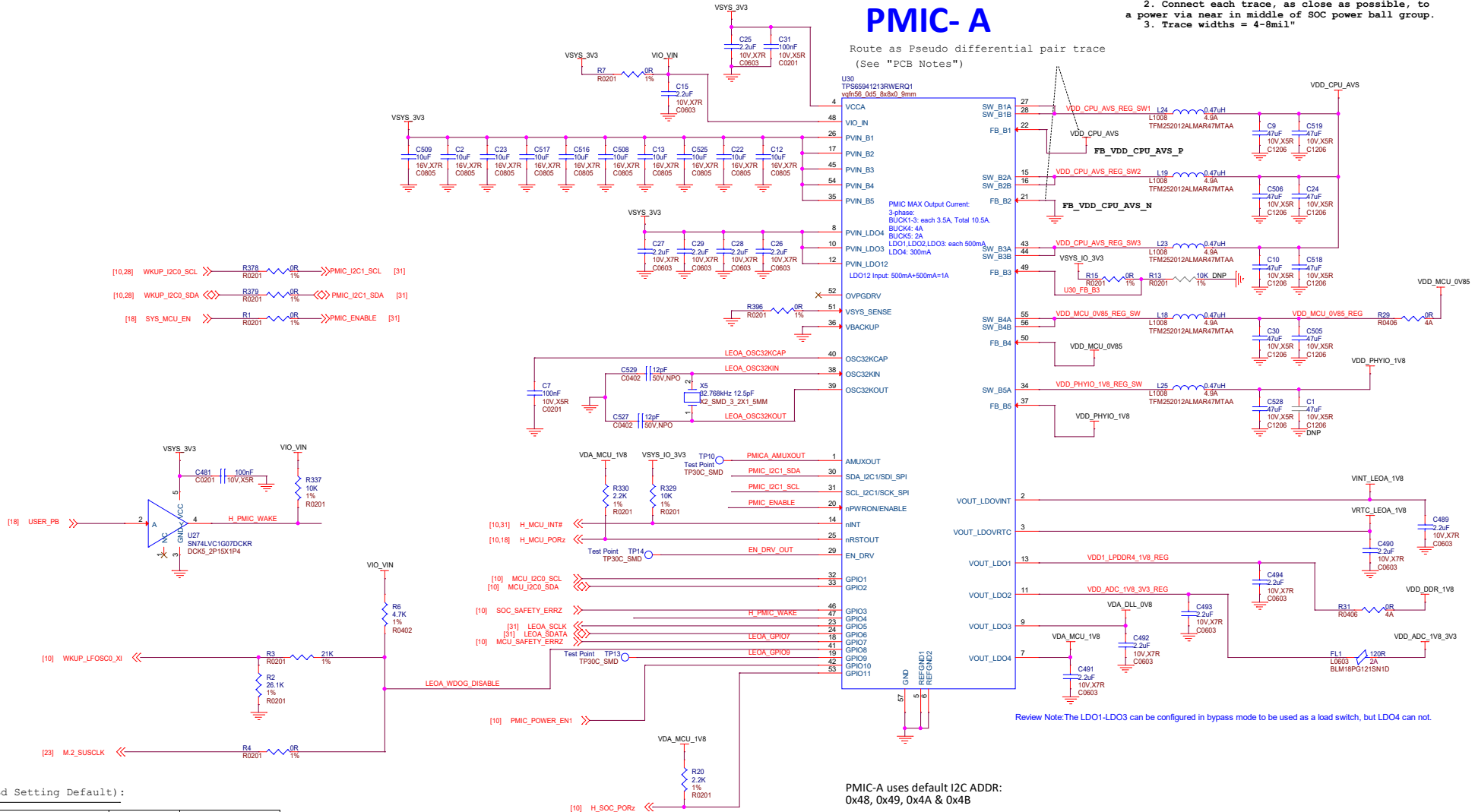
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:

1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

PMIC- A

Route as Pseudo differential pair trace
(See "PCB Notes")



(EVM Bd Setting Default):

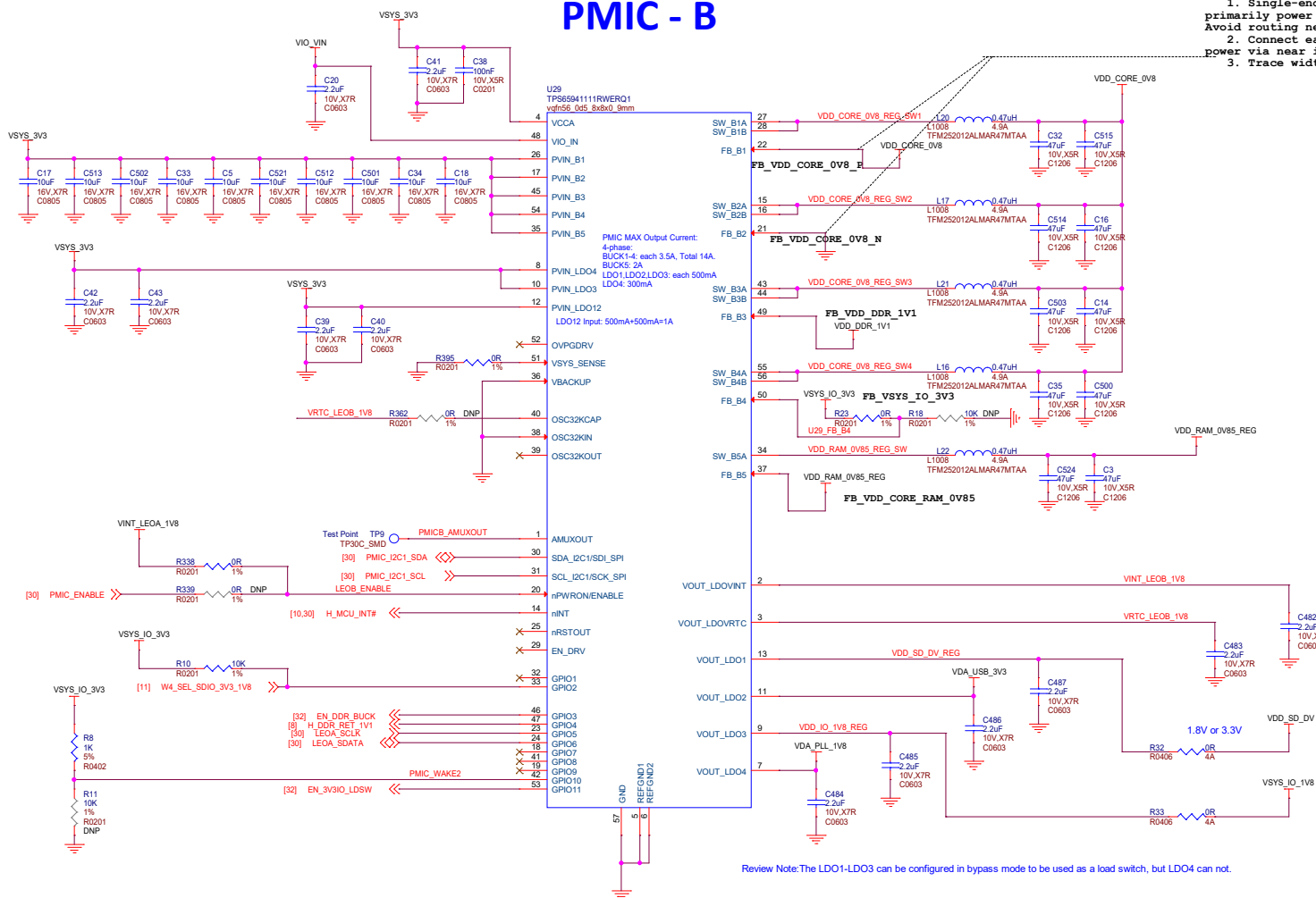
LEOA_WDOG_DISABLE	PD (Low)	Enable WDOG
	PU (High)	Disable WDOG

PMIC-A uses default I2C ADDR:
0x48, 0x49, 0x4A & 0x4B

<Variant Name>

 The IoT Hardware Enabler		https://www.seeedstudio.com	
Title:		BeagleBone AI-64	
Size:	Document Number:	30. PMIC A	Rev:
C			B1
Draw By:	Junjing.Xin	Date:	Wednesday, June 08, 2022
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PMIC - B



PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:

1. Pseudo differential pair traces on same layer & net to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd via or across Decap in middle of SOC power ball group.

Trace widths = 4-8mil & separation distance = 8-50mil. Try to keep traces near each other as best as possible while

For single phase Buck converters, route remote sense feedback as follows:

1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

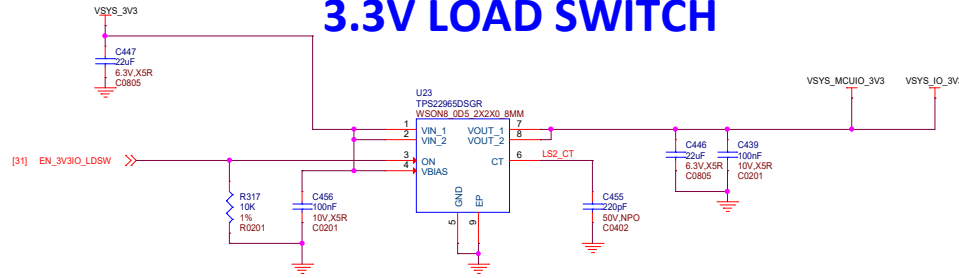
Review Note: The LDO1-LDO3 can be configured in bypass mode to be used as a load switch, but LDO4 can not

PCB1
BeagleBone AI-64_PCB

Label 1
DC 5V Label

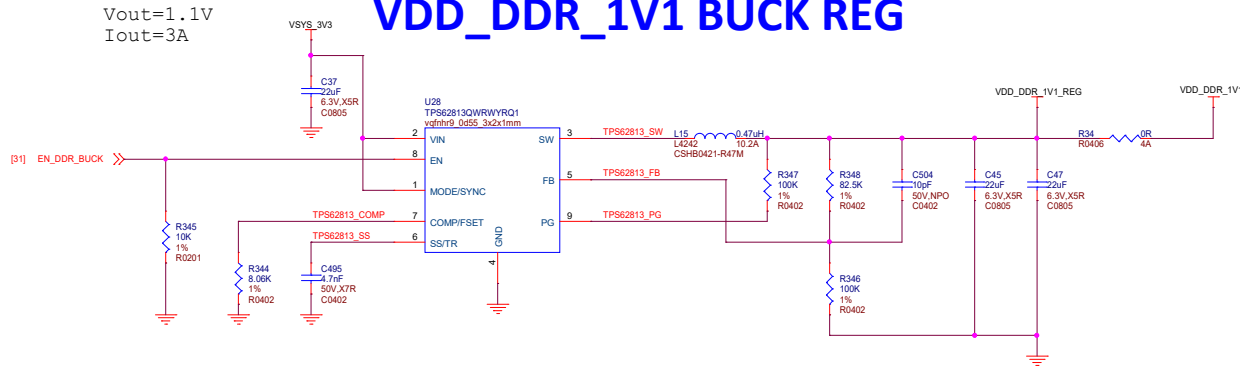
Label 2
SN Label

3.3V LOAD SWITCH



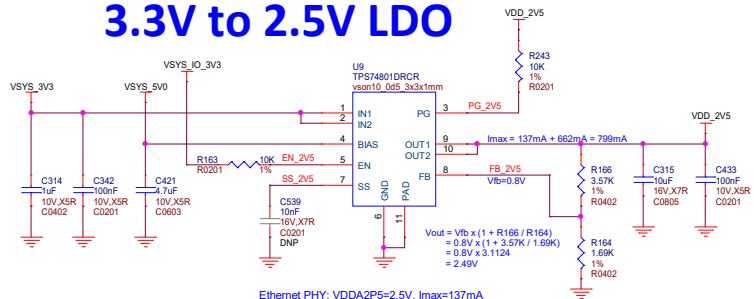
VDD_DDR_1V1 BUCK REG

Vout=1.1V
Iout=3A



ETHERNET POWER

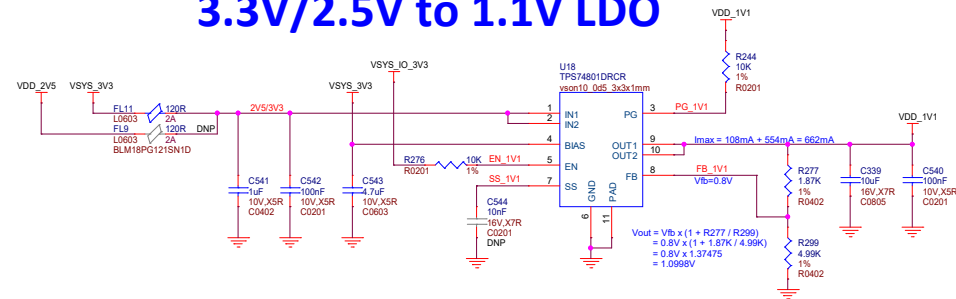
3.3V to 2.5V LDO



Ethernet PHY: VDDA2P5=2.5V, Imax=137mA
LDO U18 Power In=2.5V, Imax=662mA
Total: Imax= 137mA + 662mA = 799mA
Power Consumption: (3.3V-2.5V) * 0.799A = 0.6392W
Thermal Junction-to-ambient: 0.6392W * 44.2°C/W=28.25°C

USB3.0 HUB & ETHERNET POWER

3.3V/2.5V to 1.1V LDO



Ethernet PHY: VDD1P0=1.1V, Imax=108mA
USB3.0 HUB: VDD=1.1V, Imax=554mA
Total: Imax = 108mA + 554mA = 662mA
Option 1: VIN_2V5/3V3 = 3.3V
Power Consumption: (3.3V-1.1V) * 0.662A = 1.4564W
Thermal Junction-to-ambient: 1.4564W * 44.2°C/W=64.37°C
Option 2: VIN_2V5/3V3 = 2.5V
Power Consumption: (2.5V-1.1V) * 0.662A = 0.9268W
Thermal Junction-to-ambient: 0.9268W * 44.2°C/W=40.96°C