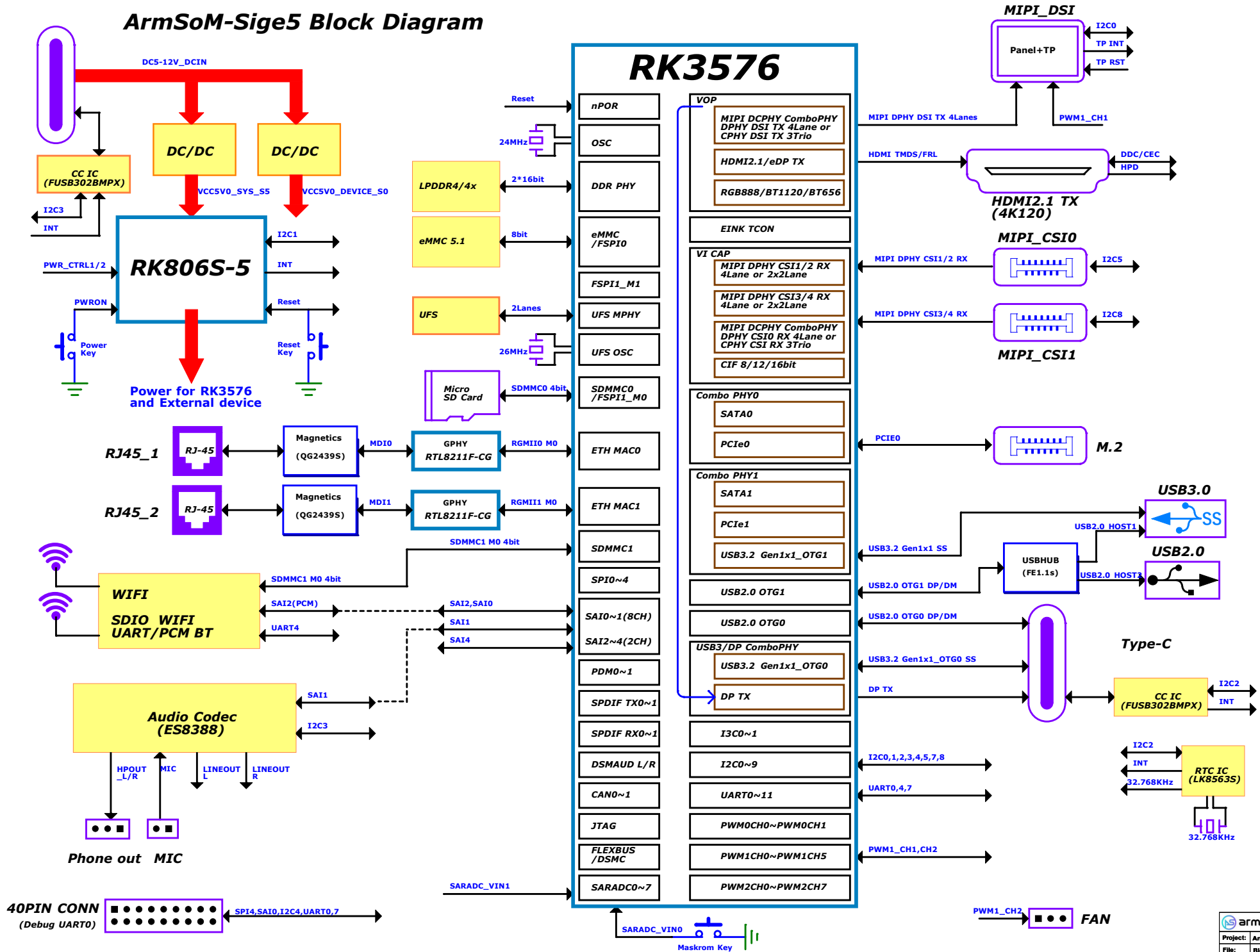
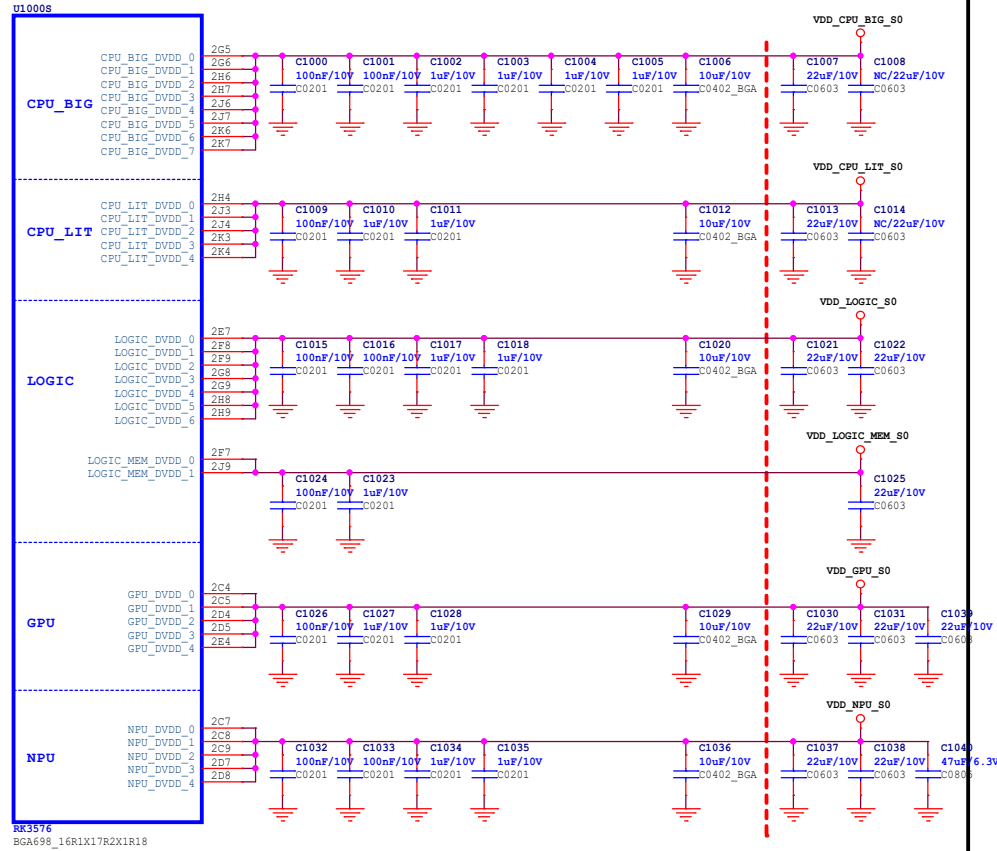


ArmSoM-Sige5 Block Diagram

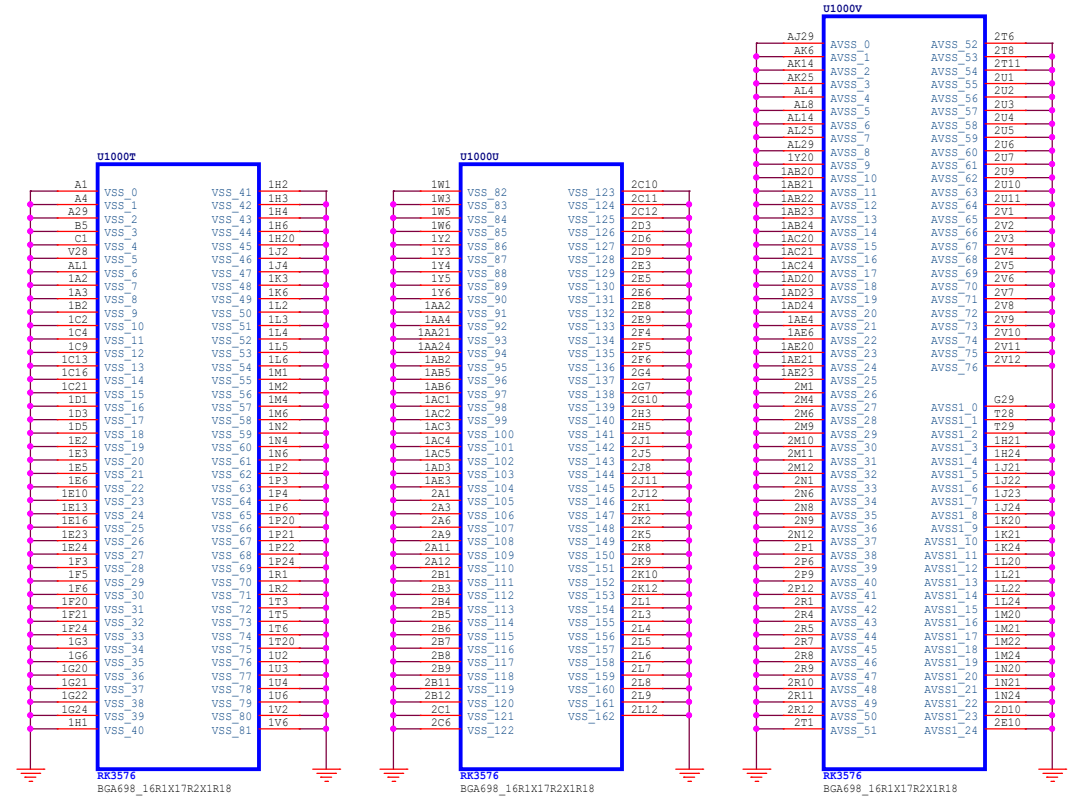


RK3576_S (Power)

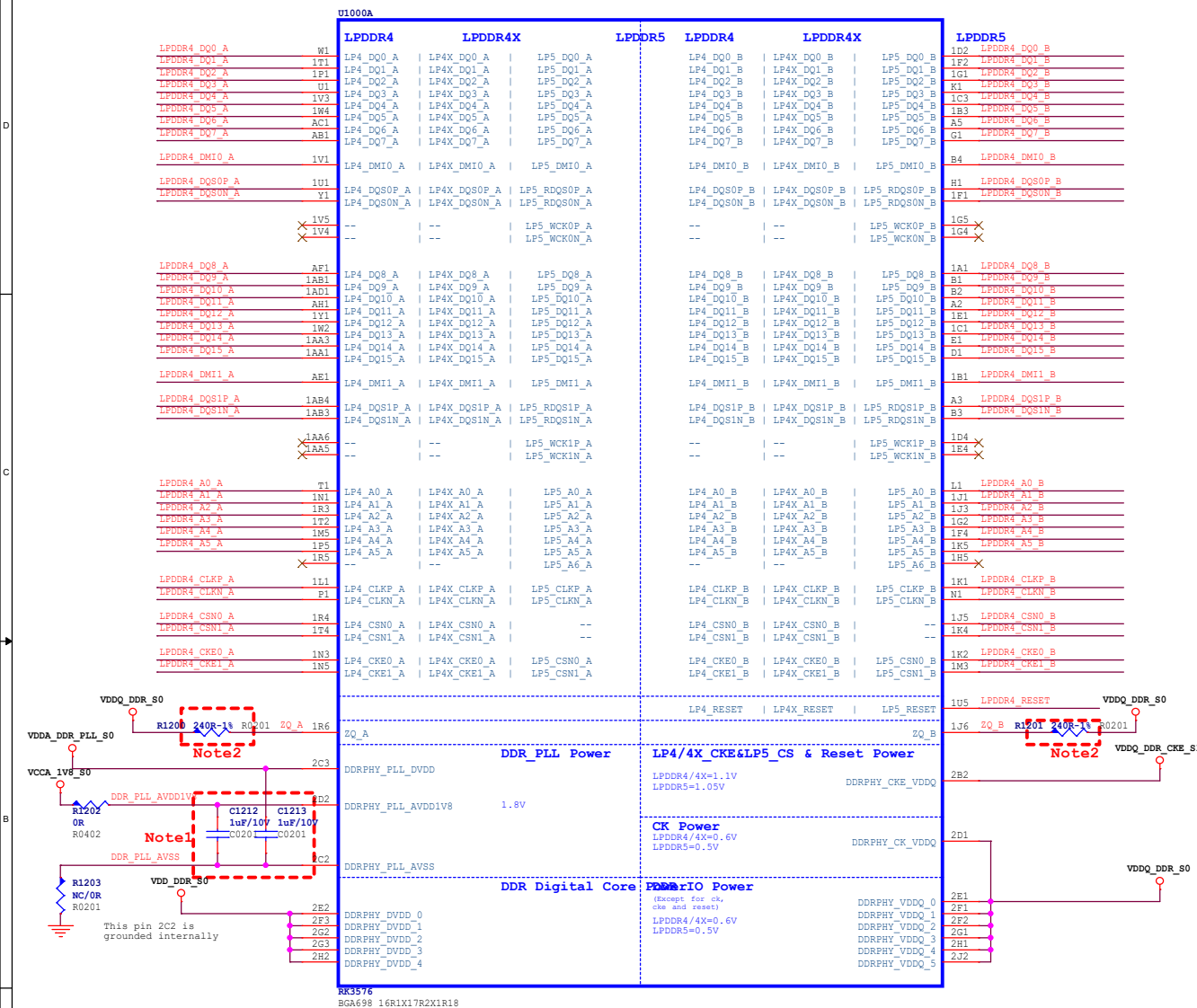
RK3576_T/U/V (GND)



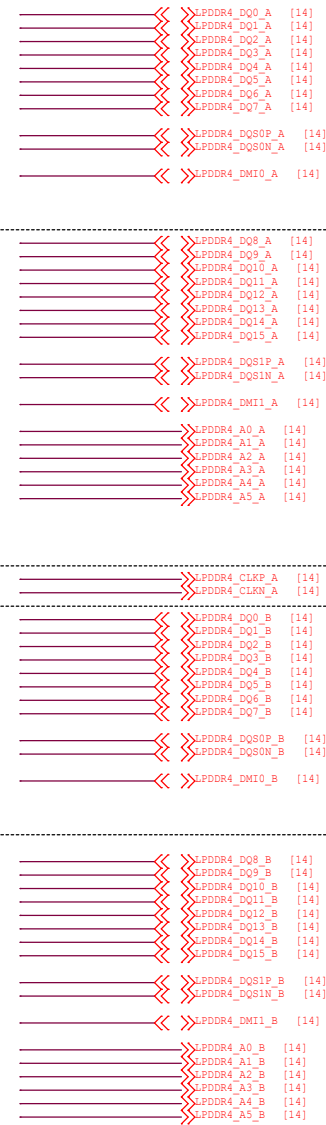
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



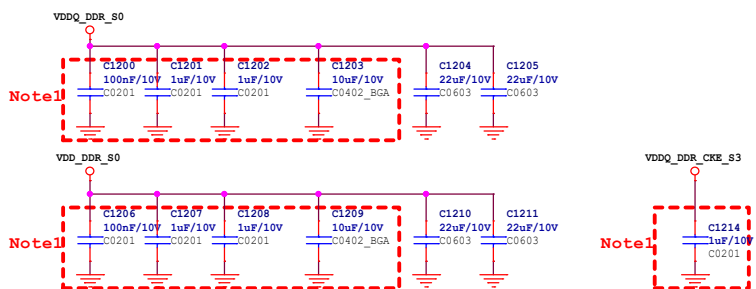
RK3576 A (DDRPHY)



LPDDR4 Signal



DDR FILTER



Note:

- (1) Power Sequence: VDD-VDDQ_CKE-VDDQ
(2) Hold power of DDRPHY_CKE_VDDQ during retention times.

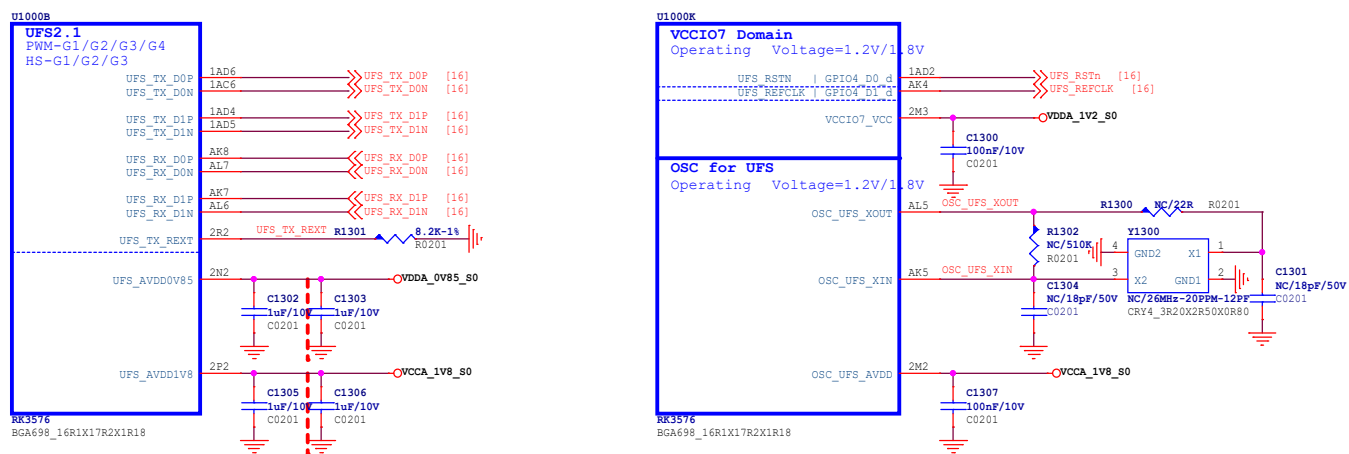
Note1:

Caps in the red line dotted box
should be placed under the U1000 package

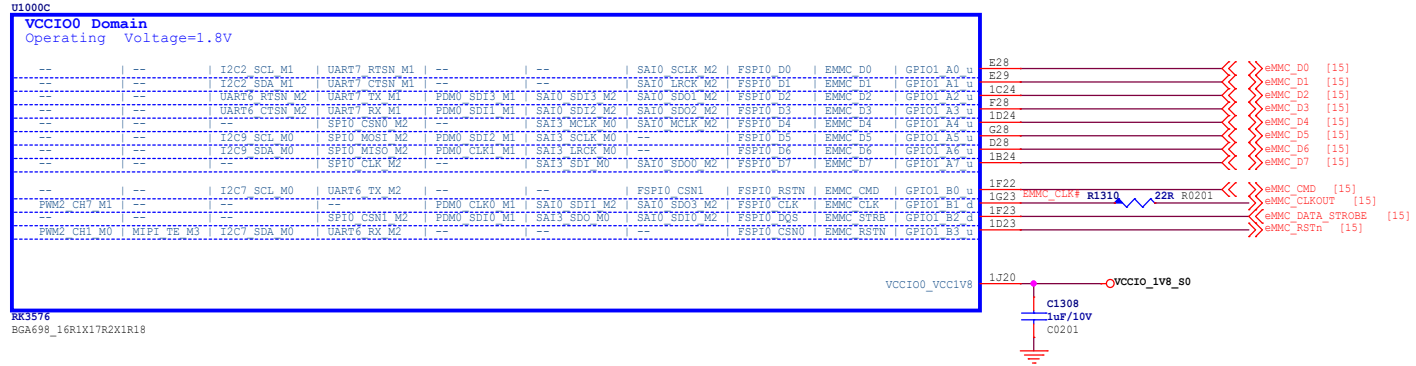
Note2:

Resistors in the red line dotted box
should be placed under the U1000 package

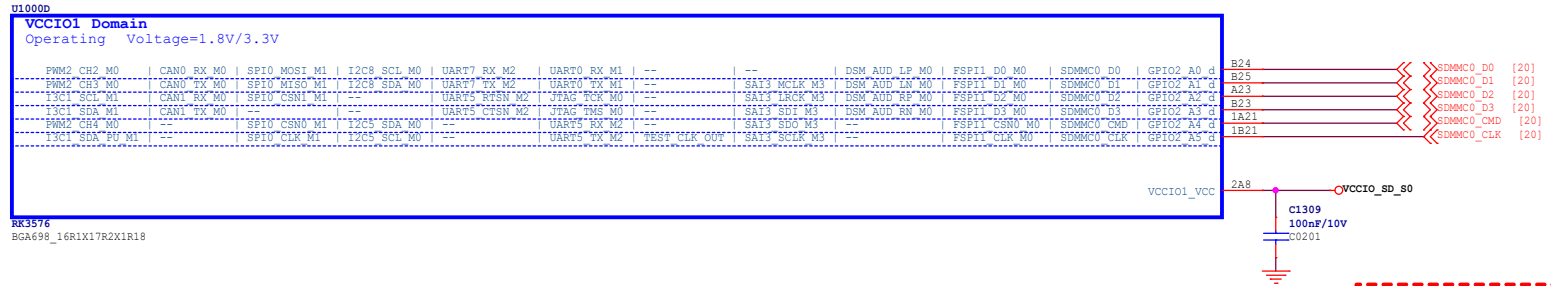
RK3576 B (UFS2.1)



RK3576 C (VCCIO0)



RK3576 D (VCCIO1)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3576 L (USB3/DP)

U1000L

USB3 OTG0/DP1.4 Alt
USB:USB3.2 Gen1x1 OTG0
DP :RBR/HBR/HBR2/HBR3

-- | DP_TX_AUXP
-- | DP_TX_AUXN

USB3_OTG0_SSRX1P | DP_TX_D0P
USB3_OTG0_SSRX1N | DP_TX_D0N

USB3_OTG0_SSTX1P | DP_TX_D1P
USB3_OTG0_SSTX1N | DP_TX_D1N

USB3_OTG0_SSRX2P | DP_TX_D2P
USB3_OTG0_SSRX2N | DP_TX_D2N

USB3_OTG0_SSTX2P | DP_TX_D3P
USB3_OTG0_SSTX2N | DP_TX_D3N

USB3_OTG0_REXT | DP_TX_REXT

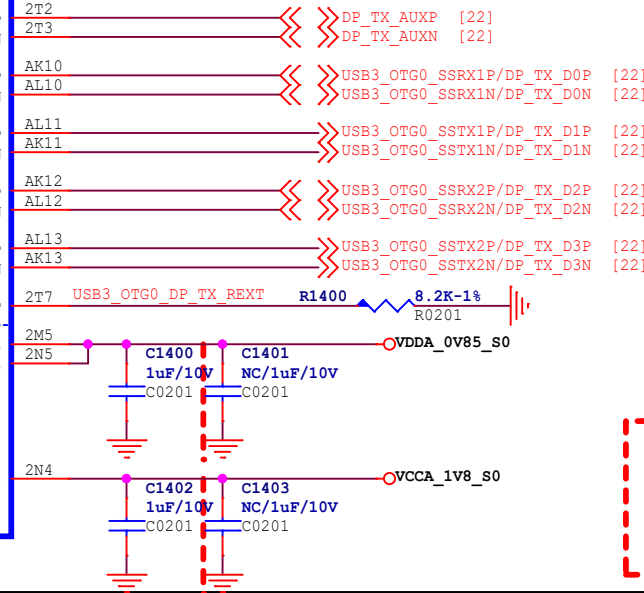
USB3_OTG0_DP_TX_AVDD0V85
USB3_OTG0_DP_TX_DVDD0V85

USB3_OTG0_DP_TX_AVDD1V8

RK3576

BGA698_16R1X17R2X1R18

Support:
Type-C With Displayport Alternate Mode



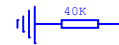
Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

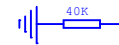
RK3576 M (USB2)

U1000M

USB2 OTG0
OTG/HOST/DEVICE
HS/FS/LS Download Port



USB2 OTG1
OTG/HOST/DEVICE
HS/FS/LS



USB2_OTG0_DP
USB2_OTG0_DM

USB2_OTG0_ID

USB2_OTG0_VBUSDET

USB2_OTG0_REXT

USB2_OTG1_DP
USB2_OTG1_DM

USB2_OTG1_ID

USB2_OTG1_VBUSDET

USB2_OTG1_REXT

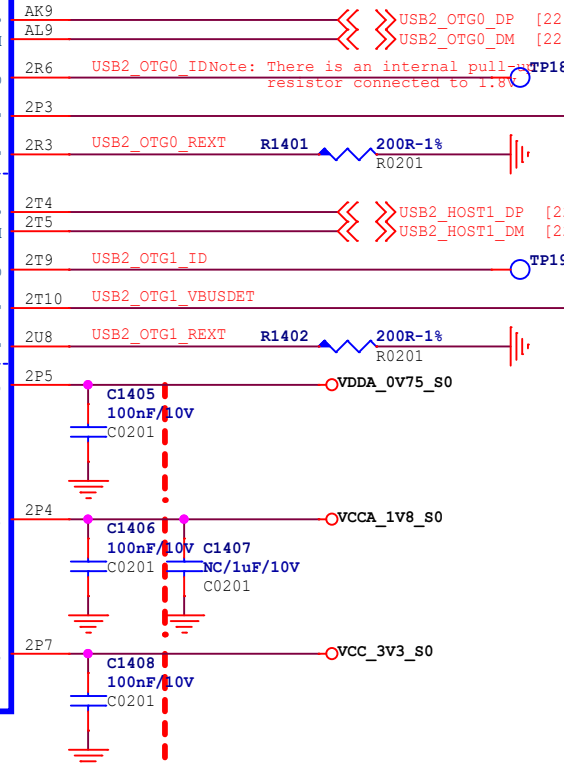
USB2_OTG_DVDD0V75

USB2_OTG_AVDD1V8

USB2_OTG_AVDD3V3

RK3576

BGA698_16R1X17R2X1R18



The USB2 OTG1 function cannot be used, if the PCIe1 or SATA1 function of Combo PHY1 is selected



<https://armsom.org/>

Project: ArmSoM-Sige5

File: RK3576-TypeC/USB

Date: Wednesday, May 22, 2024

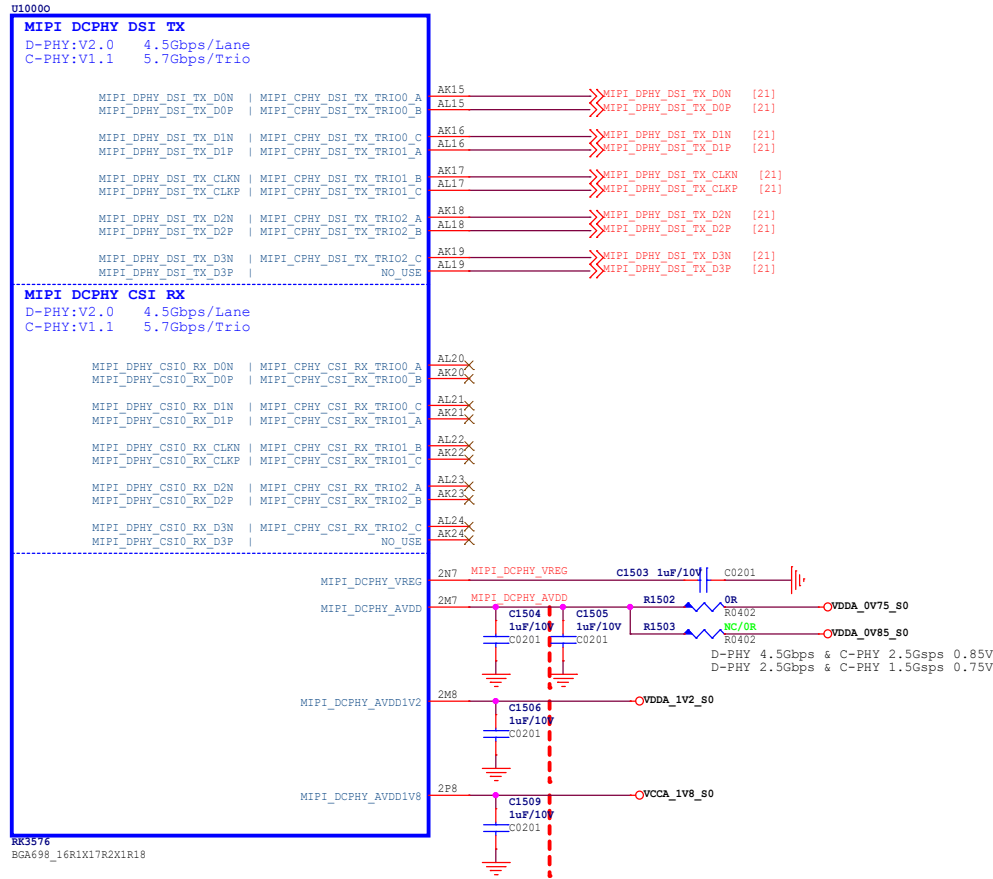
Rev: V1.1

Designed by: Park

Reviewed by: <Checker>

Sheet: 6 of 25

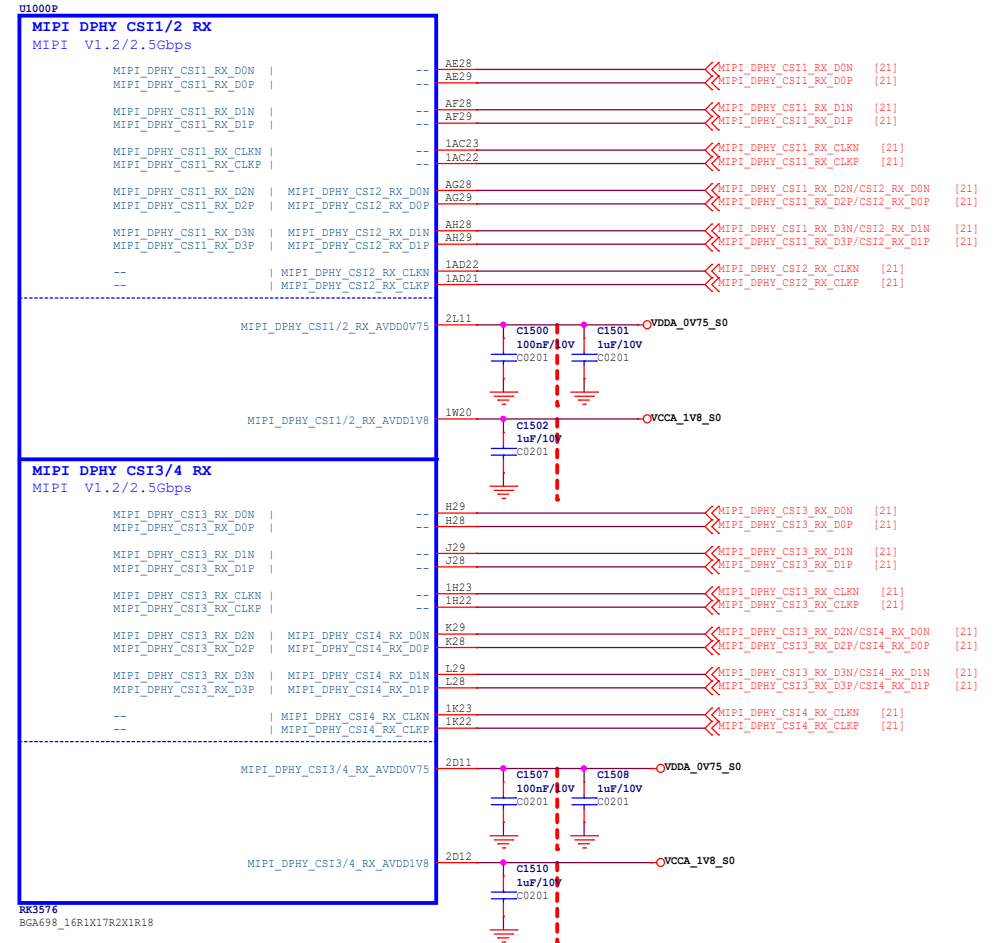
RK3576_O (MIPI DCPHY)



Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3576_P (MIPI DPHY CSI RX)

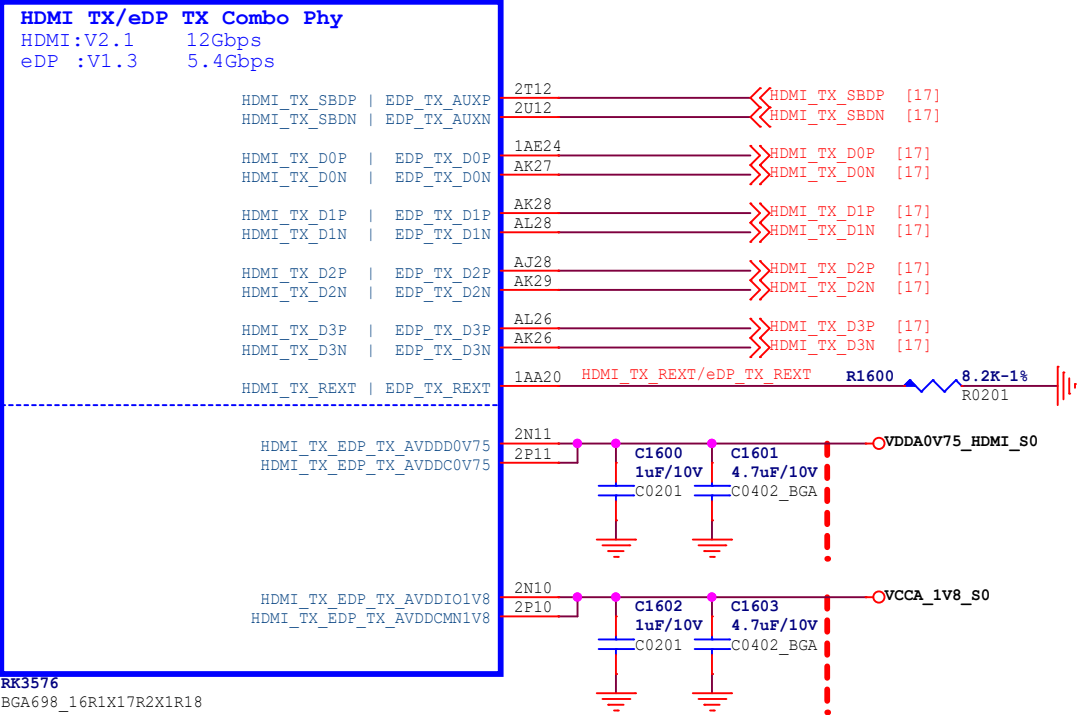


Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3576_Q (HDMI/eDP)

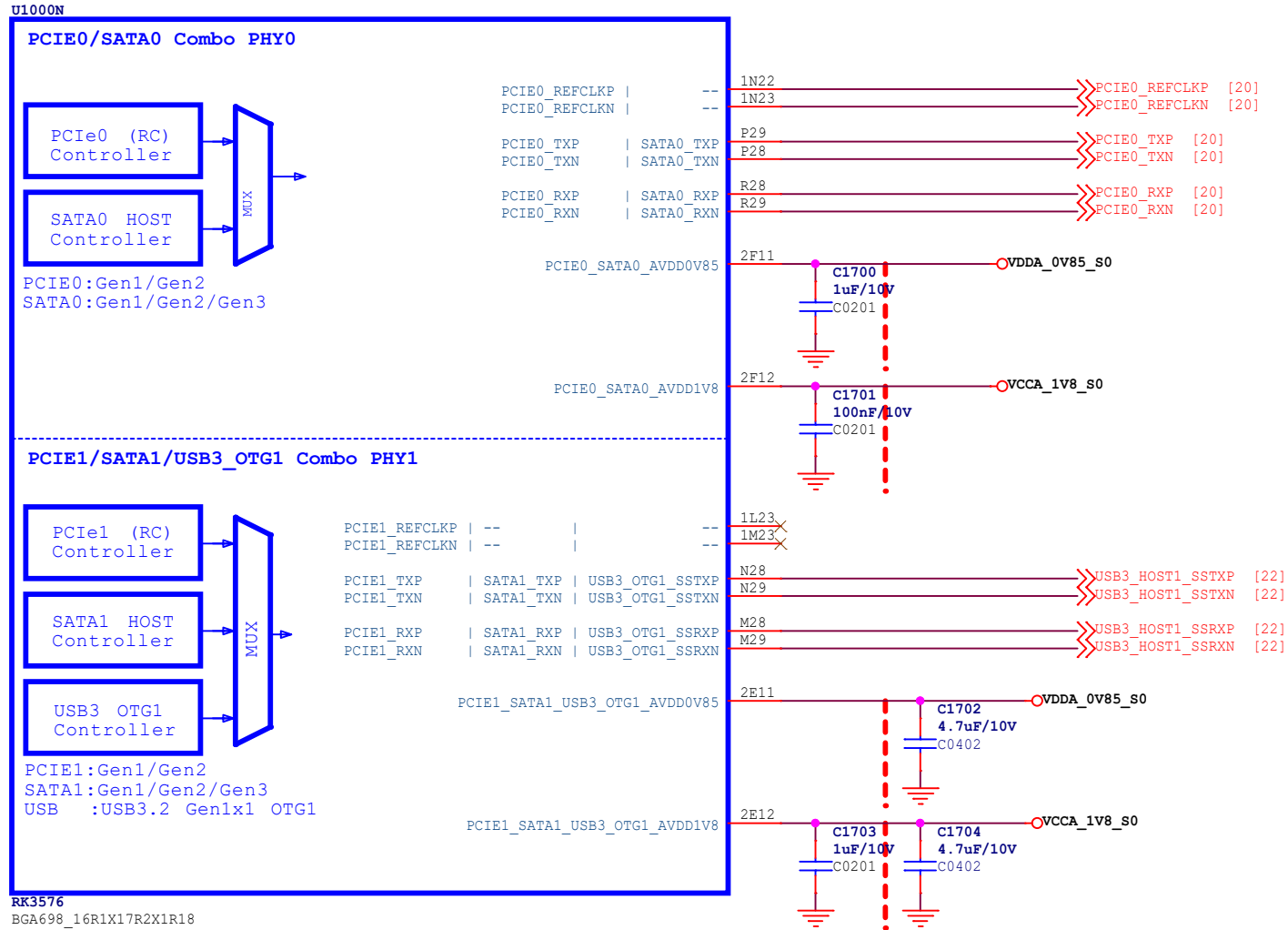
Note:
HDMI 2.1 supports up to 4Kx2K@120Hz
U1000Q



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

 armsom		https://armsom.org/	
Project:	ArmSoM-Sig5		
File:	RK3576-MIPI DSI/CSI		
Date:	Wednesday, May 22, 2024		Rev: V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 8 of 25

RK3576_N (PCIe/SATA/USB3)

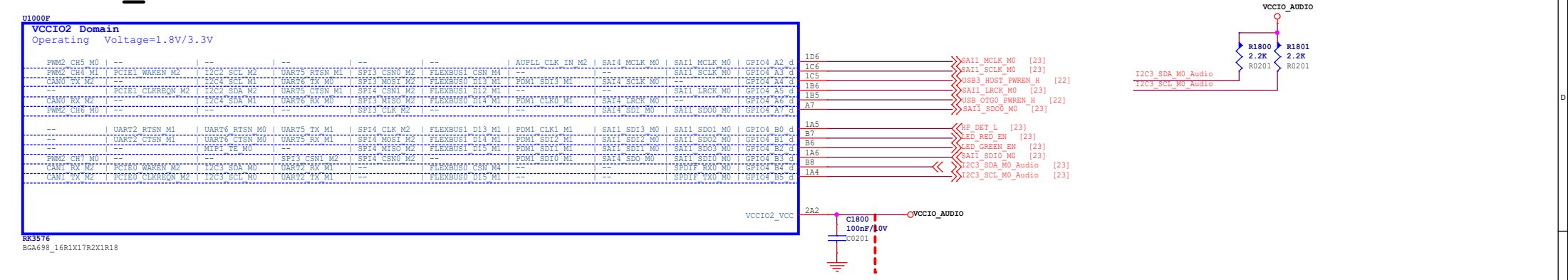


Note:

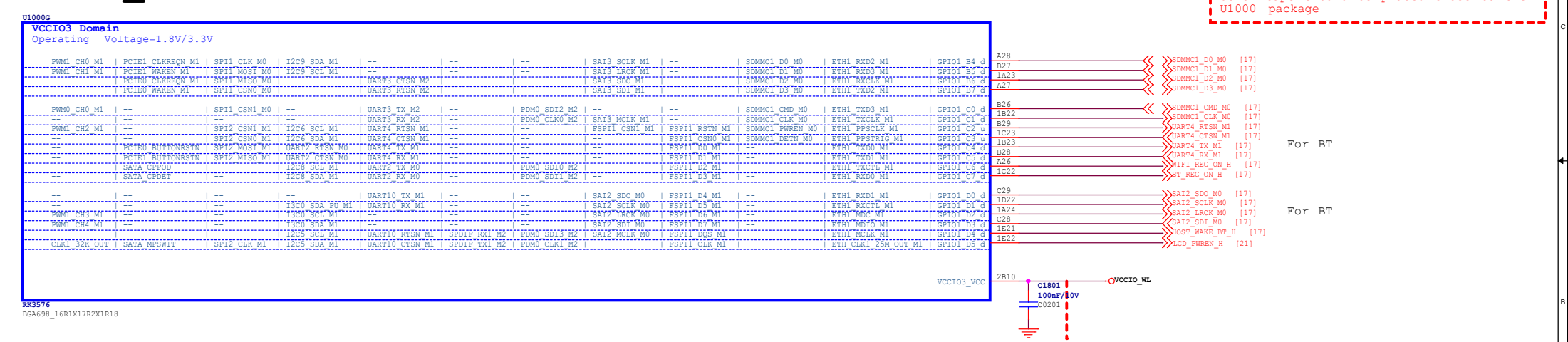
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

 armsom		https://armsom.org/	
Project:	ArmSoM-Sige5		
File:	RK3576-PCIe/SATA/USB3		
Date:	Tuesday, May 21, 2024		Rev: V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 9 of 25

RK3576_F (VCCIO2)

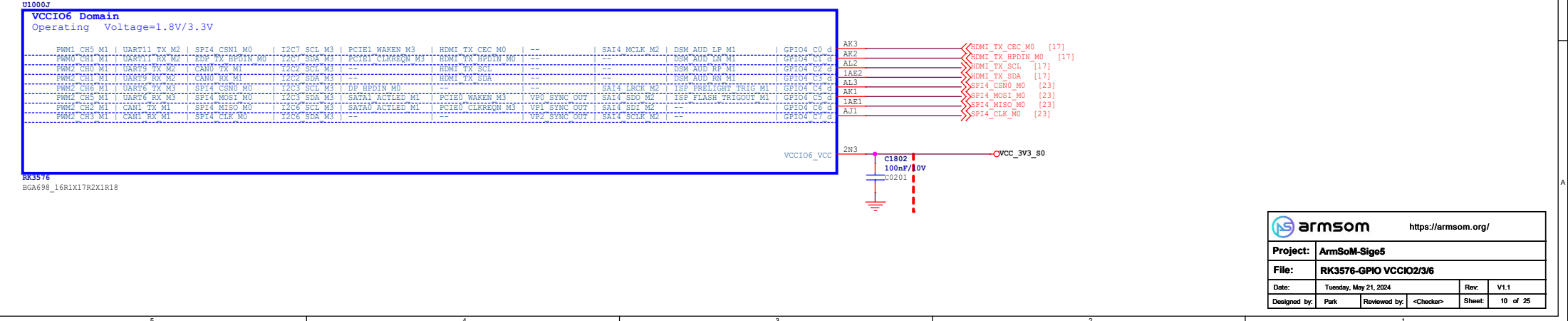


RK3576_G (VCCIO3)

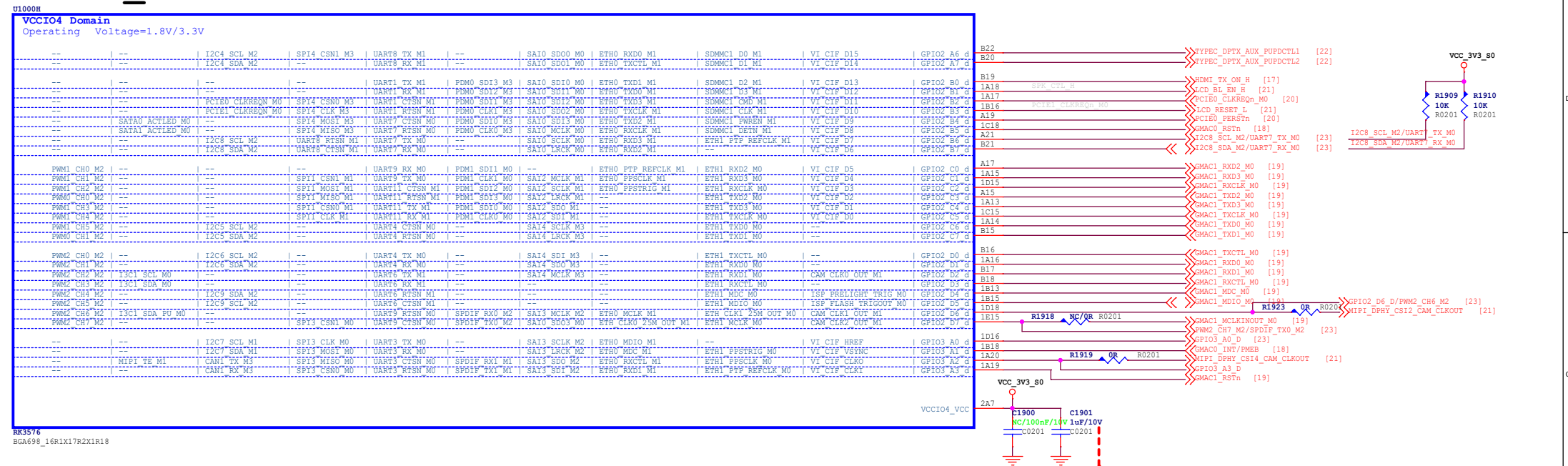


Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

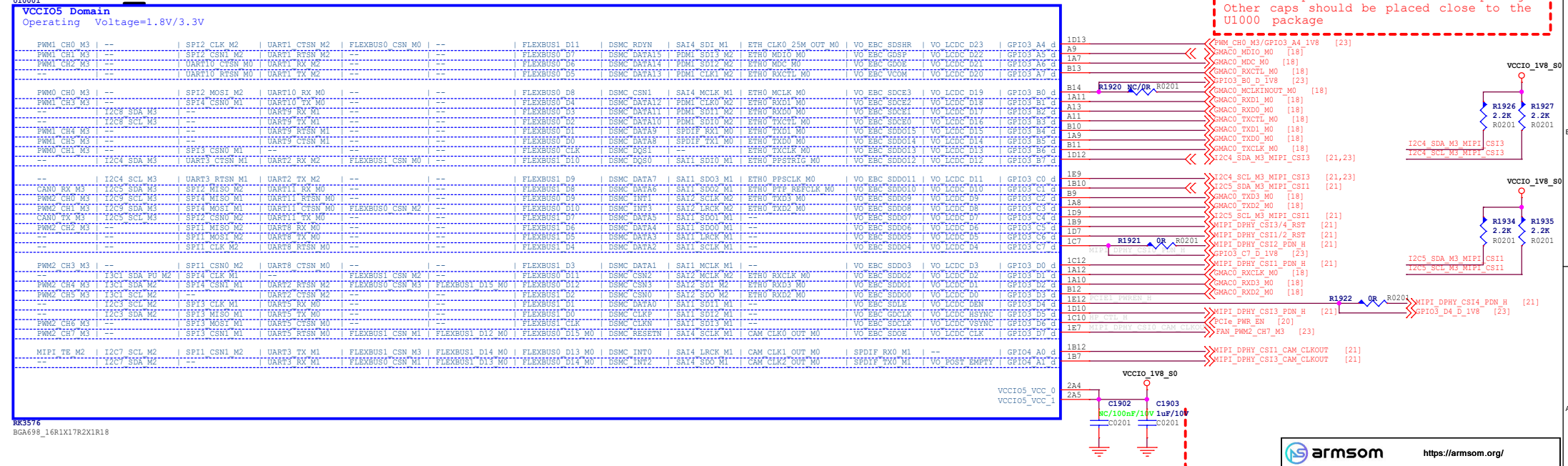
RK3576_J (VCCIO6)



RK3576 H (VCCIO4)



RK3576 I (VCCI05)



```

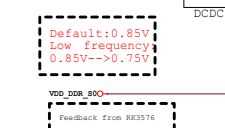
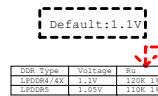
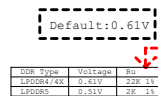
3] 12C1_SDA_M0_RK804 >>>
3] 12C1_SCL_M0_RK804 >>>

[3] PMIC_FWR_CTRL1 >>>
[3] PMIC_FWR_CTRL1 >>>

[3] PMIC_INT_1 <<<
[3,23] RESET_1 >>>

[13] PMIC_EXT_EN_OUT <<<
[23] PWON_1 >>>

```



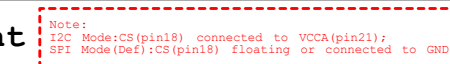
This device must be mounted. Replacing TVS mode is not recommended, if must, please choose the same specifications

Operating Supply Voltage : 5.5V(5.25-6V)

PeakPulse Current:>10A(tp=8/20uS)

Surge Clamping Voltage:<6.5V

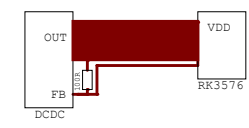
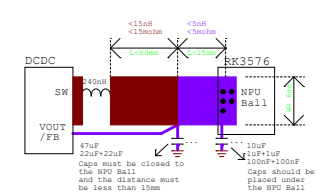
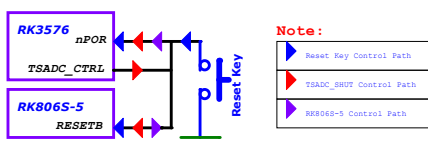
DO NOT DELETE IT!

[illegible]

Note:

The RK806 LDO power distribution of the reference schematics is only suitable for the interface used in the reference schematics.

If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re-evaluated, otherwise the added

[illegible]

Note:

	Reset Key Control Path
	TSADC_SHUT Control Path
	RK806S-5 Control Path

Default:1.8V

Default:1.8V

Default:1.2V

Default:3.0V

Default:3.3V

Default:0.75V

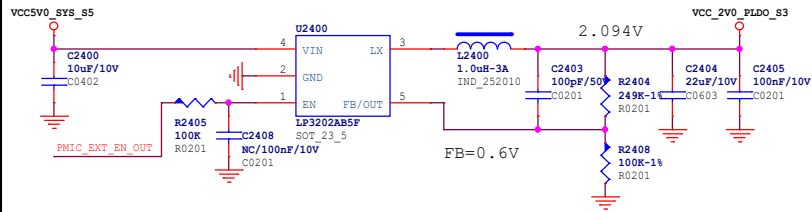
Default:0.85V;Low frequency:0.85V-->0.75V

Default:0.75V

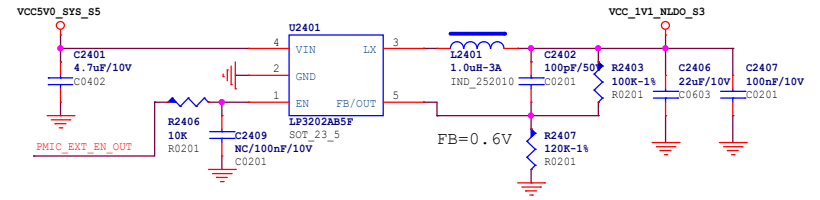
Default:0.85V

Default:0.75V

VCC_2V0_PLDO_S3

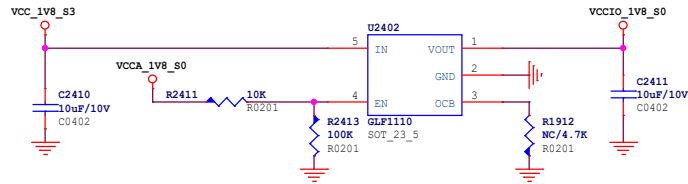


VCC_1V1_NLDO_S3



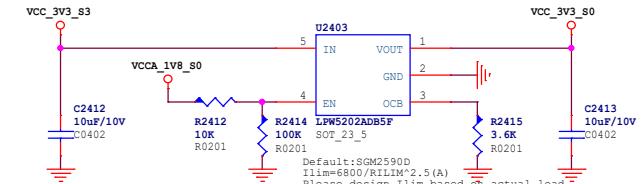
VCCIO_1V8_S0

Note: Need quick output discharge

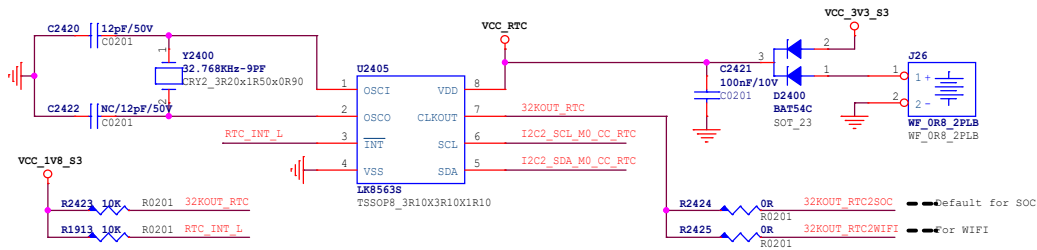


VCC_3V3_S0

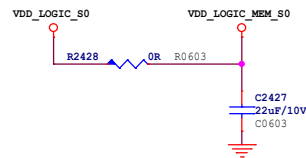
Note: Need quick output discharge



RTC

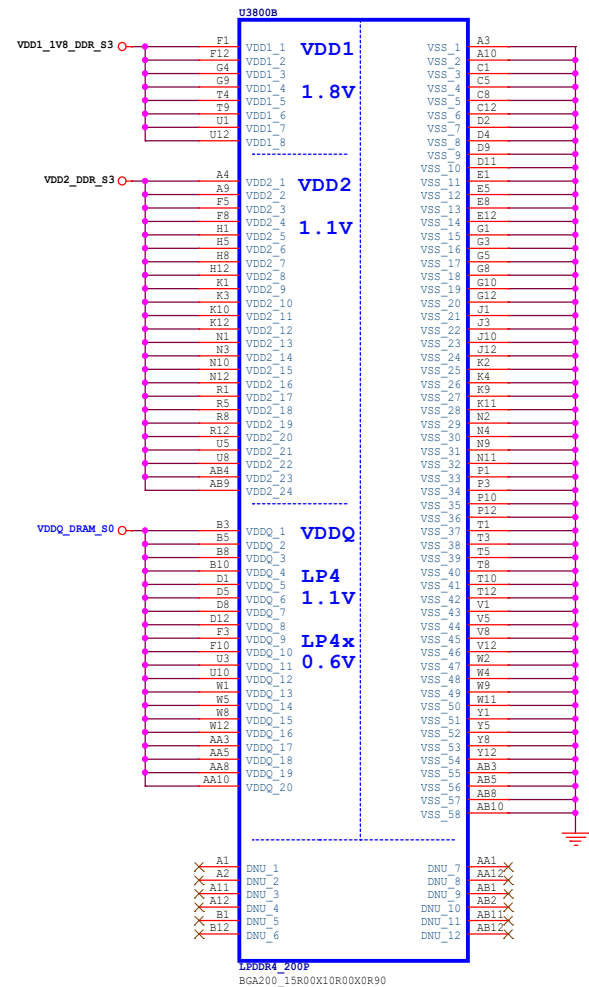
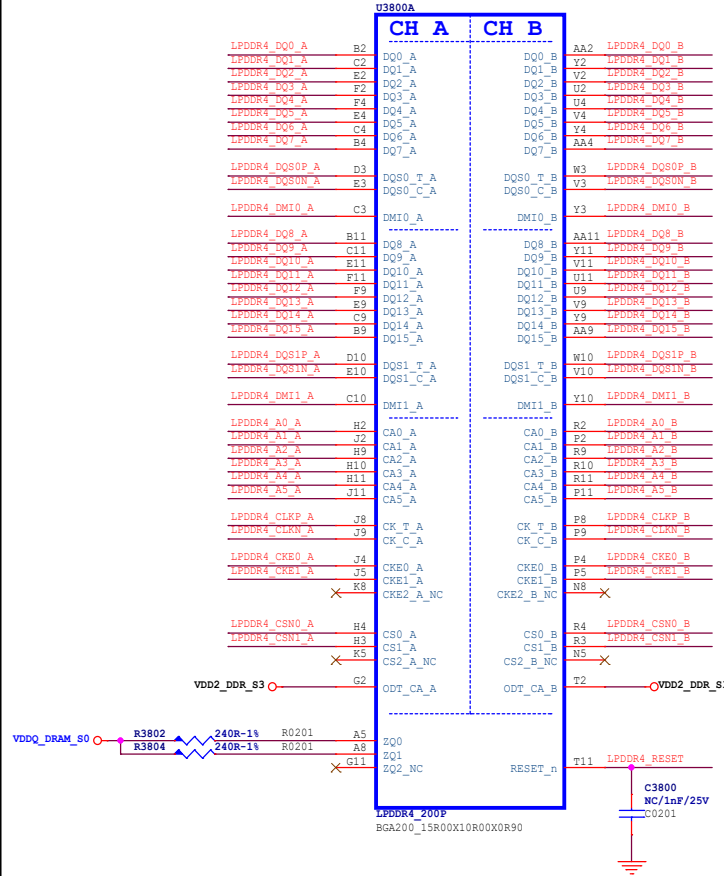
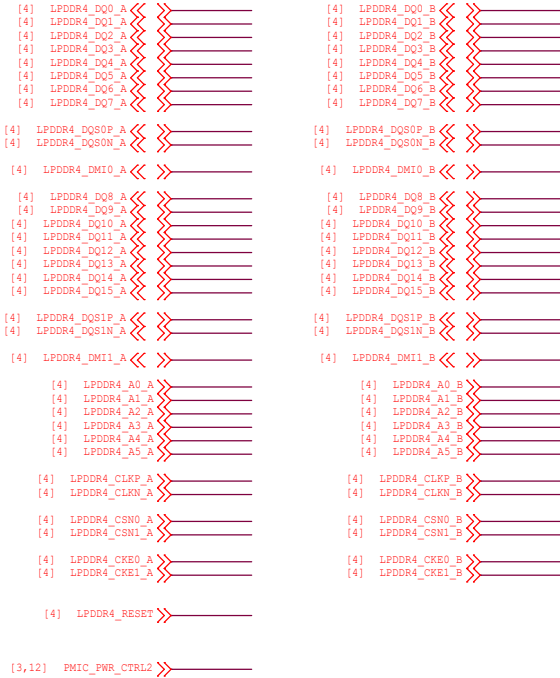


VDD_LOGIC_MEM EXT (Option for test)



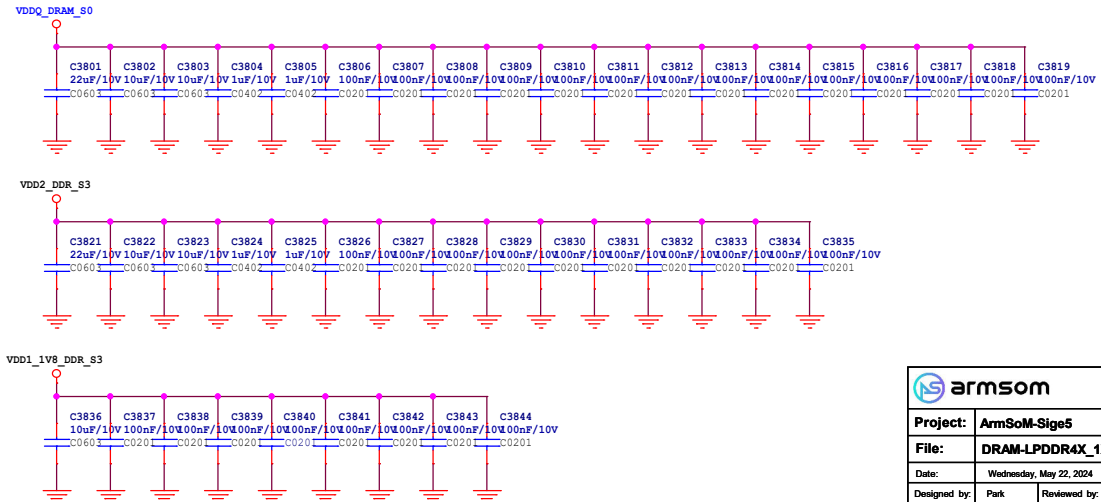
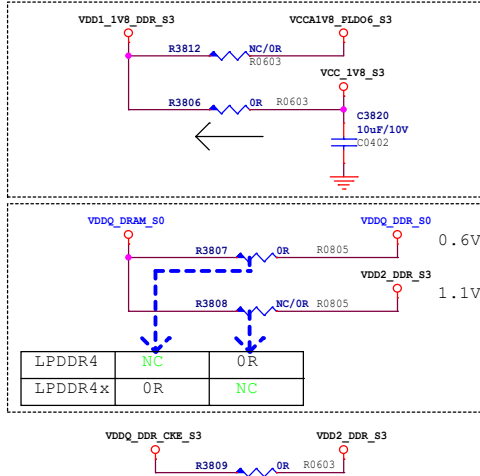
		https://armsom.org/	
Project:	ArmSoM-Sig5		
File:	Power-Ext Discrete/RTC		
Date:	Wednesday, May 22, 2024		Rev: V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 13 of 25

LPDDR4/4X



Note:
Sequence: VDD1-VDD2-VDDQ

	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65



		armsom		https://armsom.org/	
Project:	ArmSoM-Sig5				
File:	DRAM-LPDDR4X_1X32bit_200P				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	14 of 25

eMMC FLASH

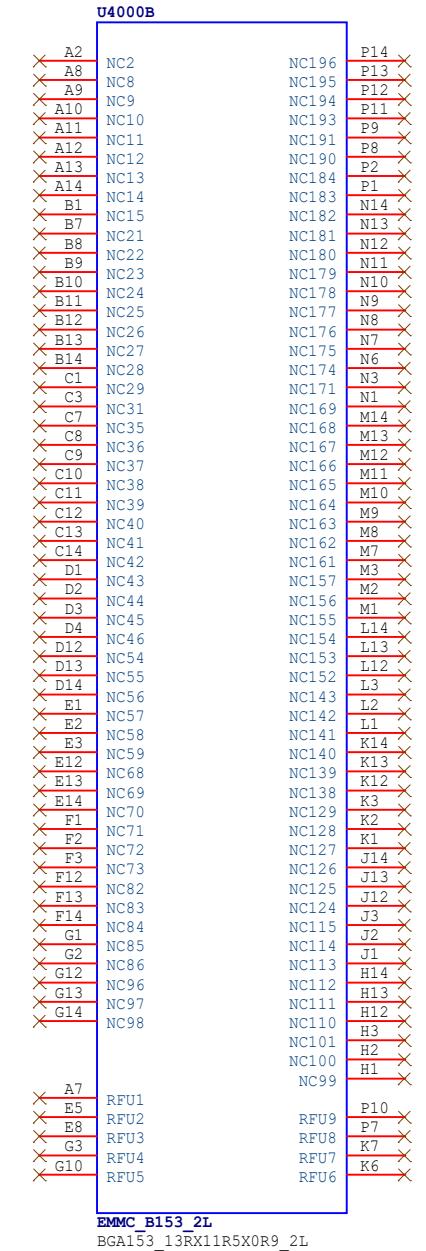
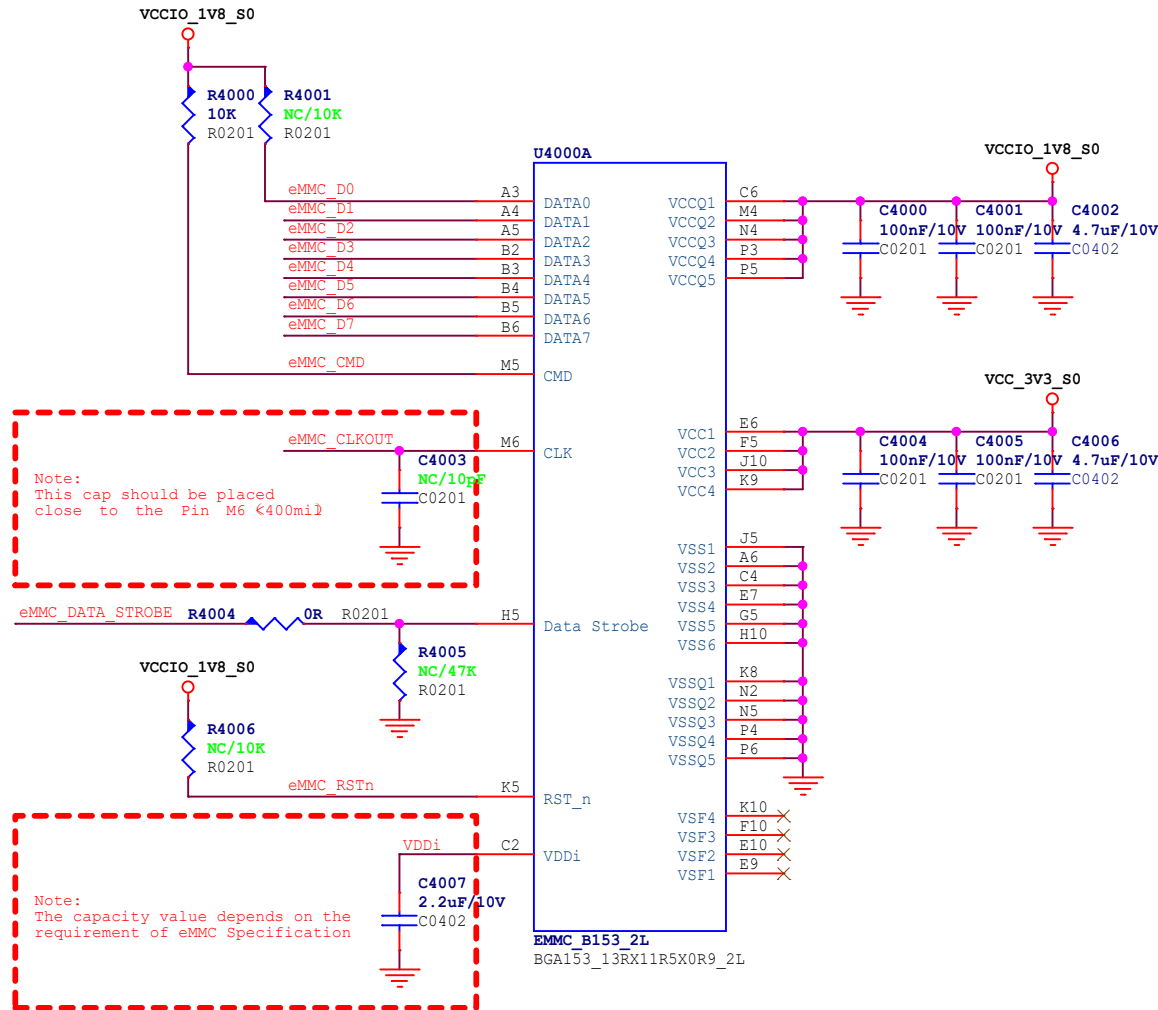
[5] eMMC_D0<<>>
[5] eMMC_D1<<>>
[5] eMMC_D2<<>>
[5] eMMC_D3<<>>
[5] eMMC_D4<<>>
[5] eMMC_D5<<>>
[5] eMMC_D6<<>>
[5] eMMC_D7<<>>

[5] eMMC_CMD<<>>

[5] eMMC_CLKOUT<<>>

[5] eMMC_DATA_STROBE<<>>

[5] eMMC_RSTn<<>>





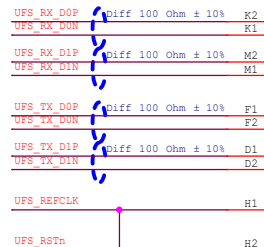
armsom

<https://armsom.org/>

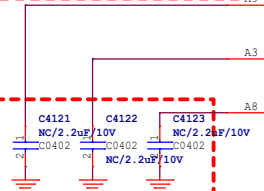
Project:	ArmSoM-Sige5				
File:	Flash-eMMC				
Date:	Wednesday, May 22, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	15 of 25

UFS Flash

(1) UFS_TX_D0P
(1) UFS_TX_D0N
(1) UFS_TX_D1P
(1) UFS_TX_D1N
(5) UFS_RX_D0P
(5) UFS_RX_D0N
(5) UFS_RX_D1P
(5) UFS_RX_D1N
(3) UFS_RSTn
(5) UFS_REFCLK

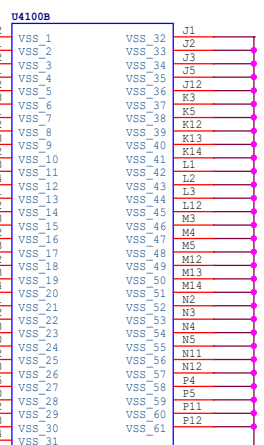


Note:
These caps should be placed close to the pin of UFS device



Note:
The capacitance value of these capacitors depends on the selected UFS device

NC/UFS_B153
FBGA153_11R5X13R0X1R00



NC/UFS_B153
FBGA153_11R5X13R0X1R00

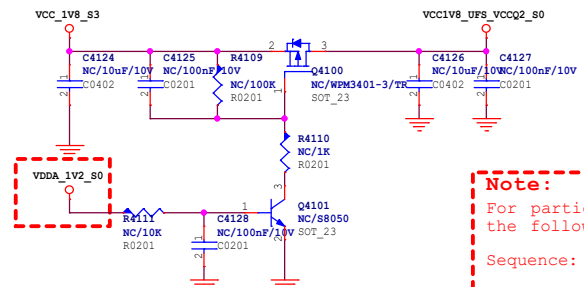
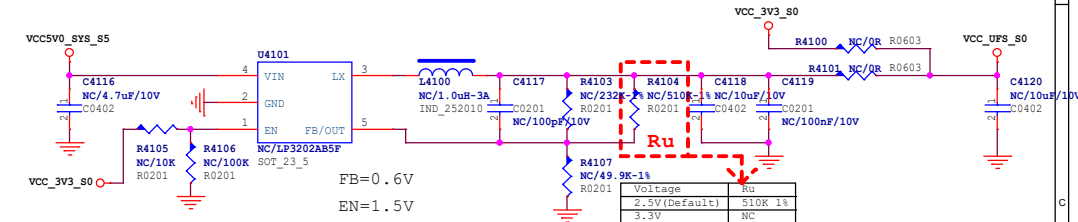
Note:
For particles above UFS4.0, Pin B13, P3, and P6 need to refer to the particle datasheet for design

UFS POWER

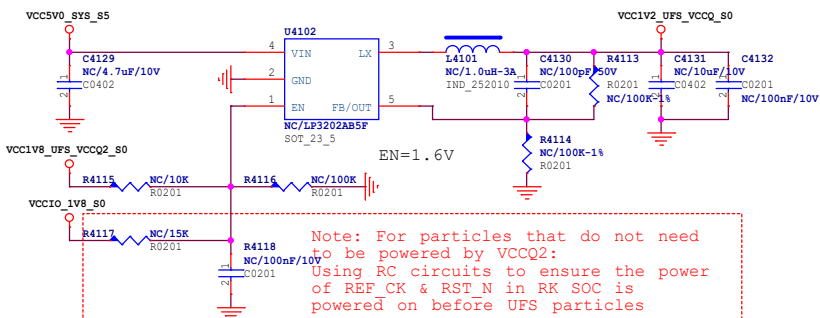
	VCCQ	VCCQ2	VCC	Default UFS device: UFS2.2
UFS2.0	1.2V	1.8V	3.3V	
UFS2.1	No Connect	1.8V	3.3V	
UFS2.2	No Connect	1.8V	3.3V	
UFS3.0	1.2V	No Connect	2.5V/3.3V	
UFS3.1	1.2V	No Connect	2.5V/3.3V	
UFS4.0	1.2V	No Connect	2.5V	

Sequence: VCCQ2->VCCQ, VCC is independent

Note: Do not support UFS4.0 Device!
The power ball that is not used at the particle must be kept floating.



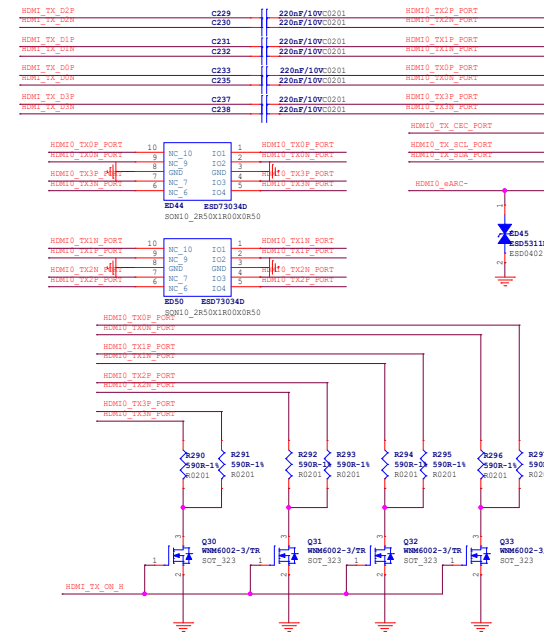
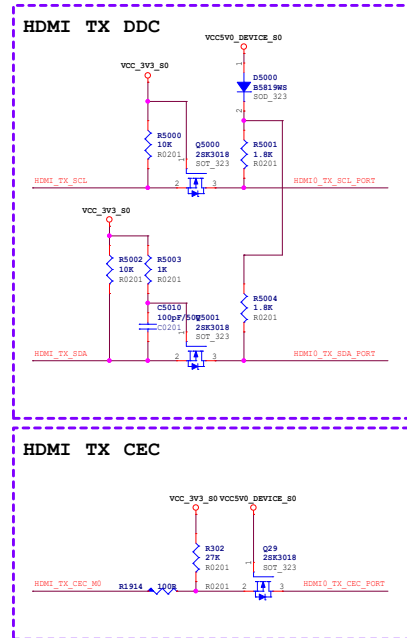
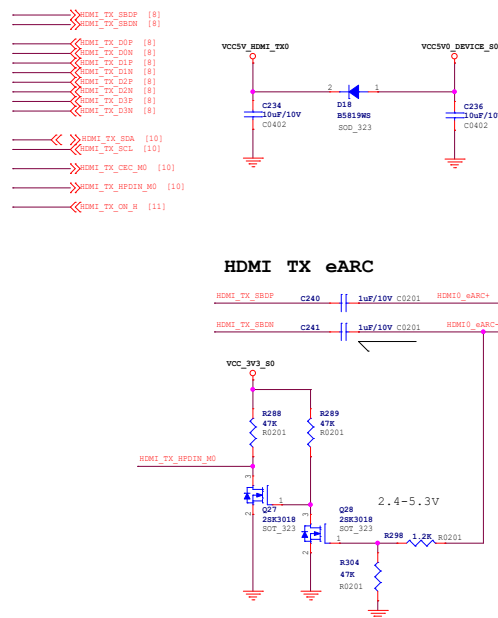
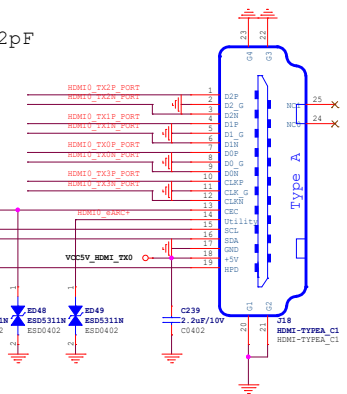
Note:
For particles that require VCCQ and VCCQ2, the following timing needs to be met:
Sequence: VDDA_1V2_S0->VCCQ2->VCCQ
VDDA_1V2_S0 is the power of REF CK & RST_N in RK SOC, which needs to be powered on before UFS particles



Note: For particles that do not need to be powered by VCCQ2:
Using RC circuits to ensure the power of REF CK & RST_N in RK SOC is powered on before UFS particles

armsom		https://armsom.org/	
Project: ArmSoM-Sig5			
File: Flash-UFS			
Date: Wednesday, May 22, 2024	Rev: V1.1	Designed by: Park	Reviewed by: <Checker>
Sheet: 16 of 25			

HDMI TX0

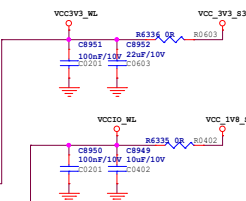
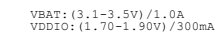
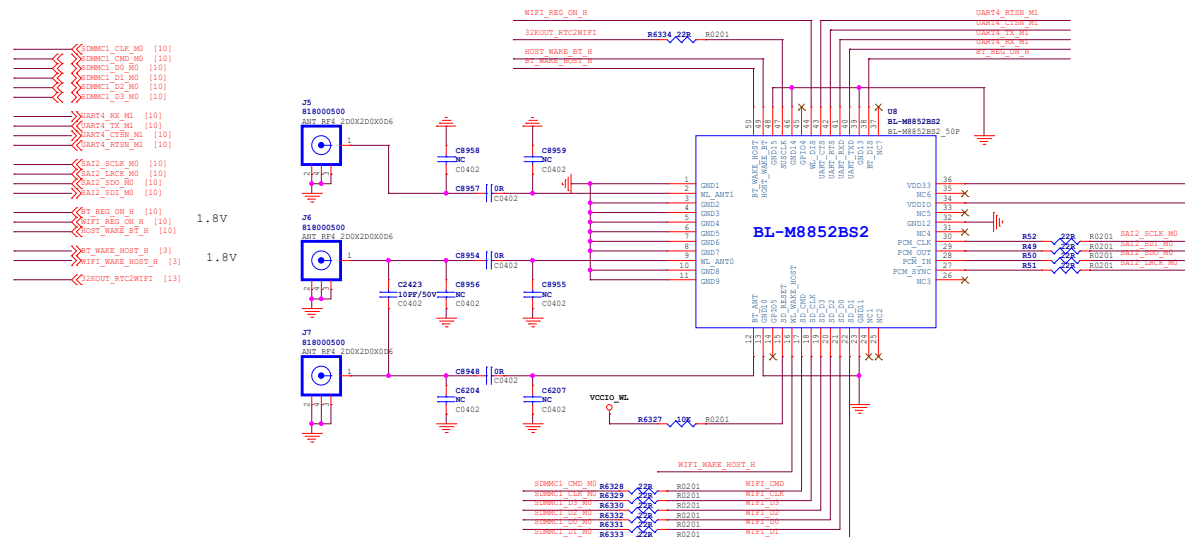
 $C_j \leq 0.2 \text{ pF}$ 

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

Note:
The controller only support AC coupled link. In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.

SDIO WIFI6/BT Module-2T2R



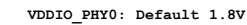
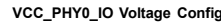
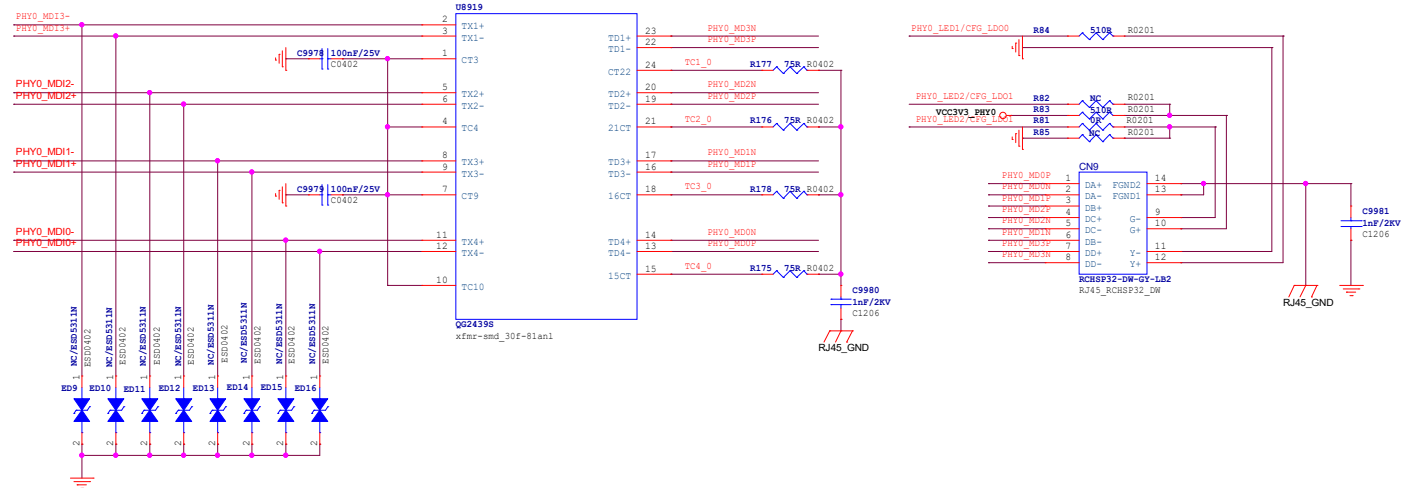
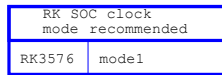
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    >>GNACO_TXD0_M0 [11]
    <<GNACO_TXD1_M0 [11]
    >>GNACO_TXD2_M0 [11]
    <<GNACO_TXD3_M0 [11]
    >>GNACO_TXCTL_M0 [11]
    <<GNACO_TXCLK_M0 [11]

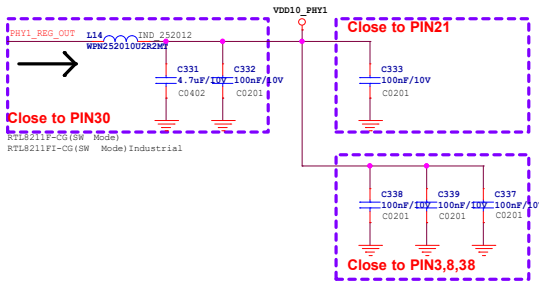
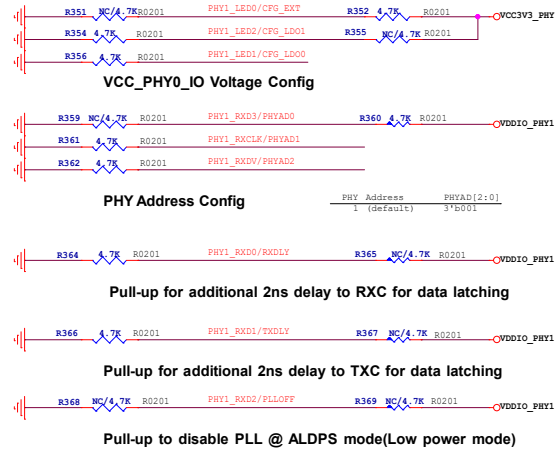
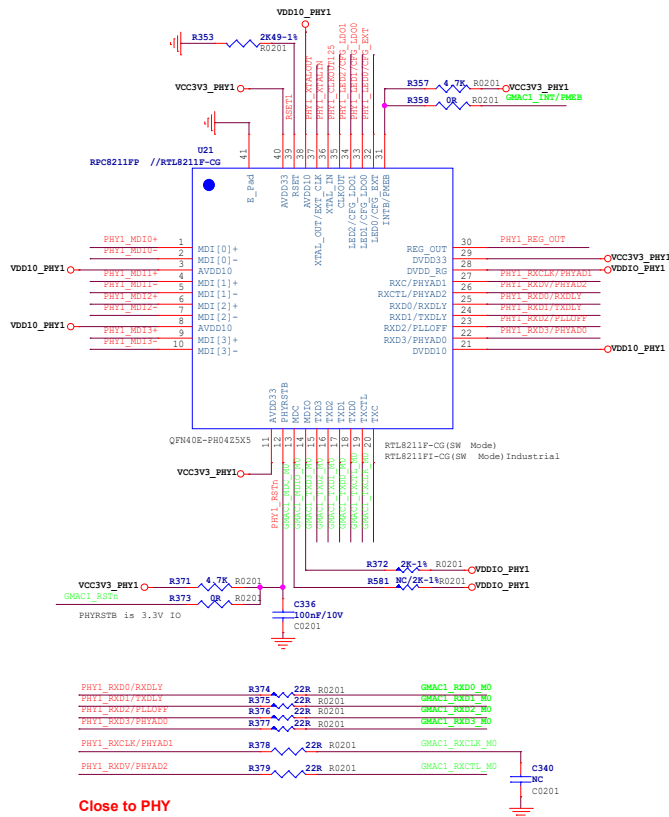
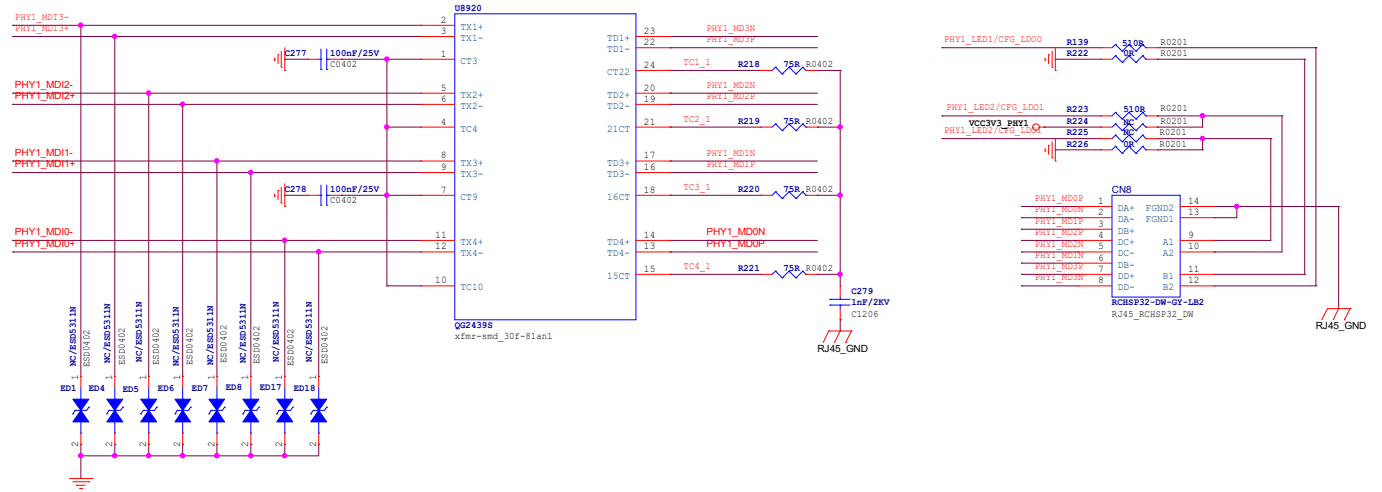
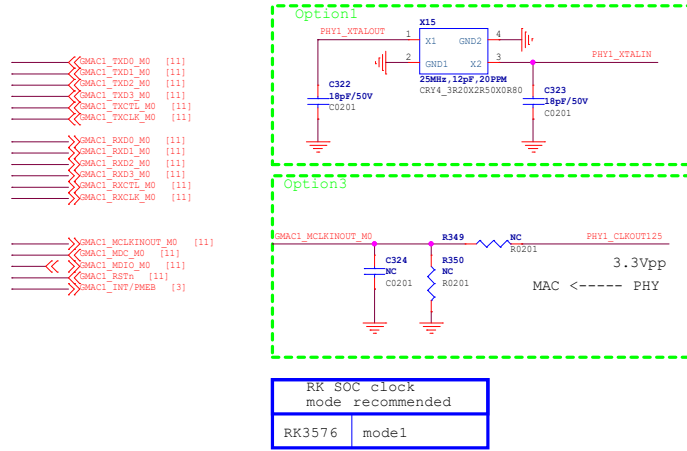
    >>GNACO_RXD0_M0 [11]
    <<GNACO_RXD1_M0 [11]
    >>GNACO_RXD2_M0 [11]
    <<GNACO_RXD3_M0 [11]
    >>GNACO_RXCTL_M0 [11]
    <<GNACO_RXCLK_M0 [11]

    >>GNACO_MCCLKINOUT_M0
    <<GNACO_MDC_M0 [11]
    <<GNACO_MDIO_M0 [11]
    <<GNACO_RSTn [11]
    GNACO_INT/PMBE [11]

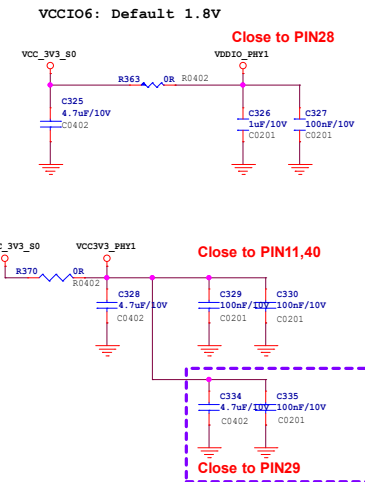
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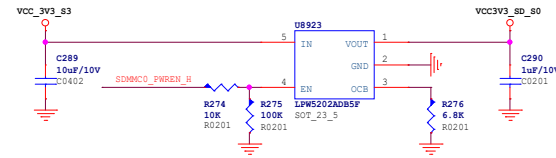
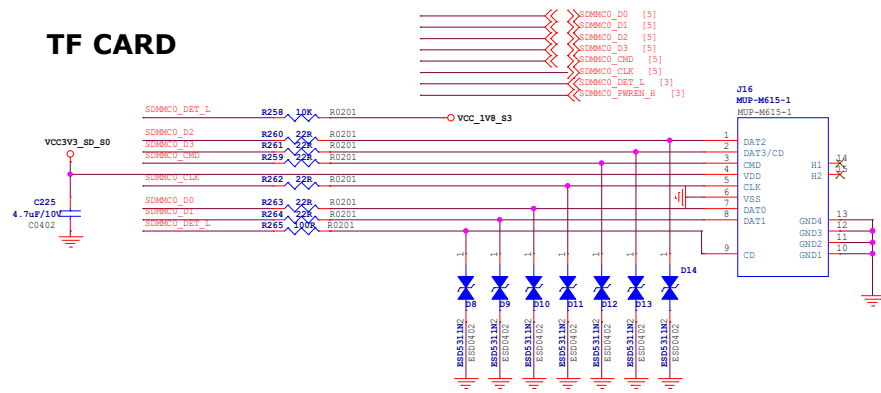
Giga PHY1_WAN



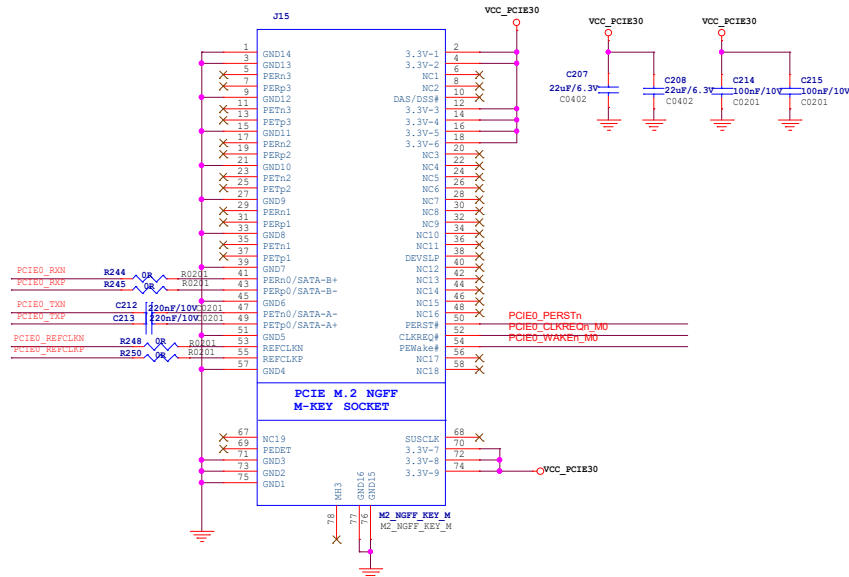
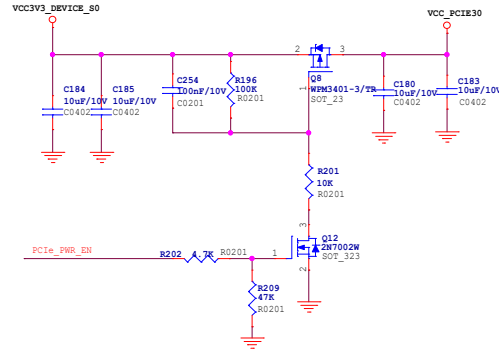
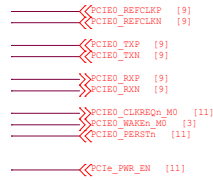
RGMI1 Power Source	CFG EXT	CFG LDO[1:0]	
External 3.3V(default)	1'b1	2'b00	CFG_EXT: 1:External Power Source for IO pad. 0:Integrated LDO for IO pad
External 1.8V	1'b1	2'b10	CFG_LDO[1:0]: 10:1.8V 00:3.3V
Internal 1.8V	1'b0	2'b10	



TF CARD



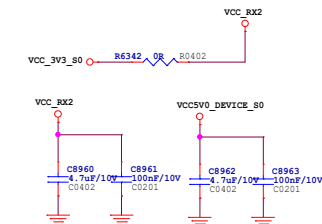
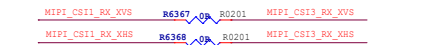
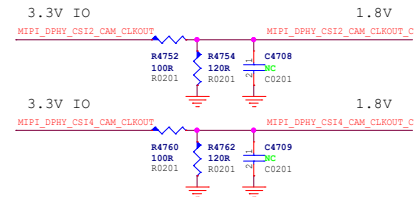
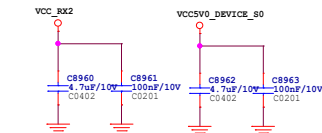
M.2_PCIE



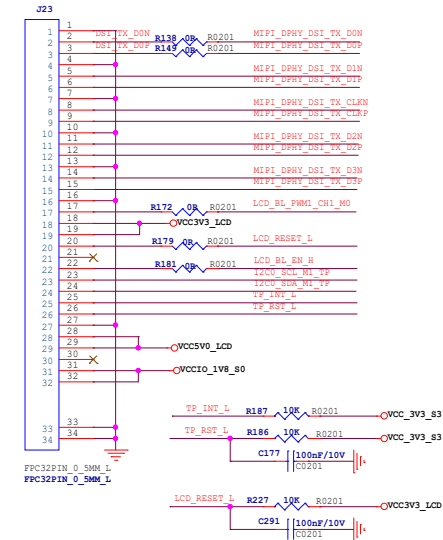
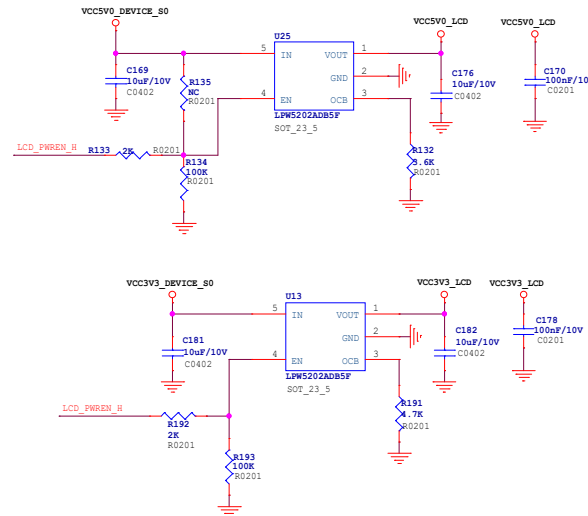
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>>>MPLI_DPHY_CS11_RX_DQDN [7]
>>>MPLI_DPHY_CS11_RX_DP [7]
>>>MPLI_DPHY_CS11_RX_DQDN [7]
>>>MPLI_DPHY_CS11_RX_DP [7]
>>>MPLI_DPHY_CS11_RX_CLKEN [7]
>>>MPLI_DPHY_CS11_RX_CLKP [7]
>>>MPLI_DPHY_CS11_RX_DQDN/GS12_RX_DQDN [7]
>>>MPLI_DPHY_CS11_RX_DQDP/GS12_RX_DQDP [7]
>>>MPLI_DPHY_CS11_RX_DQDP/GS12_RX_DQDP [7]
>>>MPLI_DPHY_CS11_RX_CLKEN [7]
>>>MPLI_DPHY_CS12_RX_CLKP [7]
>>>MPLI_DPHY_CS11_CAM_CLKOUT [11]
>>>MPLI_DPHY_CS12_CAM_CLKOUT [11]
>>>C2CS_SDA_M3_MIPSI_CS11 [11]
>>>C2CS_SCL_M3_MIPSI_CS11 [11]
>>>MPLI_DPHY_CS11_PDN_N [11]
>>>MPLI_DPHY_CS12_PDN_N [11]
>>>MPLI_DPHY_CS11/2_RST [11]

```

[illegible]

$\llcorner$MPI0_DPWH_DSI_TX_D0N [7]
 $\llcorner$MPI0_DPWH_DSI_TX_D0P [7]
 $\llcorner$MPI0_DPWH_DSI_TX_D1N [7]
 $\llcorner$MPI0_DPWH_DSI_TX_D1P [7]
 $\llcorner$MPI0_DPWH_DSI_TX_D2N [7]
 $\llcorner$MPI0_DPWH_DSI_TX_D2P [7]
 $\llcorner$MPI0_DPWH_DSI_TX_D3N [7]
 $\llcorner$MPI0_DPWH_DSI_TX_D3P [7]
 $\llcorner$MPI0_DPWH_DSI_TX_CLKN [7]
 $\llcorner$MPI0_DPWH_DSI_TX_CLKP [7]
 $\llcorner$C2C0_SCL_M1_TP [3,22]
 $\llcorner$C2C0_SDA_M1_TP [3,22]
 $\llcorner$FPGA_INT_L [3]
 $\llcorner$FPGA_RST_L [3]
 $\llcorner$C2C0_BL_PWM1_CH1_M0 [3]
 $\llcorner$C2C0_PAREN_L [1]
 $\llcorner$C2C0_RESET_L [1]
 $\llcorner$C2C0_BL_EN_R [1]
 $\llcorner$C2C0_BL_EN_L [1]

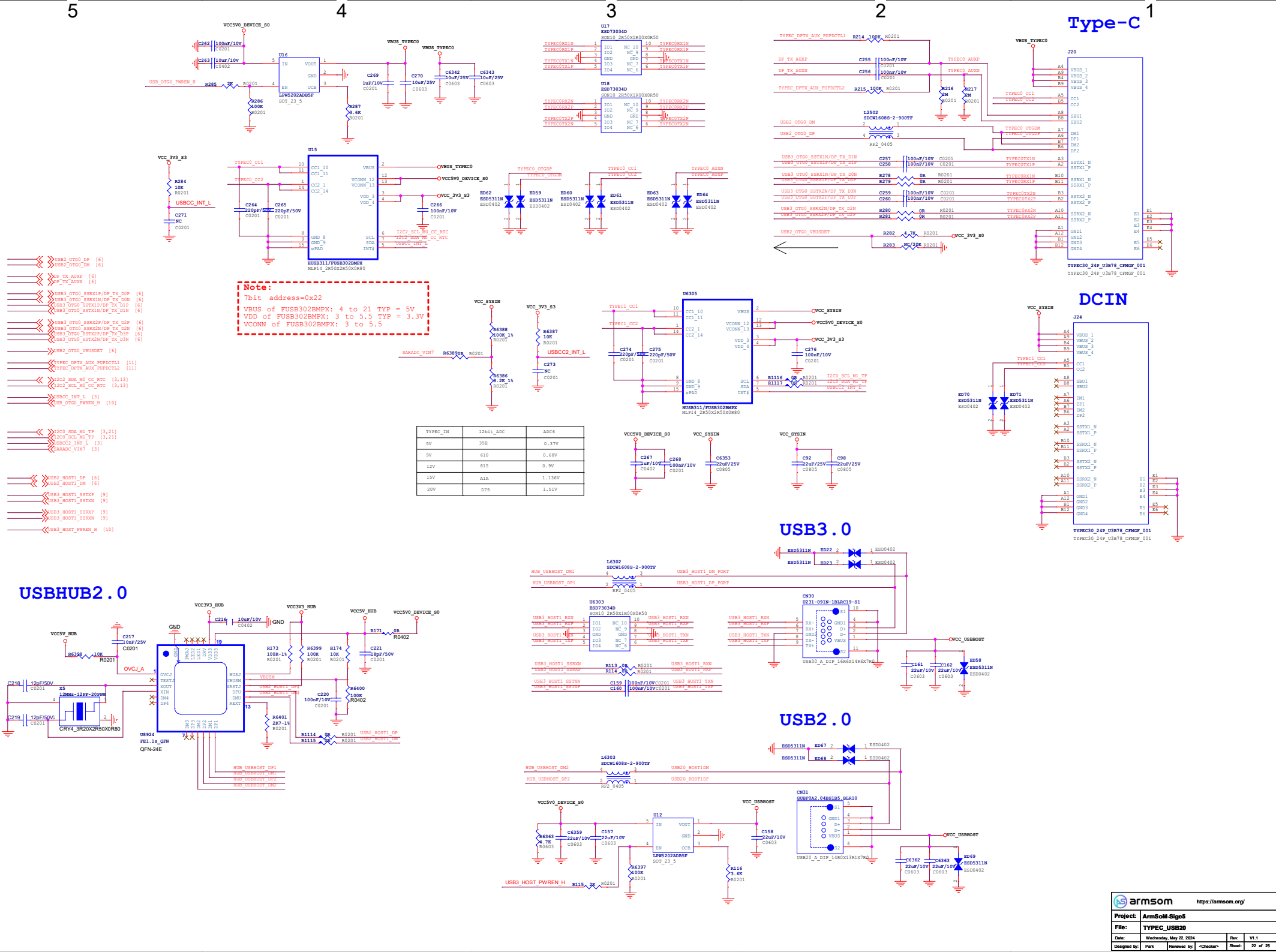


D

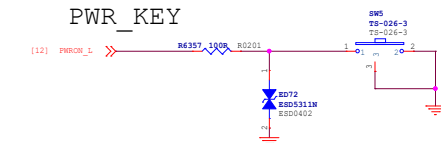
C

B

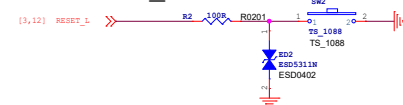
A



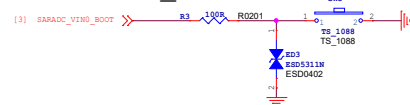
PWR KEY



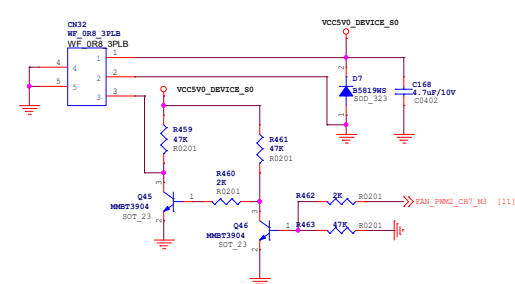
RESET_Key



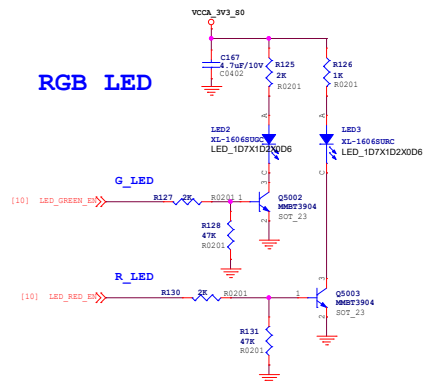
MASKROM_Key



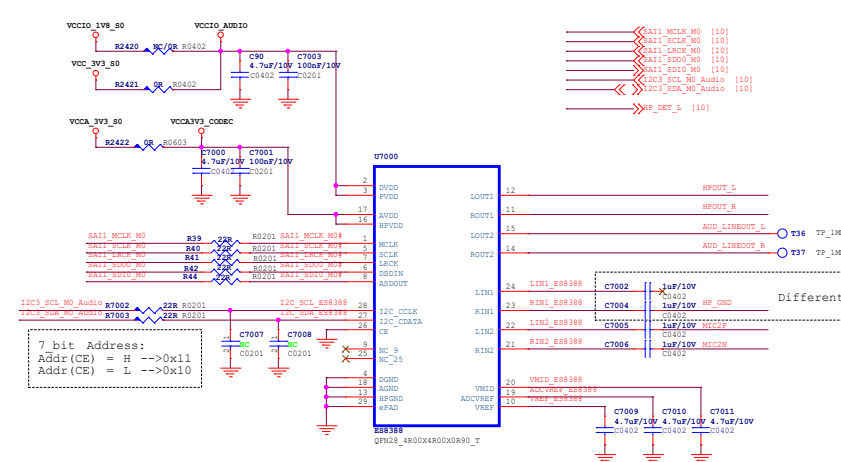
FAN



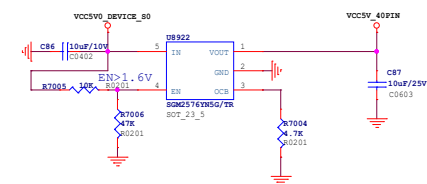
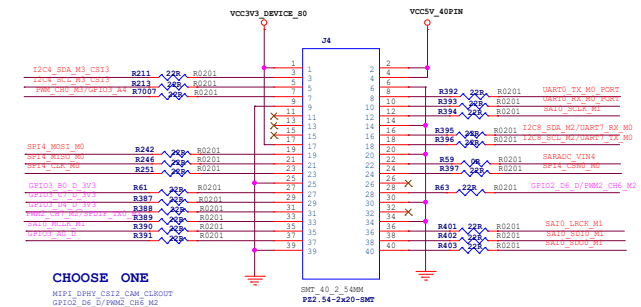
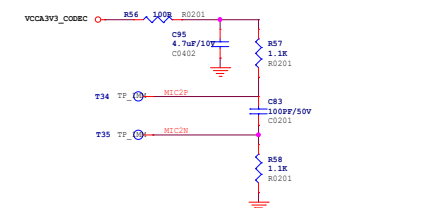
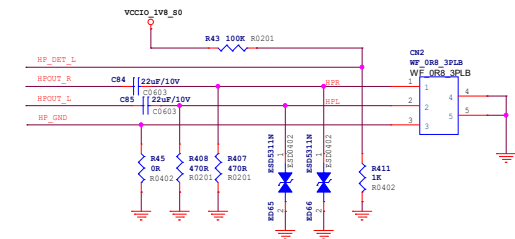
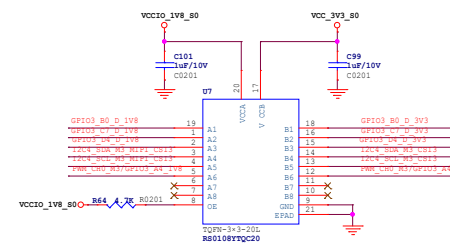
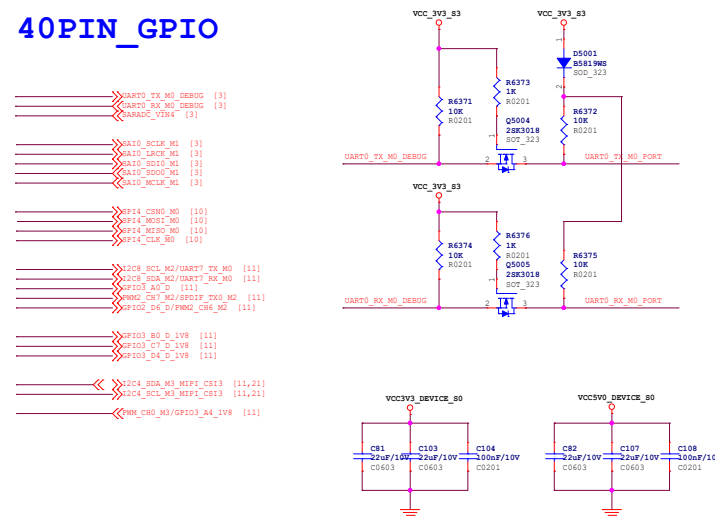
RGB LED

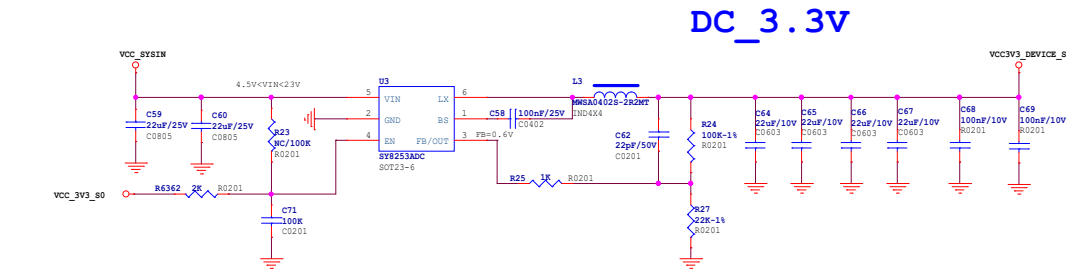
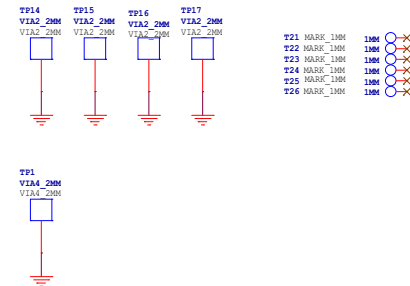
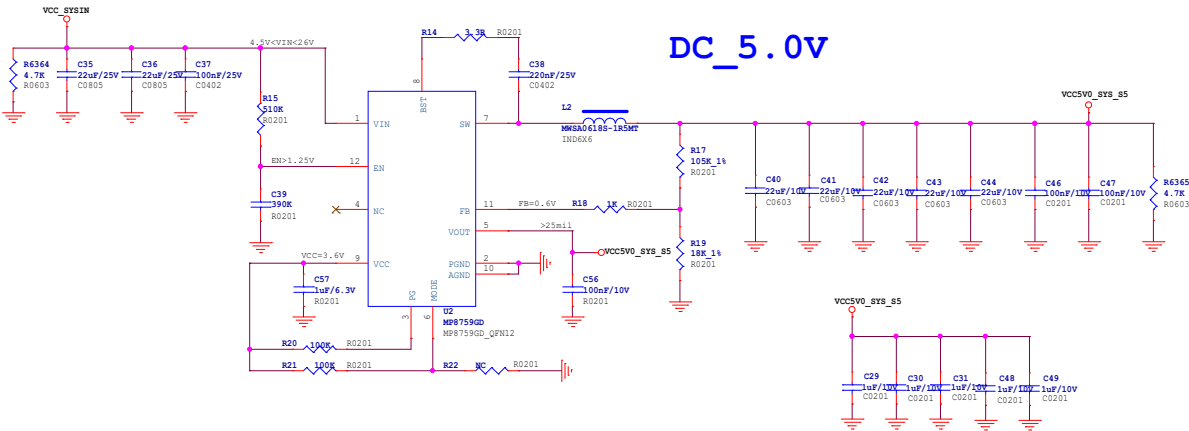
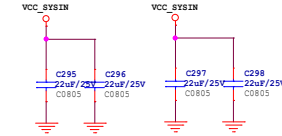
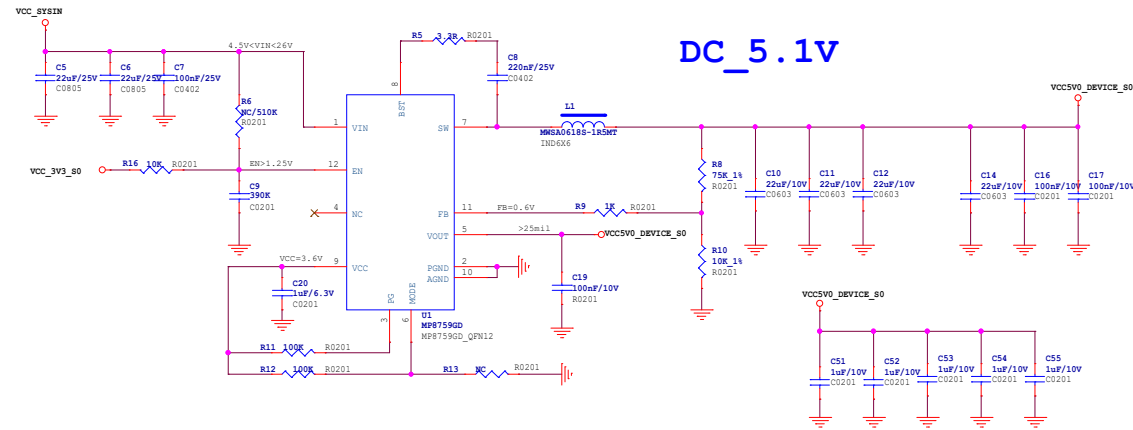


AUDIO CODEC



40PIN_GPIO





Revision History

Version	Date	By	Change Dscription	Approved
V1.0	2024-03-27	SL Chen	First release;	
V1.1	2024-05-15	SL Chen	1.U1/U2 Pin5 connect to output; TF_DET_L connect to VCC_1V8_S3; J23 Pin2&Pin3 change position; 2.J25 MIPI_DPHY_CSI3_CAM_CLKOUT&MIPI_DPHY_CSI4_CAM_CLKOUT_CON change position;	