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Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference
\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}
\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Description

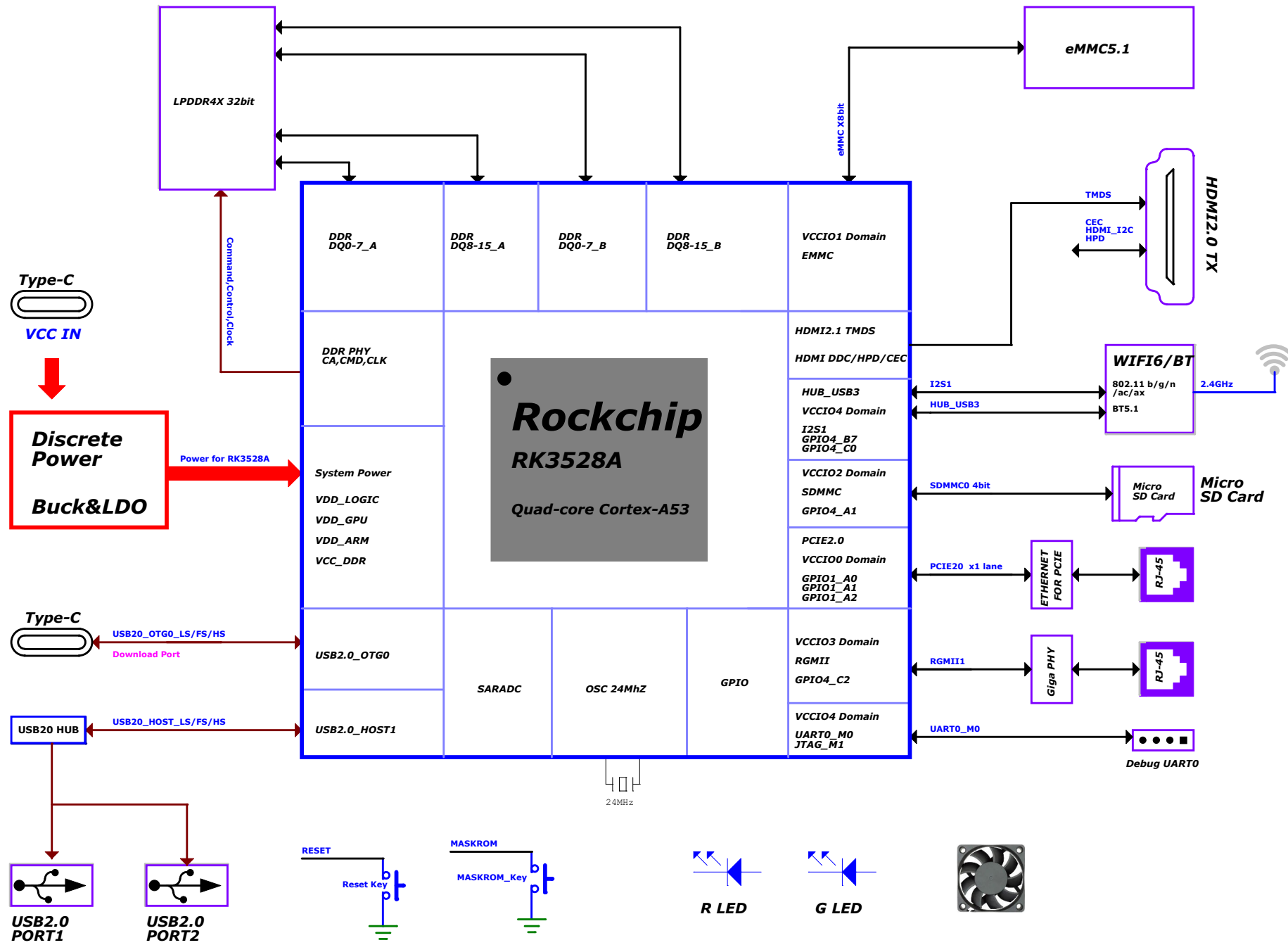
Note

Option

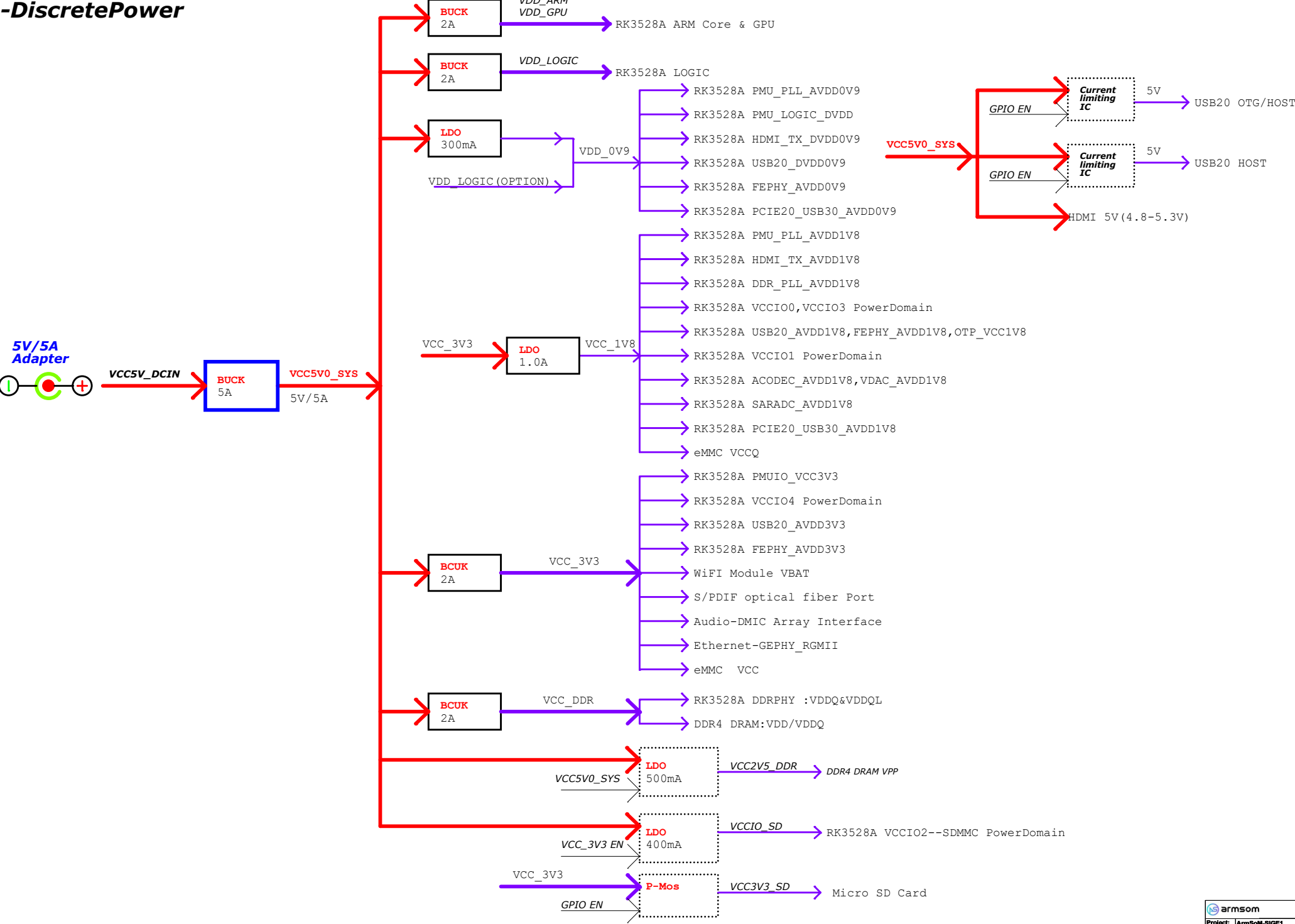
Revision History

Version	Date	By	Change Dscription	Approved
V1.0	2024-01-19	Liu Xinglin	1:Revision preliminary version	
V1.1	2024-07-01	Liu Xinglin	1. Replace DC-DC chip U2200 and peripheral circuitry. 2. Change R2207 to 47K. 3. Change R2209 to 51K. 4. Remove R2206, R2208; ground pin 1 of U2202. 5. Add U2502 and peripheral circuitry to control the VBUS pin of J2502. 6. Add Q2102, R2117, R2118. 7. Replace WIFI module U3005 and peripheral circuitry.	
V1.2	2024-07-26	Liu Xinglin	1. Replace models U2500, U2501, U2502 with SGM2576YN5G/TR. 2. Change R2833, R2834 to 22 ohms, and replace R2837 with 1K. 3. Change R3104, R3117 to 100 ohms.	

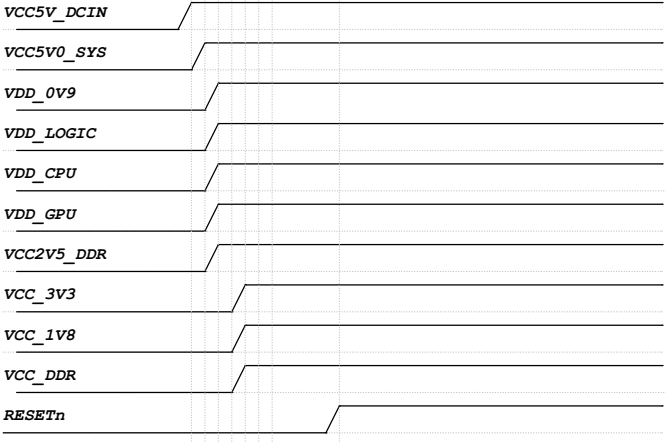
ArmSoM-SIGE1 Block Diagram



RK3528A Power Tree
-DiscretePower



DiscretePower Power Sequence

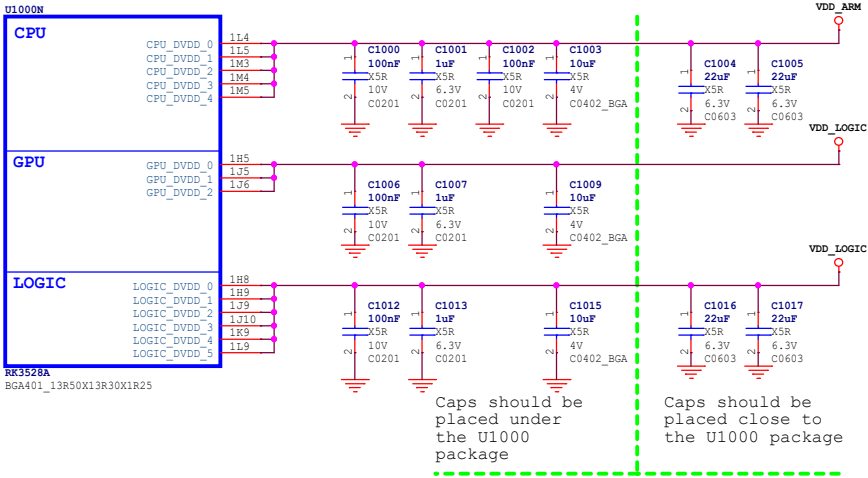


Power Supply	EXT BUCK&LDO	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC5V0_SYS	BUCK1	2.0A	VDD_LOGIC VDD_GPU	Slot:1	0.9V	ON	ON	TBD	TBD
VCC5V0_SYS	BUCK2	2.0A	VDD_ARM	Slot:1	0.95V	ON	ON	TBD	TBD
VCC5V0_SYS	LDO1	0.3A	VDD_0V9	Slot:1	0.9V	ON	ON	TBD	TBD
VCC_3V3	LDO2	1.0A	VCC_1V8	Slot:2	1.8V	ON	ON	TBD	TBD
VCC5V0_SYS	BUCK3	2.0A	VCC_3V3	Slot:2	3.3V	ON	ON	TBD	TBD
VCC5V0_SYS	BUCK4	2.0A	VCC_DDR	Slot:2	ADJ FB=0.6V	ON	ON	TBD	TBD
VCC5V_DCIN	BUCK5	3.0A	VCC5V0_SYS	Slot:0	5.2V	ON	ON	TBD	TBD

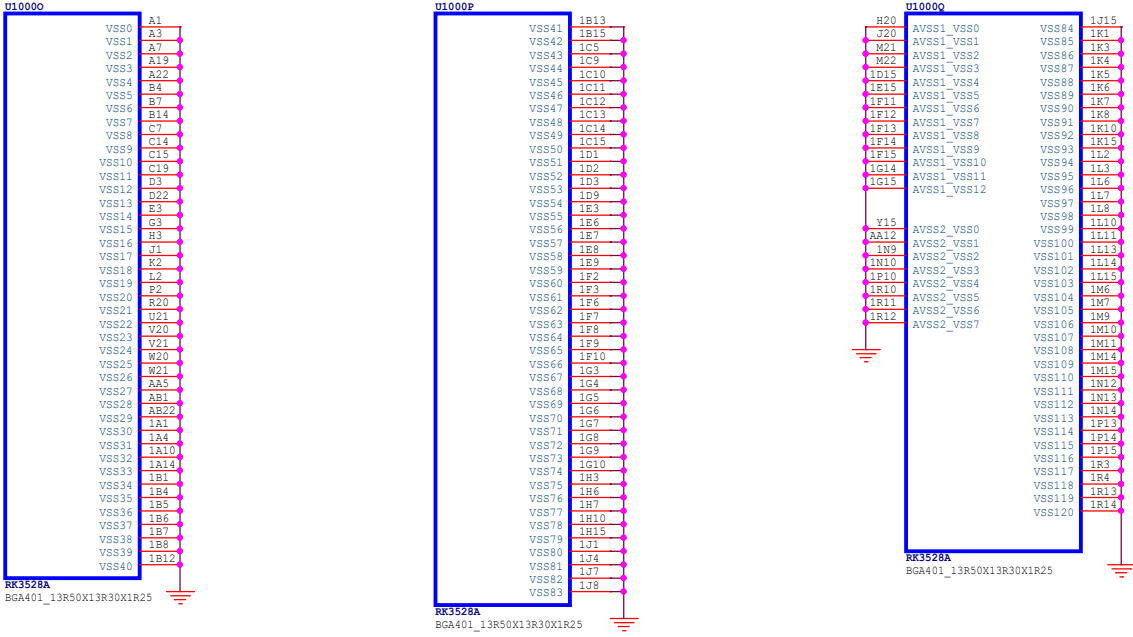
IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO	Pin 1J13	✓	✗	VCCIO_PMU	VCC_3V3	3.3V	
VCCIO0	Pin 1N6	✓	✓	VCCIO0	VCCIO_WL	1.8V	
VCCIO1	Pin 1P8	✓	✓	VCCIO1	VCCIO_FLASH	1.8V/3.3V	Select as required
VCCIO2	Pin 1B14	✓	✓	VCCIO2	VCCIO_SD	1.8V/3.3V	SD3.0 Voltage=1.8V SD2.0 Voltage=3.3V 3.3V-->1.8V
VCCIO3	Pin 1M13	✓	✓	VCCIO3	VCC_1V8 VCC_3V3	1.8V 3.3V	Select as required
VCCIO4	Pin 1J3	✓	✓	VCCIO4	VCC_3V3	3.3V	

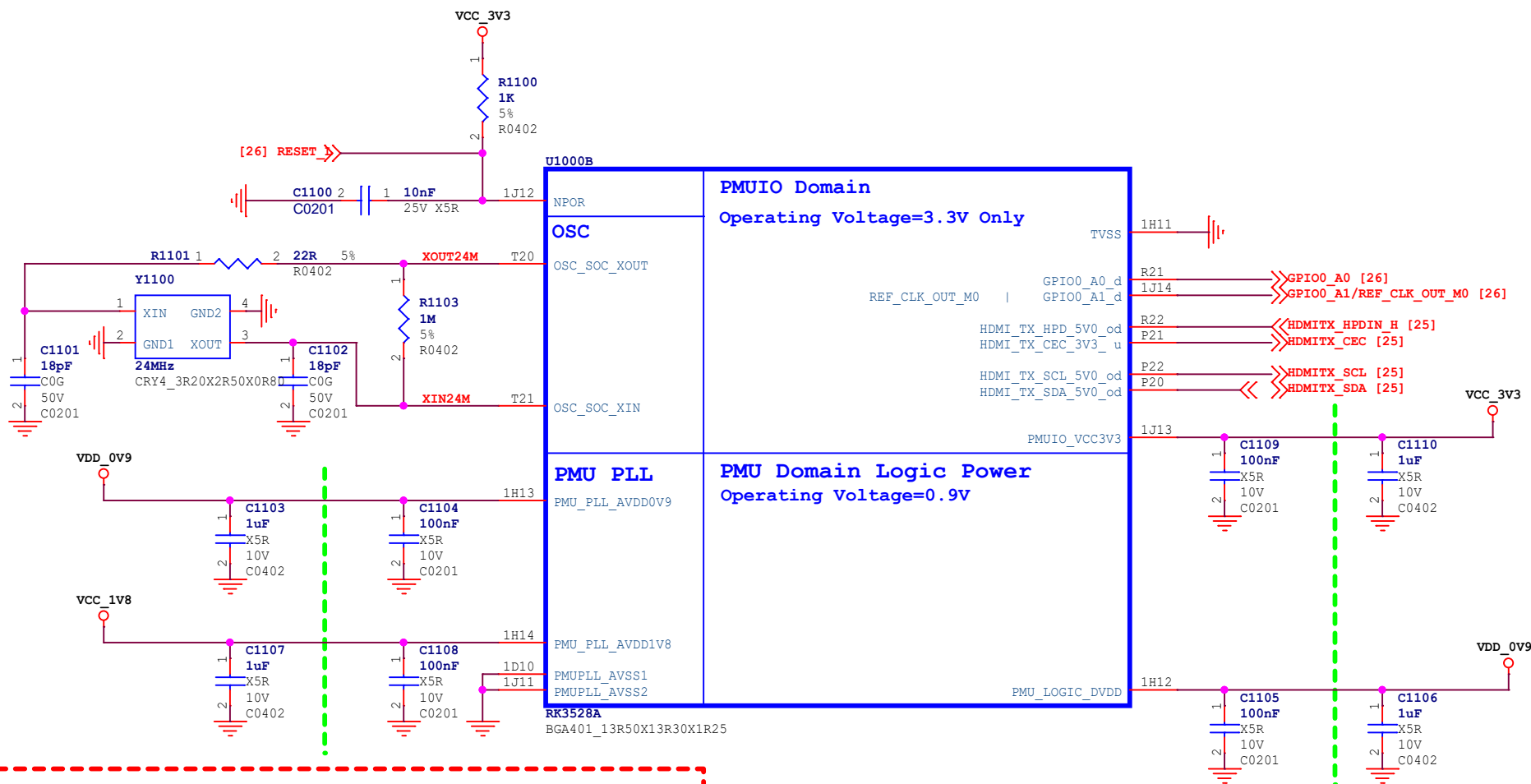
RK3528A_N (POWER)



RK3528A_O/P/Q (GND)

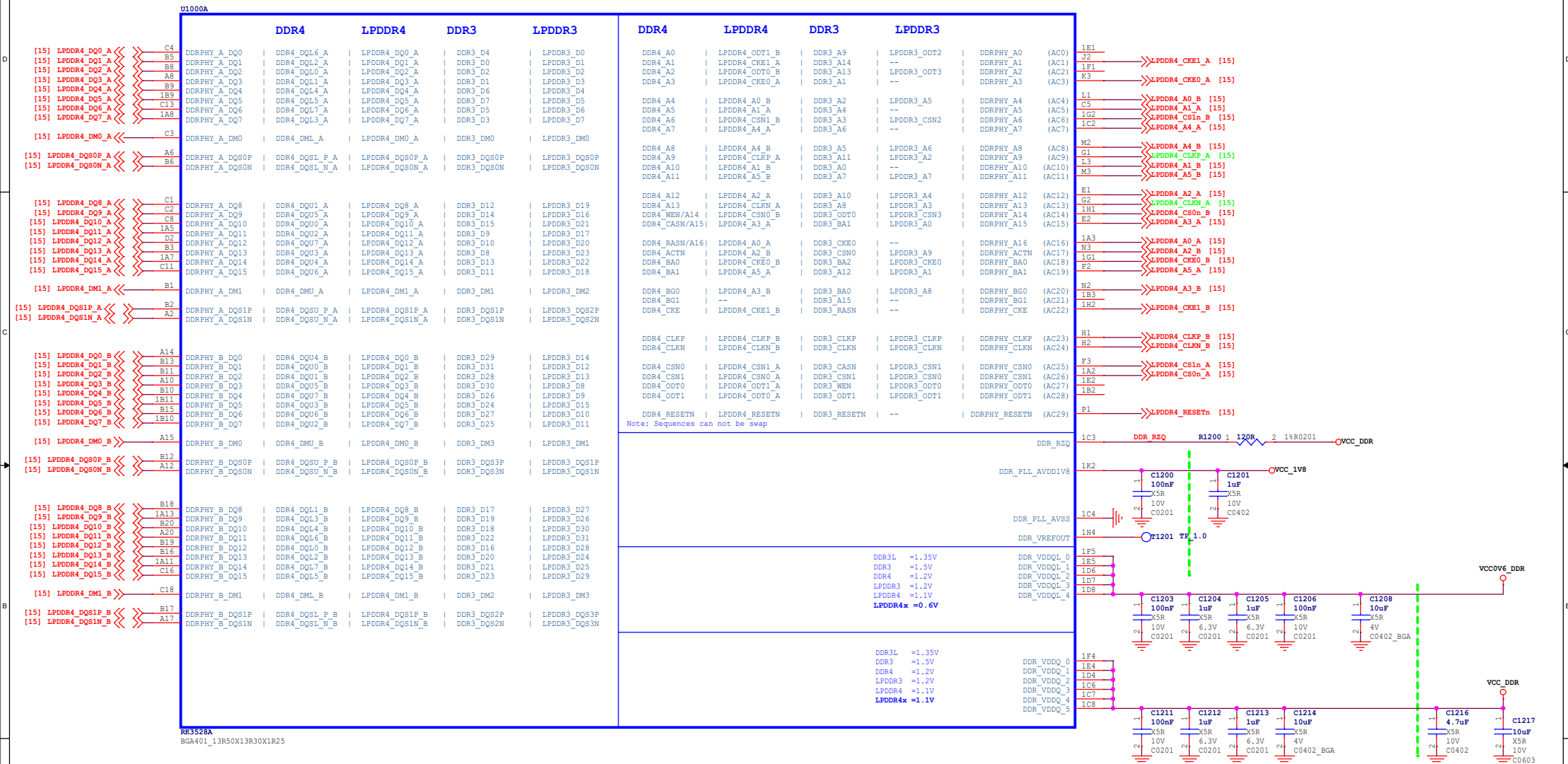


RK3528A B (OSC/PLL/PMUIO Domain)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

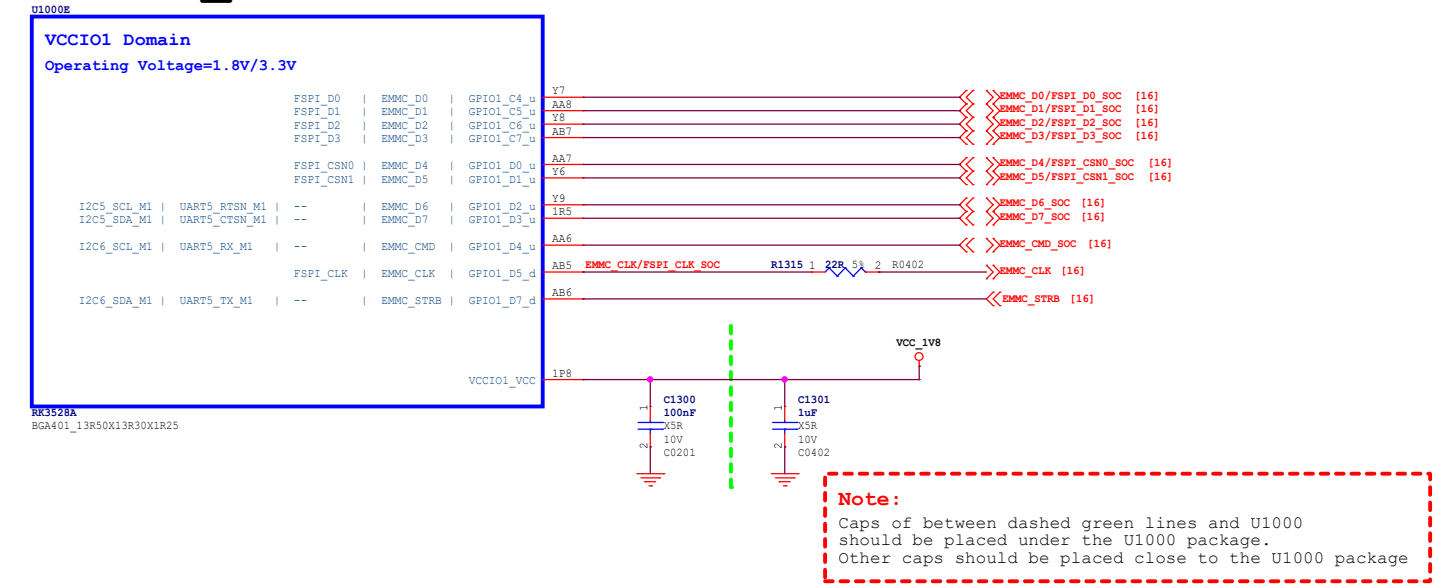
RK3528A A (DDR PHY)



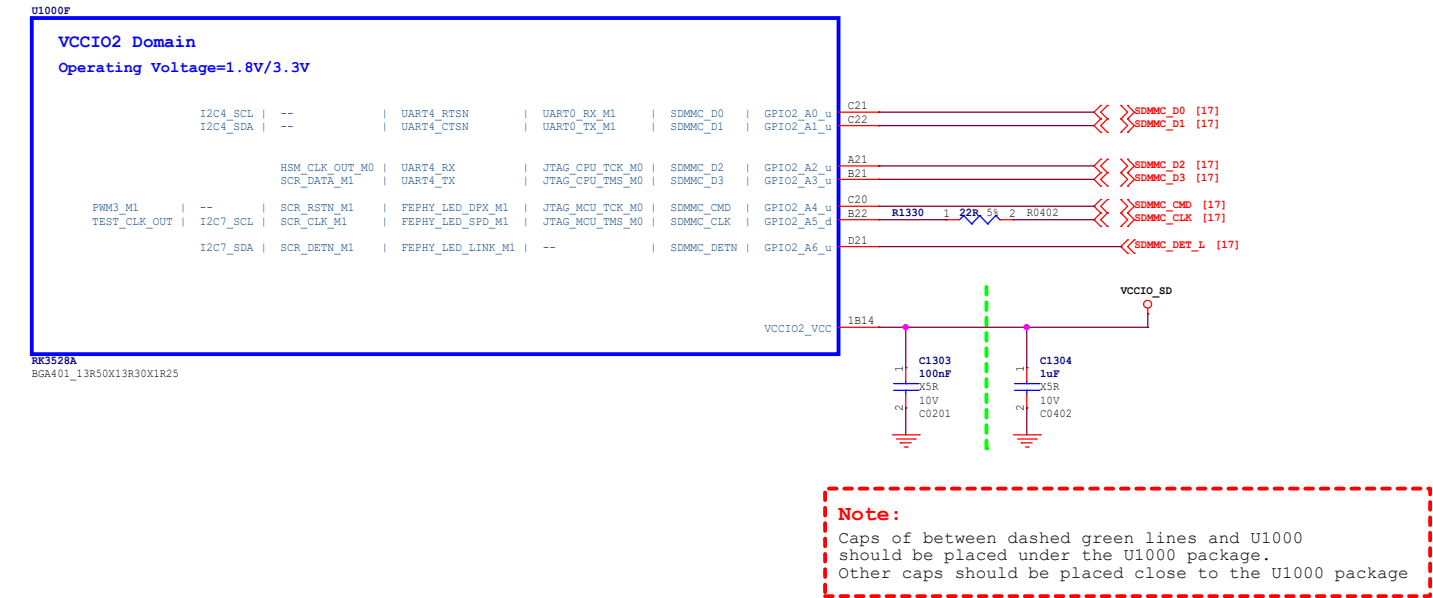
Note:

Caps of between dashed green lines and U1000
 should be placed under the U1000 package.
 Other caps should be placed close to the U1000 package

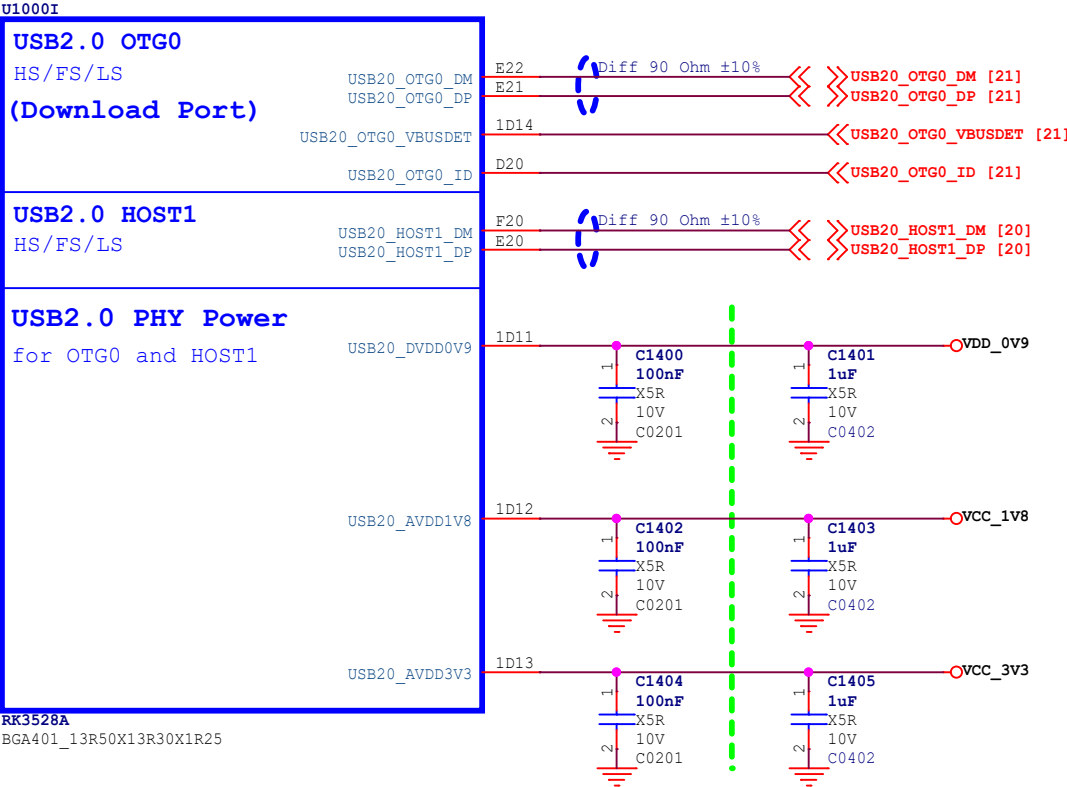
RK3528A_E (VCCIO1 Domain)



RK3528A_F (VCCIO2 Domain)

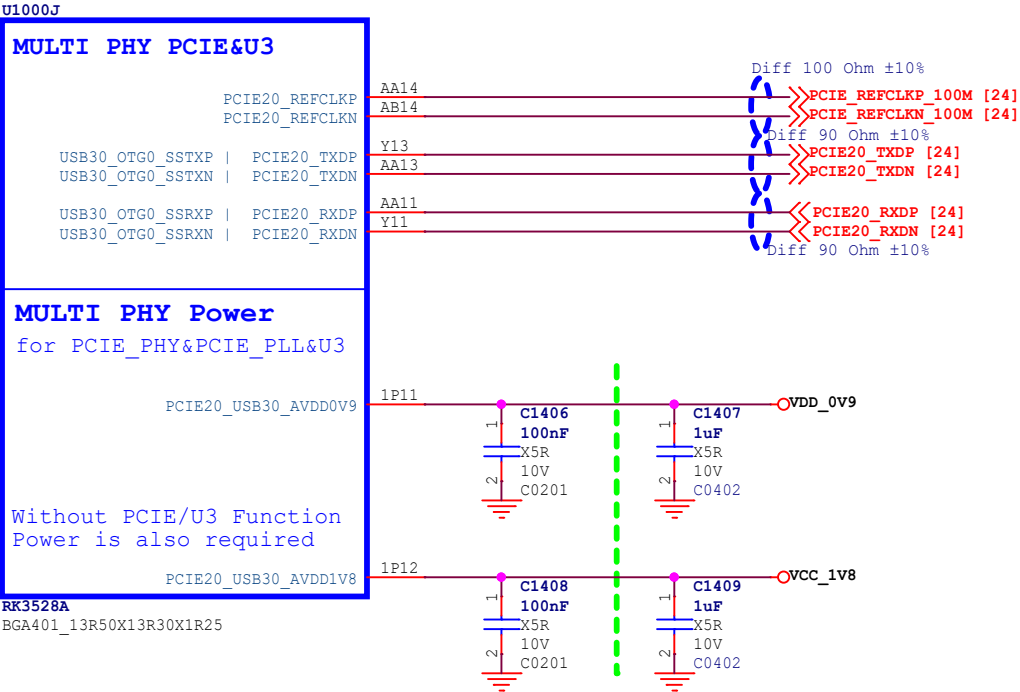


RK3528A_I (USB2.0 OTG/HOST)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

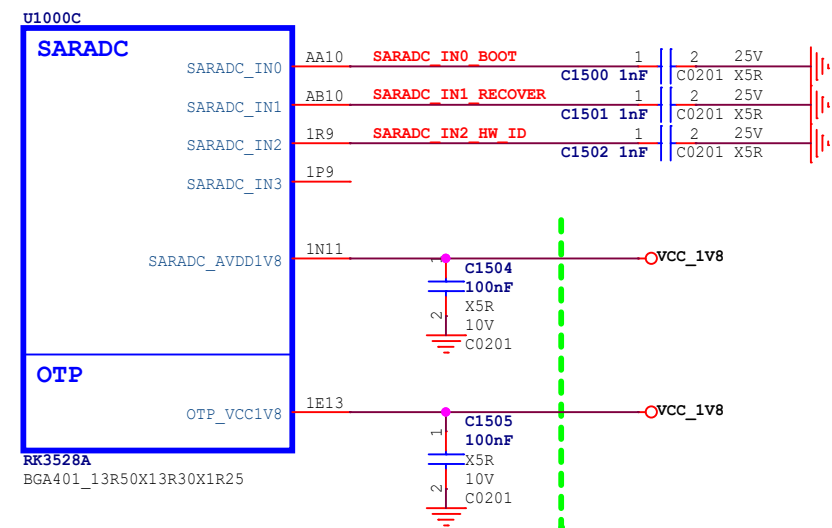
RK3528A_J (PCIE2.0/U3 PHY)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

 armsom		ArmSoM	
Project:	ArmSoM-SIGE1		
File:	10.RK3528A USB/PCIE Controller		
Date:	Saturday, July 27, 2024		Rev: V1.2
Designed by:	Liu Xinglin	Reviewed by: <Checker>	Sheet: 10 of 26

RK3528A_C (Saradc/OTP)

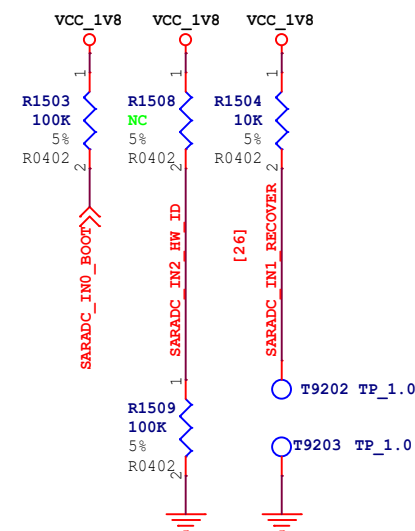


Note:

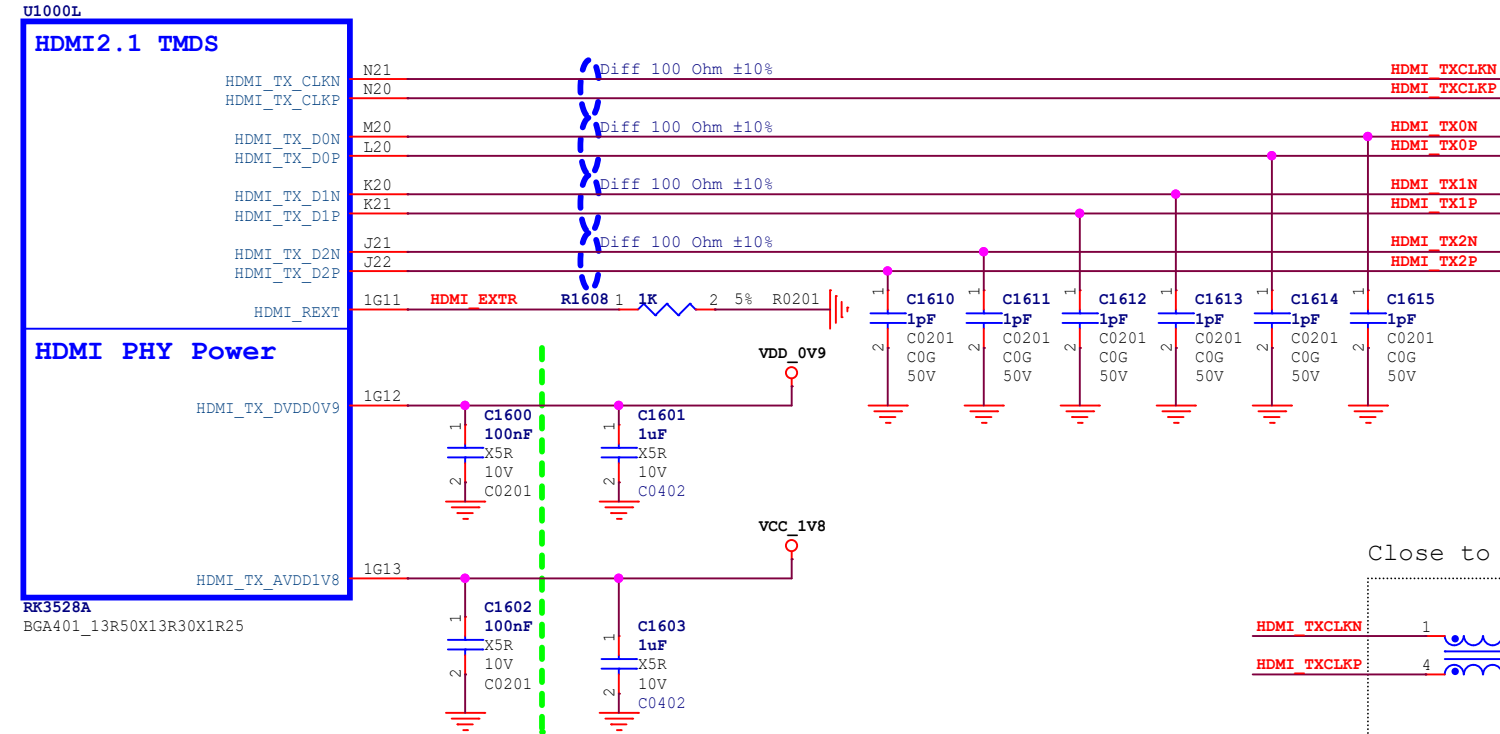
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

TABLE			
SARADC_IN2	Rup	Rdown	ADC
HW_ID0	DNP	100K	0
HW_ID1	100K	12K	114
HW_ID2	100K	27K	228
HW_ID3	100K	51K	342
HW_ID4	100K	82K	456
HW_ID5	100K	120K	570
HW_ID6	100K	200K	683
HW_ID7	100K	330K	796
HW_ID8	100K	820K	910
HW_ID9	100K	DNP	1023

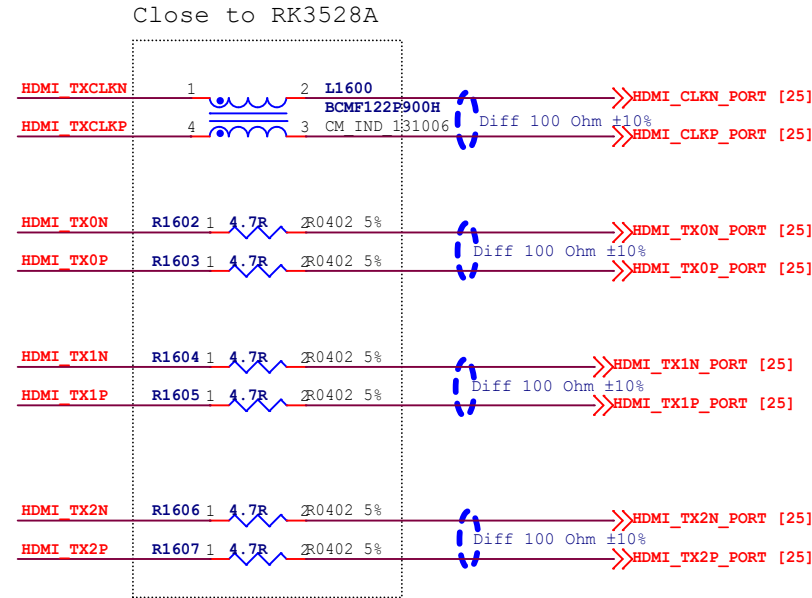
TABLE				
Item	Rup	Rdown	ADC	BOOT MODE
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	12K	114	
LEVEL3	100K	27K	228	FSPI--USB
LEVEL4	100K	51K	342	
LEVEL5	100K	82K	456	
LEVEL6	100K	120K	570	EMMC--USB
LEVEL7	100K	200K	683	EMMC--SD Card--USB
LEVEL8	100K	330K	796	SD Card--USB
LEVEL9	100K	820K	910	
LEVEL10	100K	DNP	1023	FSPI--EMMC--SD Card--USB



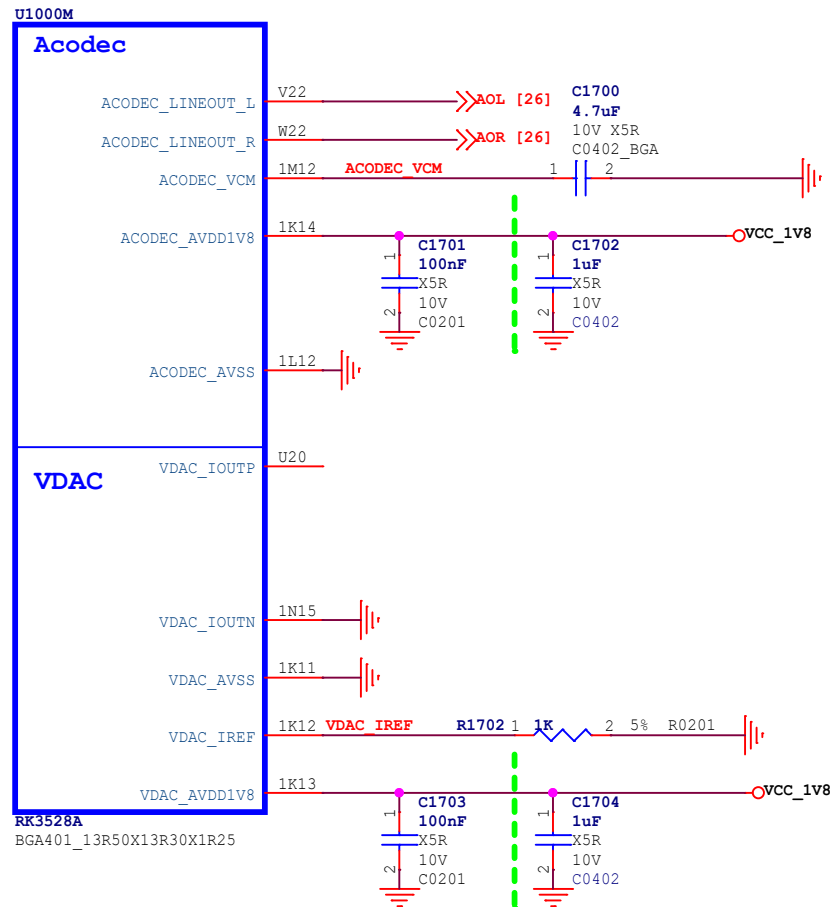
RK3528A_L (HDMI PHY)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



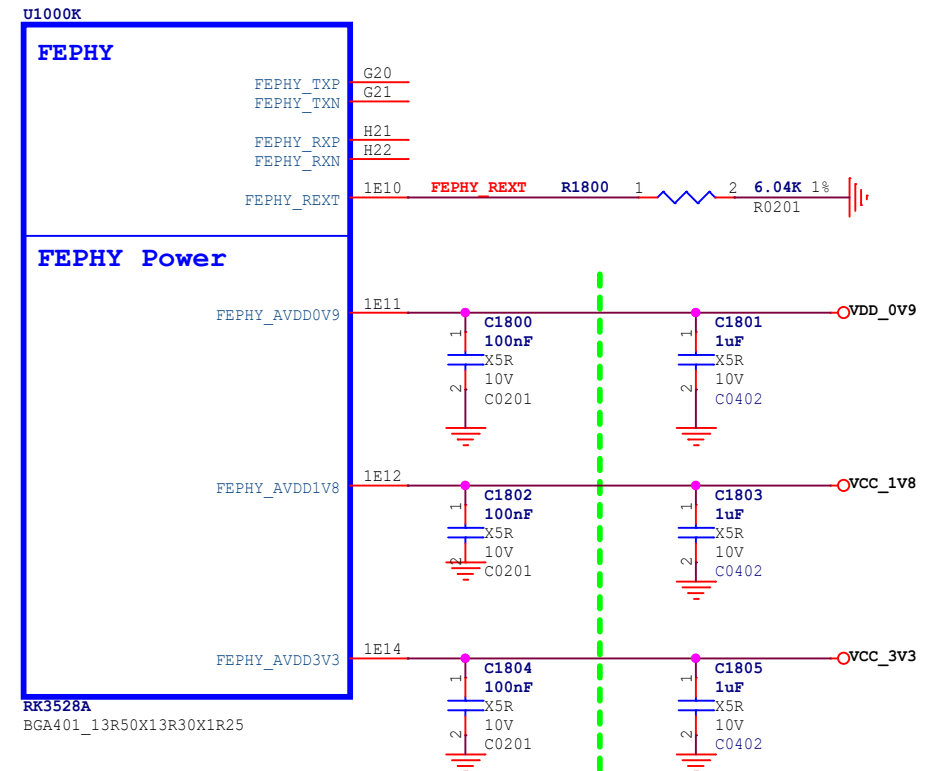
RK3528A_M (Acodec/VDAC)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3528A_K (Embed FEPHY)

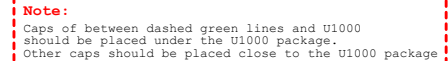
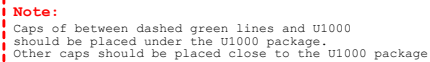


Note:

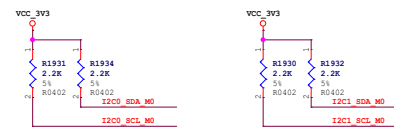
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

 armsom		ArmSoM	
Project:	ArmSoM-SIGE1		
File:	13.RK3528A AV OUT/EMBED_FEPHY		
Date:	Saturday, July 27, 2024		Rev: V1.2
Designed by:	Liu Xinglin	Reviewed by:	<Checker>
		Sheet:	13 of 26

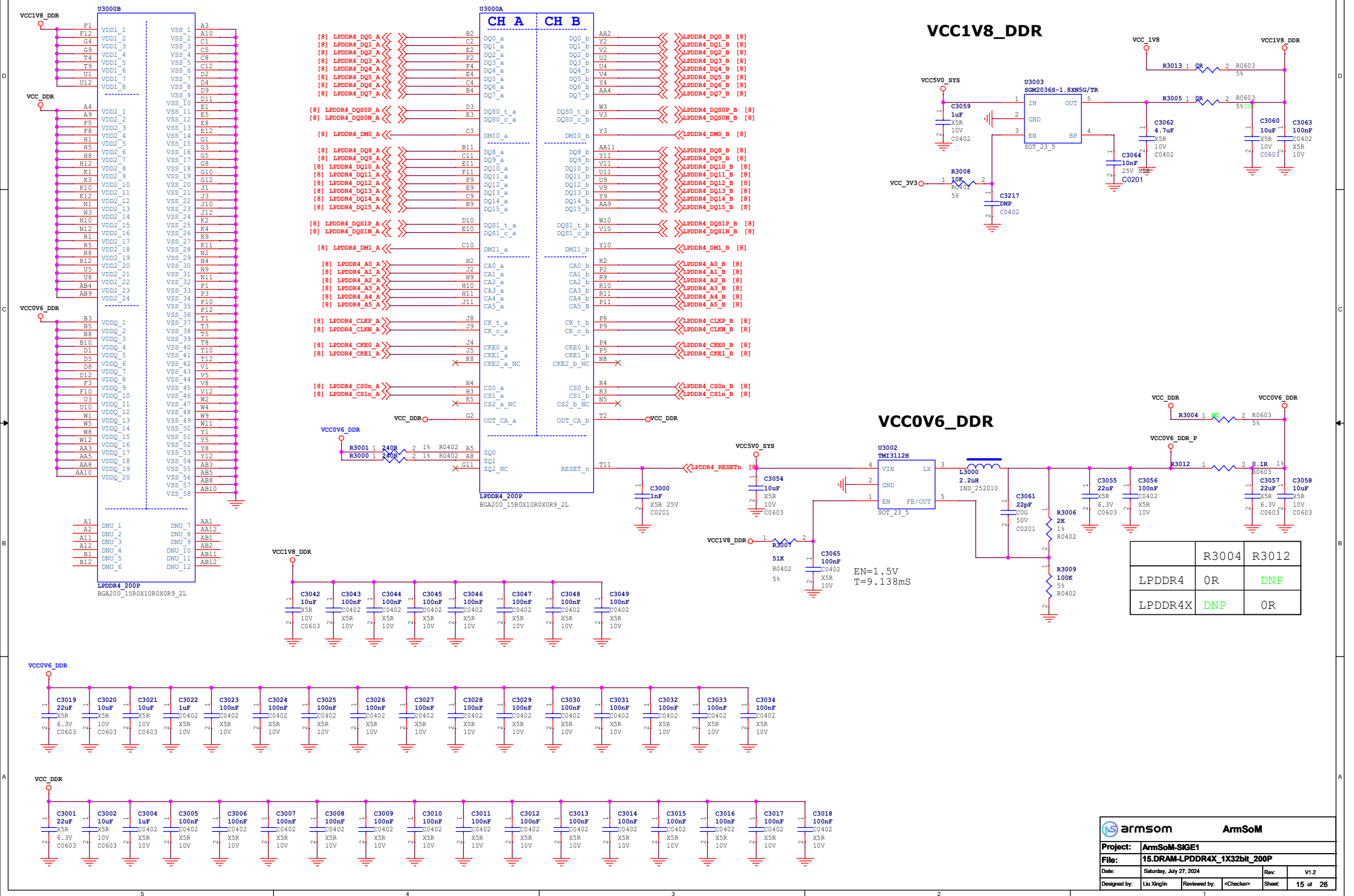
RK3528A G (VCCI03 Domain)



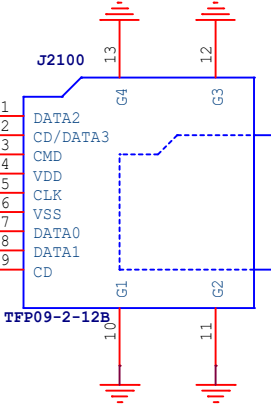
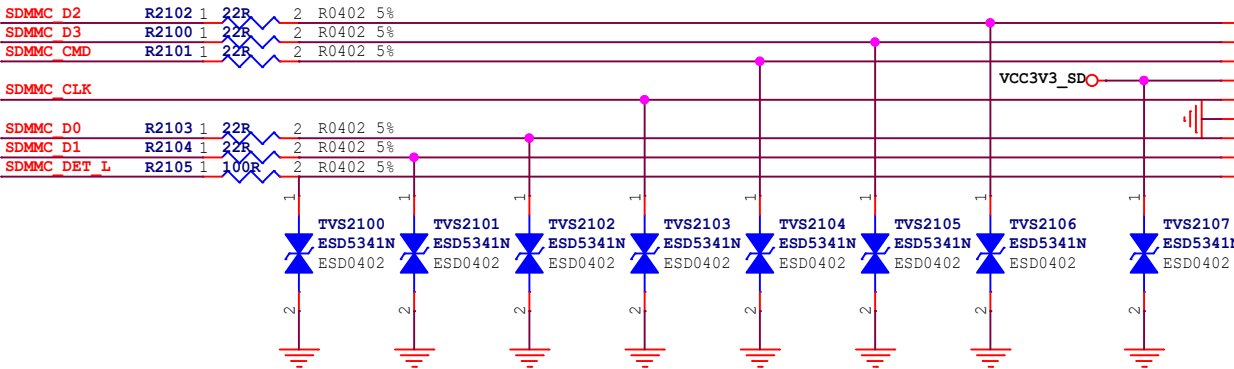
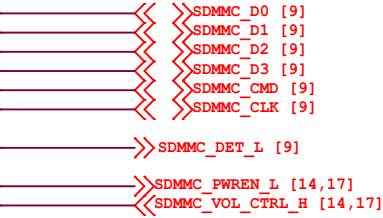
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



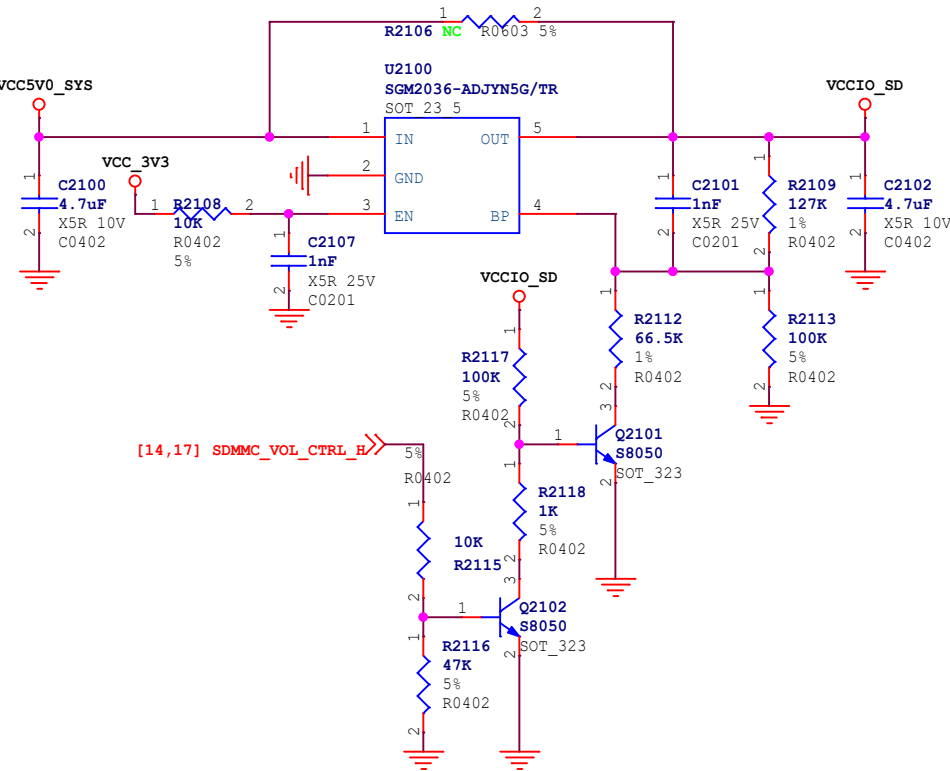
LPDDR4X 200Ba11



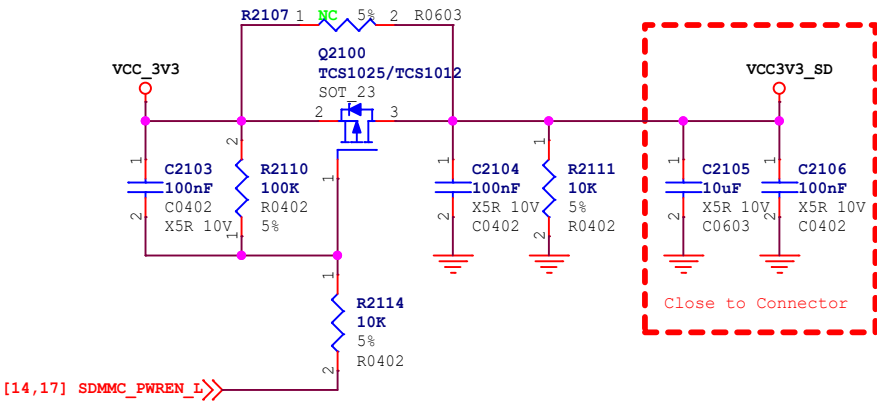
TF Card



VCCIO_SD



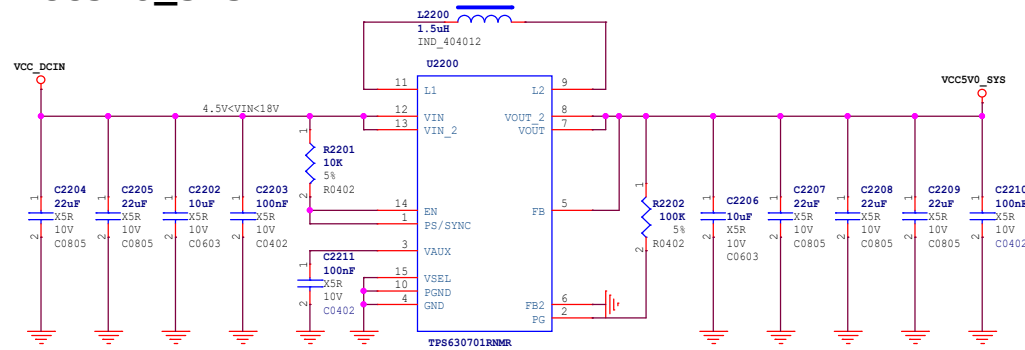
VCC3V3_SD



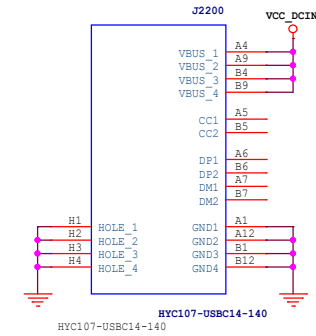
SDMMC_PWREN=L VCC_SD=3.3V(Default)
SDMMC_PWREN=H VCC_SD=0V

 armsom		ArmSoM	
Project:	ArmSoM-SIGE1		
File:	17.Flash-Micro-SD Card		
Date:	Saturday, July 27, 2024		Rev: V1.2
Designed by:	Liu Xinglin	Reviewed by: <Checker>	Sheet: 17 of 26

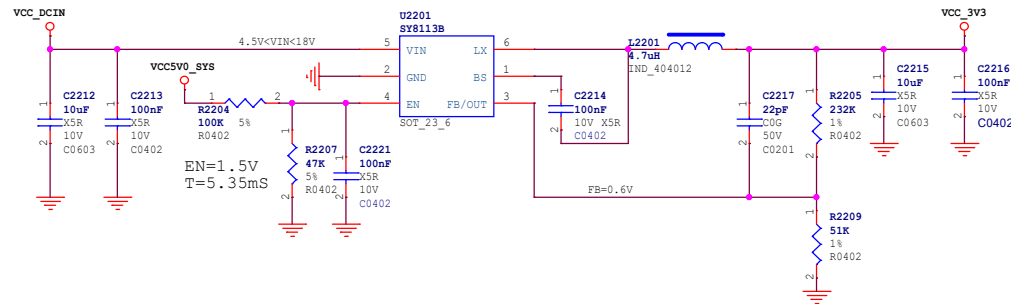
VCC5V0_SYS



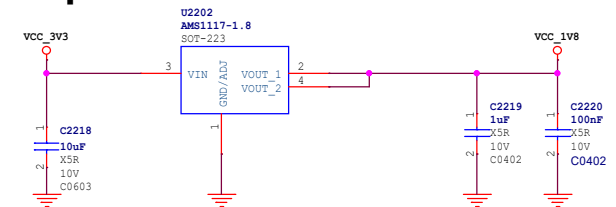
5V/3A DCIN



VCC5V0_SYS-->VCC_3V3 Step 2

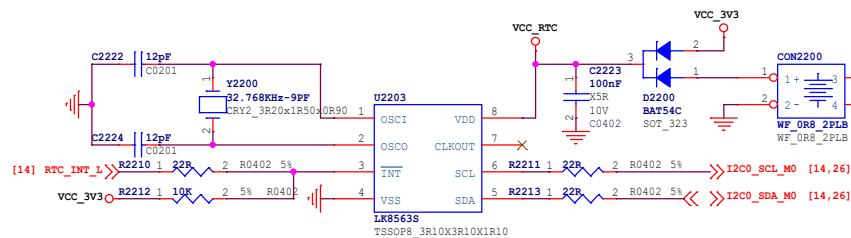


VCC_3V3->VCC_1V8(LDO) Step 2



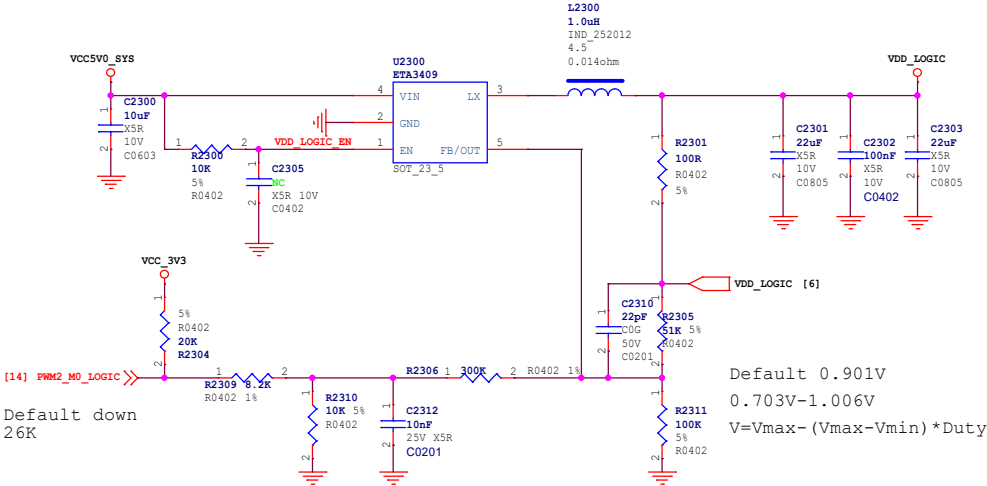
Note:
When LAYOUT, a star must be used,
Branch to each load

RTC IC

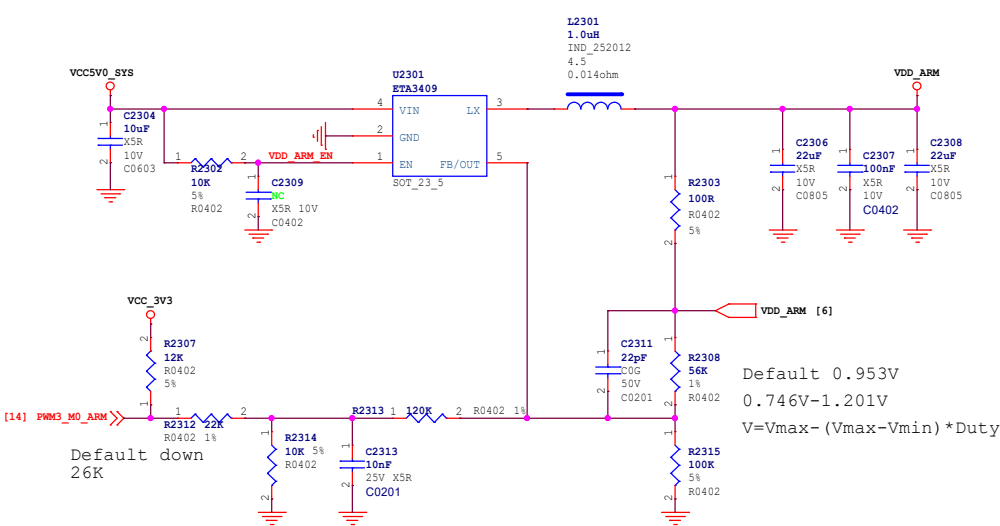


 armsom		ArmSoM	
Project:	ArmSoM-SIGE1		
File:	18.Power-DCIN		
Date:	Saturday, July 27, 2024		Rev: V1.2
Designed by:	Liu Xinglin	Reviewed by:	<Checker>
		Sheet:	18 of 26

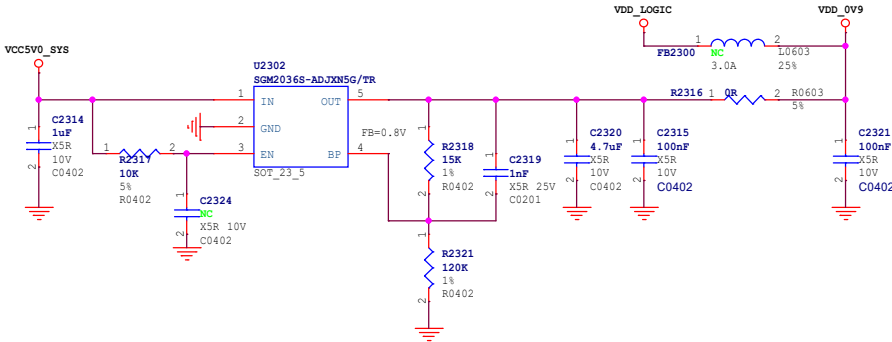
VCC5V0_SYS-->VDD_LOGIC
Step 1



VCC5V0_SYS-->VDD_ARM
Step 1

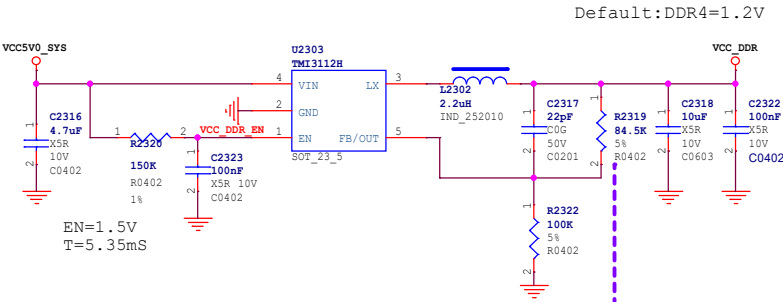


VCC5V0_SYS-->VDD_0V9
Step 1



Note:
When LAYOUT, a star must be used,
Branch to each load

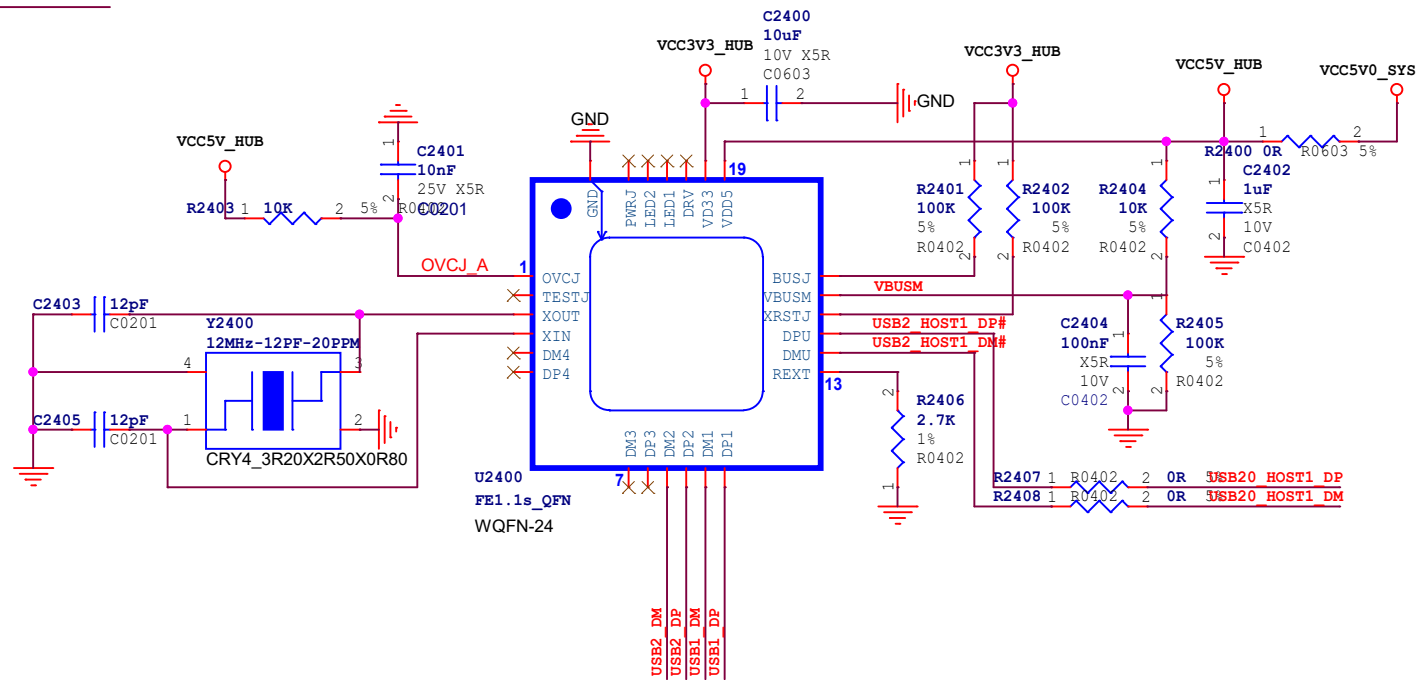
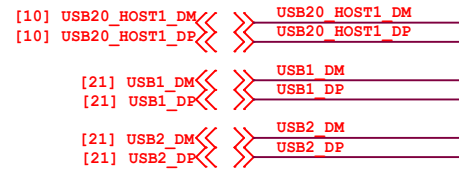
VCC5V0_SYS-->VCC_DDR
Step 2

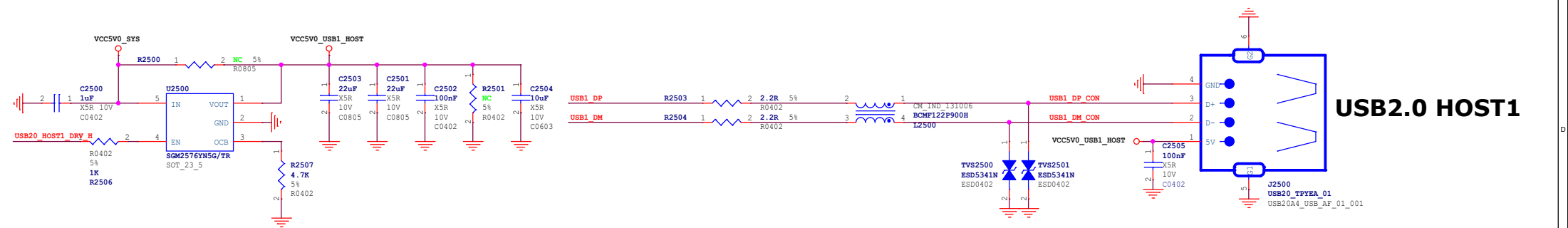


Default:DDR4=1.2V

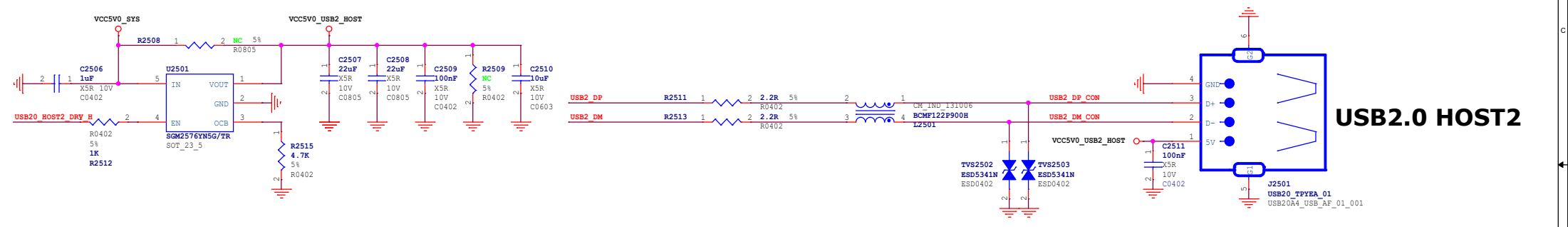
DDR4	1.20V	100K	1%
LPDDR4/4x	1.10V	84.5K	1%
DDR3	1.5V	150K	1%
DDR3L	1.35V	127K	1%
LPDDR3	1.25V	110K	1%

USB_HUB

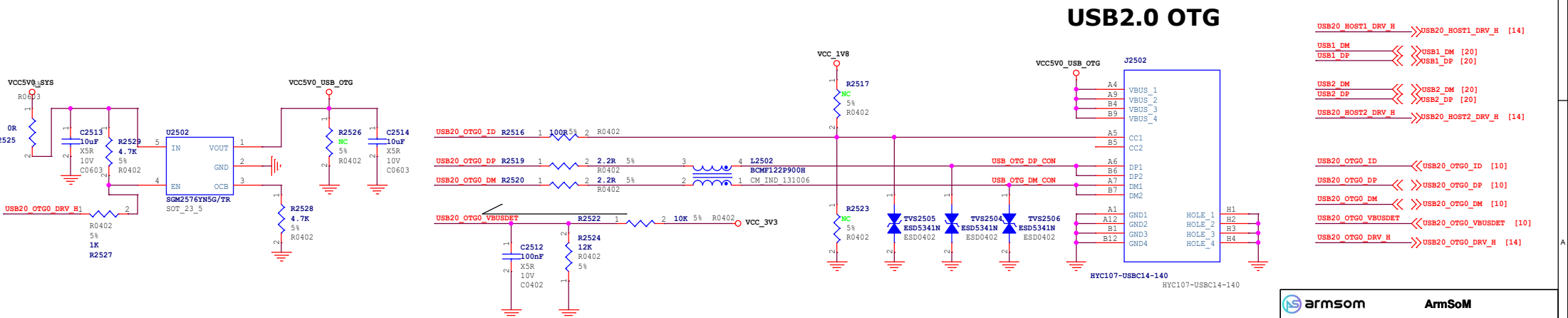




USB2.0 HOST1



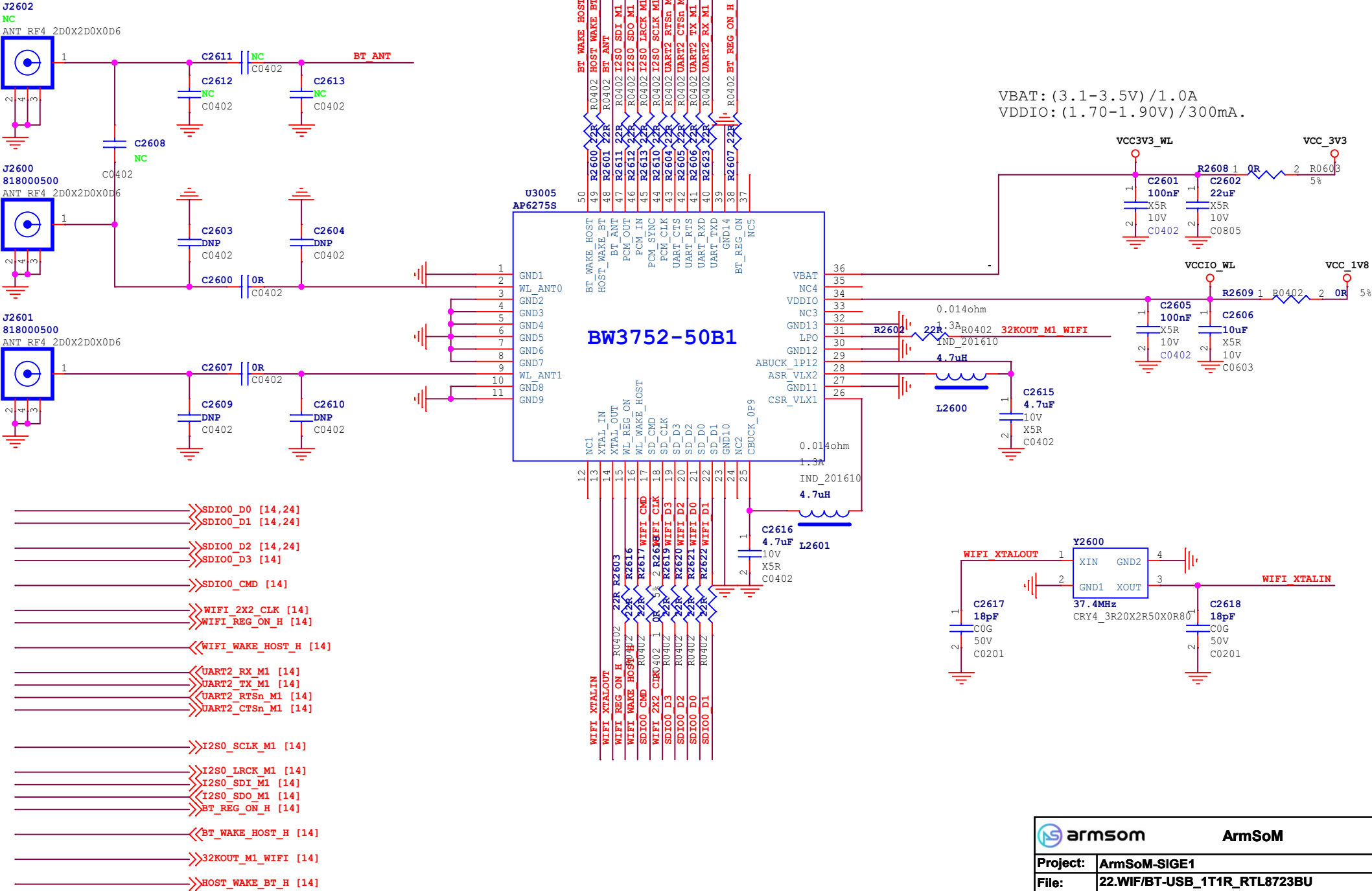
USB2.0 HOST2



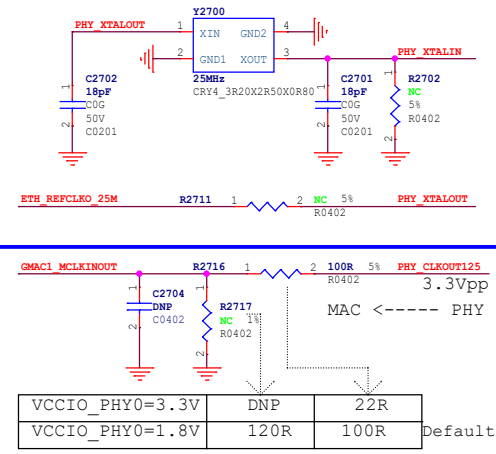
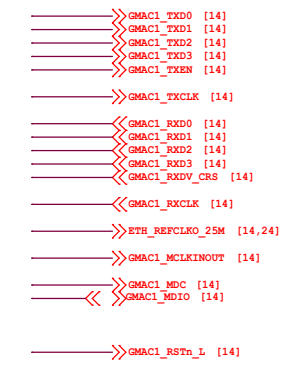
USB2.0 OTG

- USB20_HOST1_DRV_H >>> USB20_HOST1_DRV_H [14]
- USB1_DM >>> USB1_DM [20]
- USB1_DP >>> USB1_DP [20]
- USB2_DM >>> USB2_DM [20]
- USB2_DP >>> USB2_DP [20]
- USB20_HOST2_DRV_H >>> USB20_HOST2_DRV_H [14]
- USB20_OTG0_ID <<< USB20_OTG0_ID [10]
- USB20_OTG0_DP <<< USB20_OTG0_DP [10]
- USB20_OTG0_DM <<< USB20_OTG0_DM [10]
- USB20_OTG0_VBUSDET <<< USB20_OTG0_VBUSDET [10]
- USB20_OTG0_DRV_H >>> USB20_OTG0_DRV_H [14]

SDIO WIFI6/BT Module-2T2R

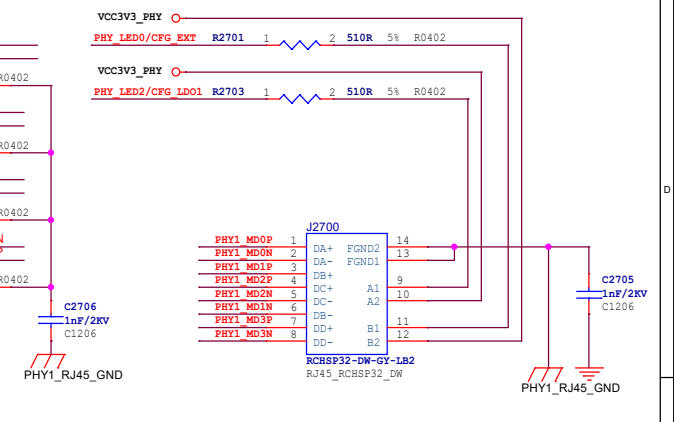
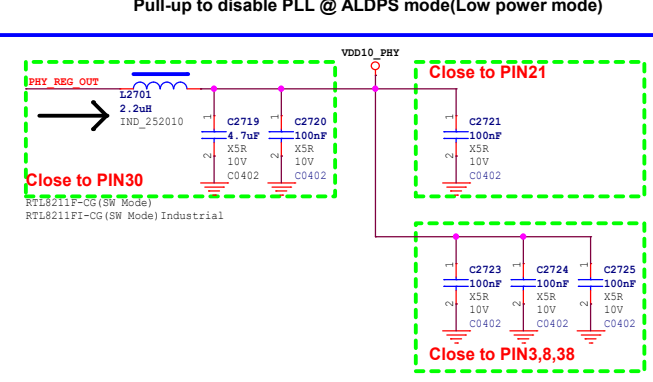
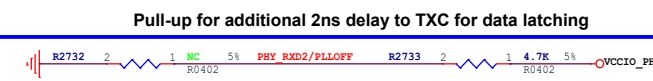
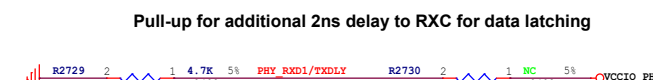
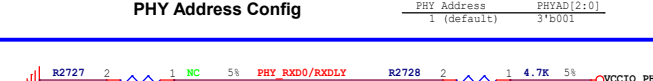
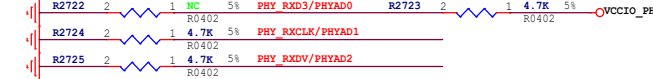
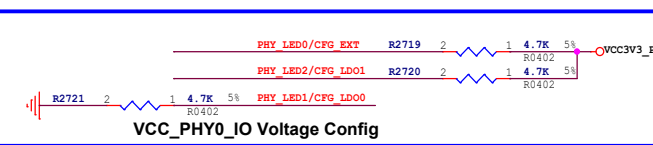
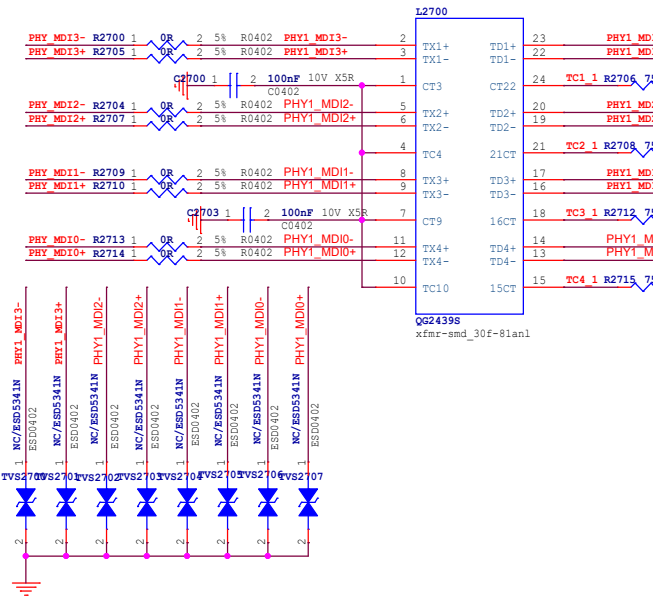
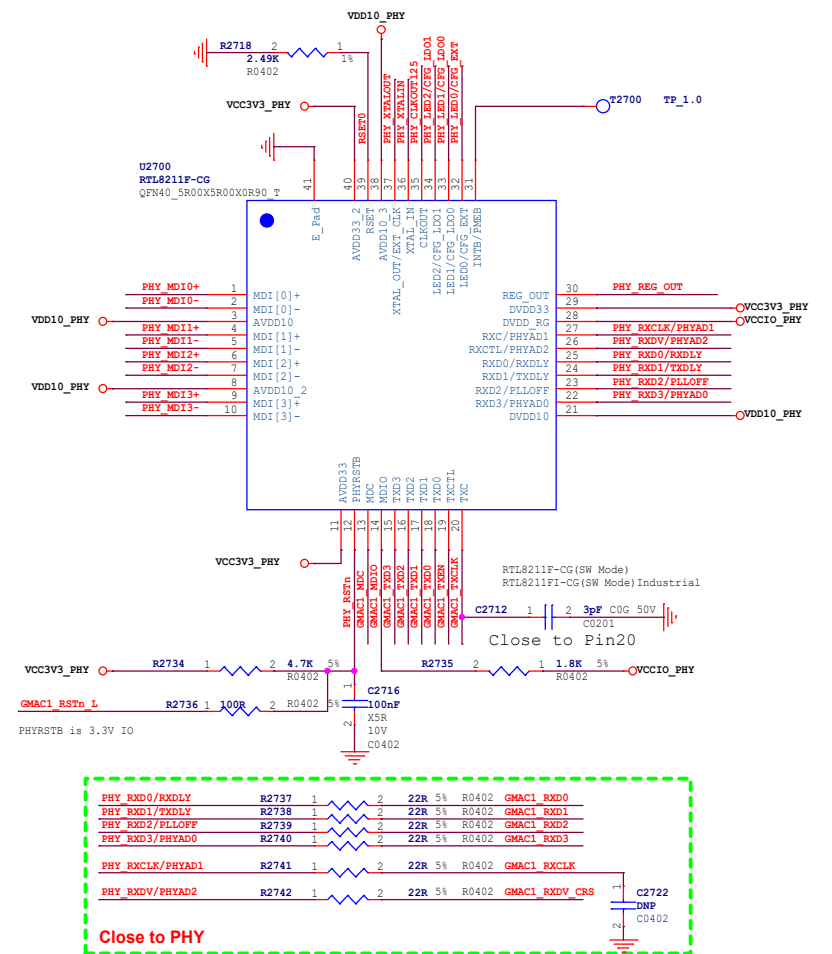


RGMII

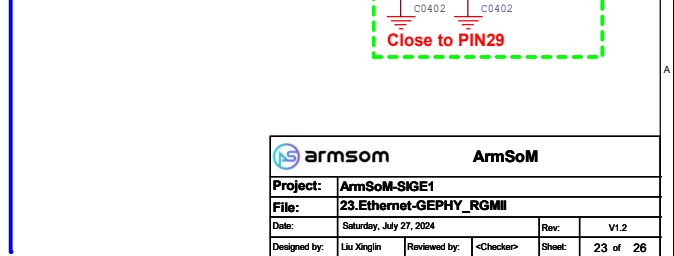
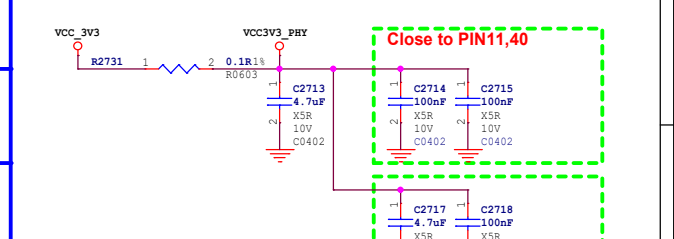
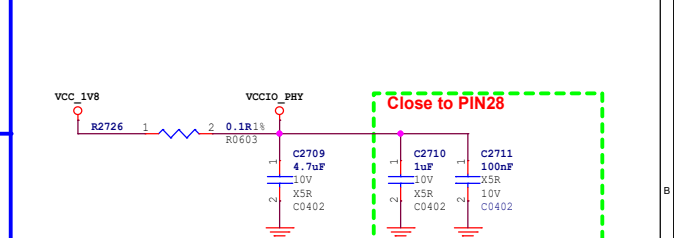
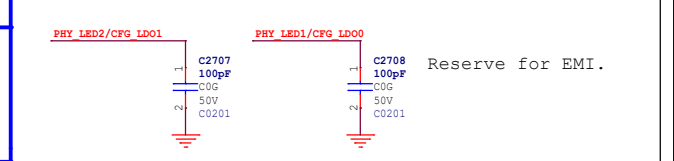


VCCIO_PHY0=3.3V	DNP	22R
VCCIO_PHY0=1.8V	120R	100R

Default



RGMII Power Source	CFG EXT	CFG LDO1[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V	1'b0	2'b10	

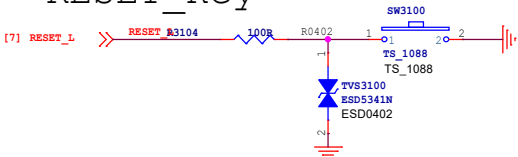


HOLE

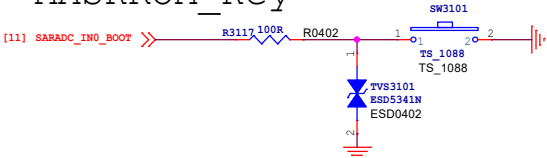


KEY

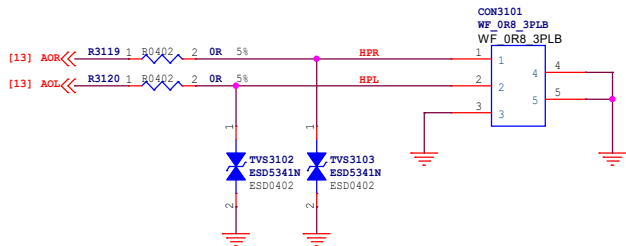
RESET_Key



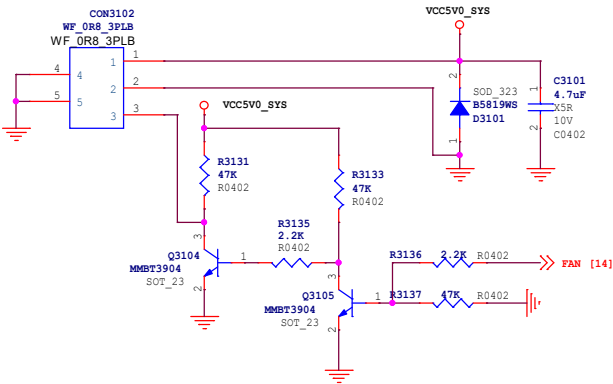
MASKROM_Key



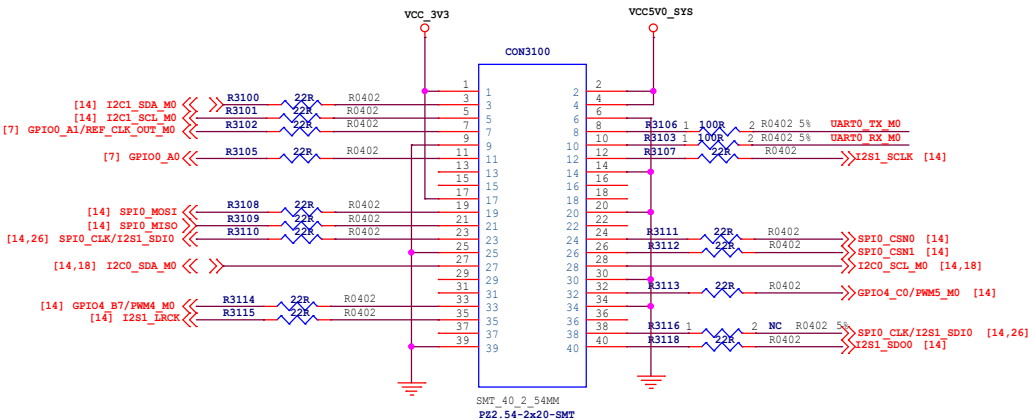
EARPHONE



FAN



40PIN_GPIO



RGB_LED

