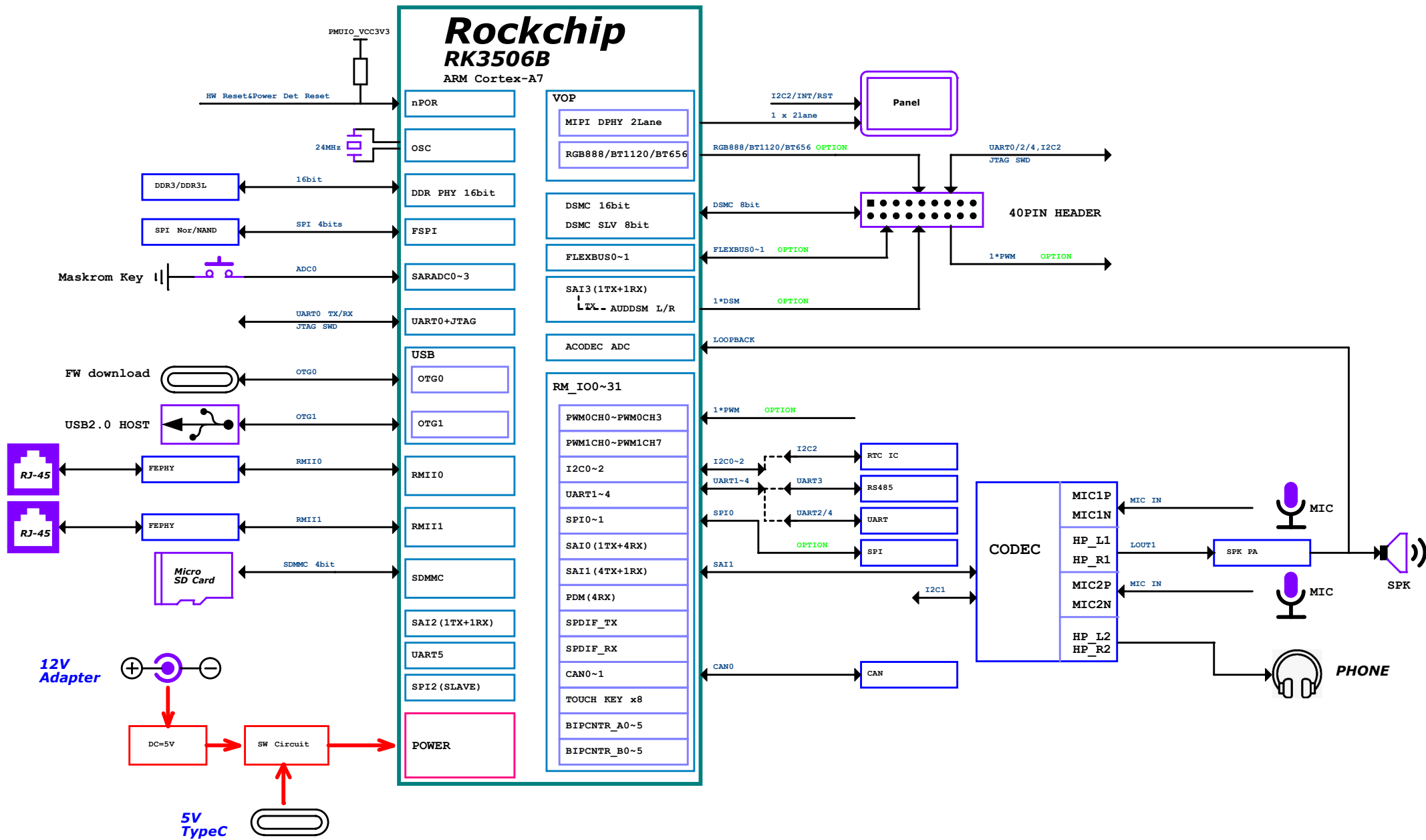
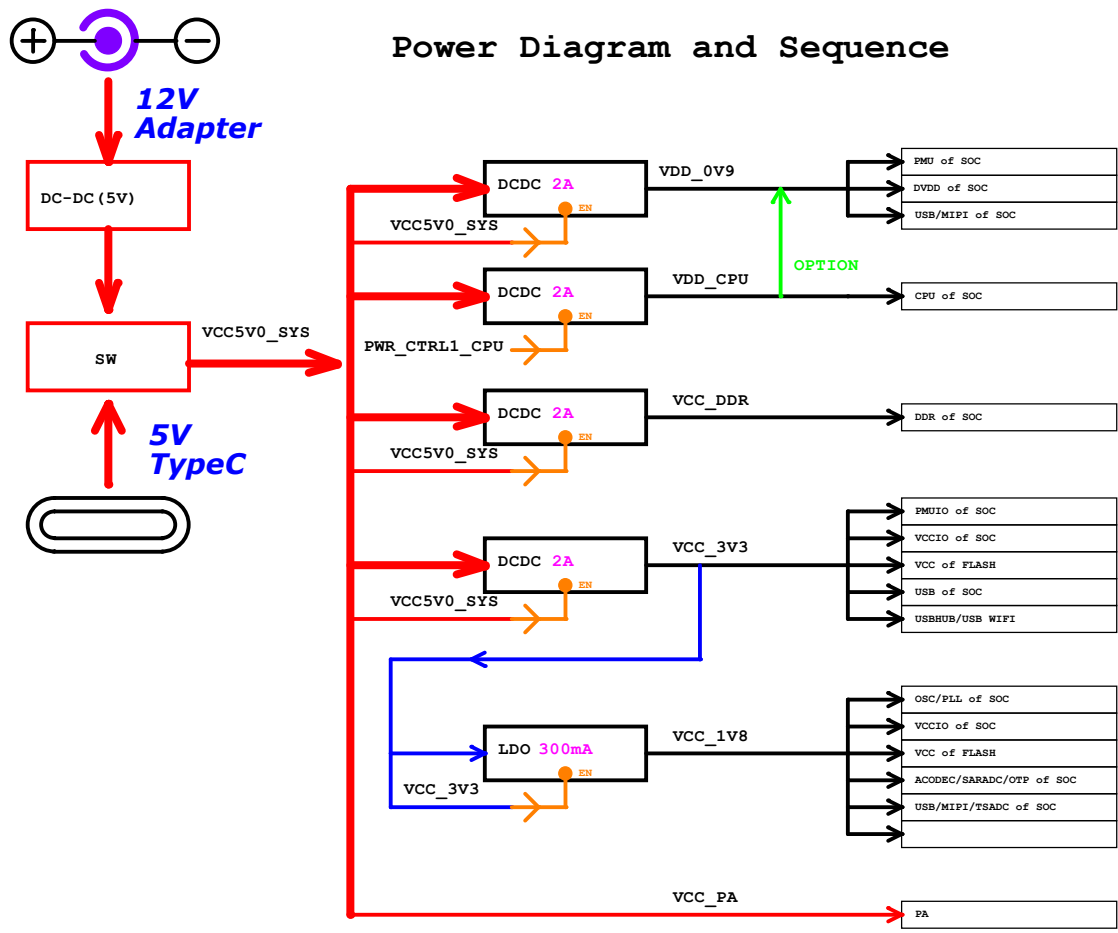


ArmSoM-FORGE1 Block Diagram

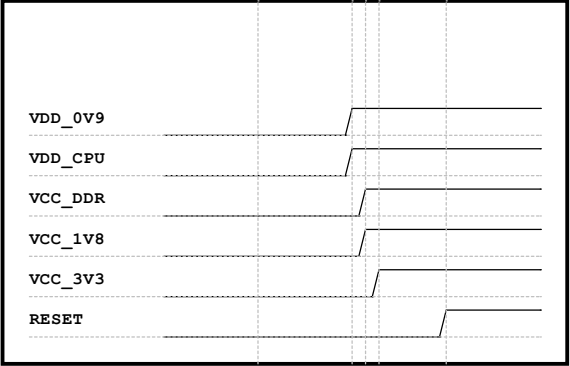
Rockchip IC

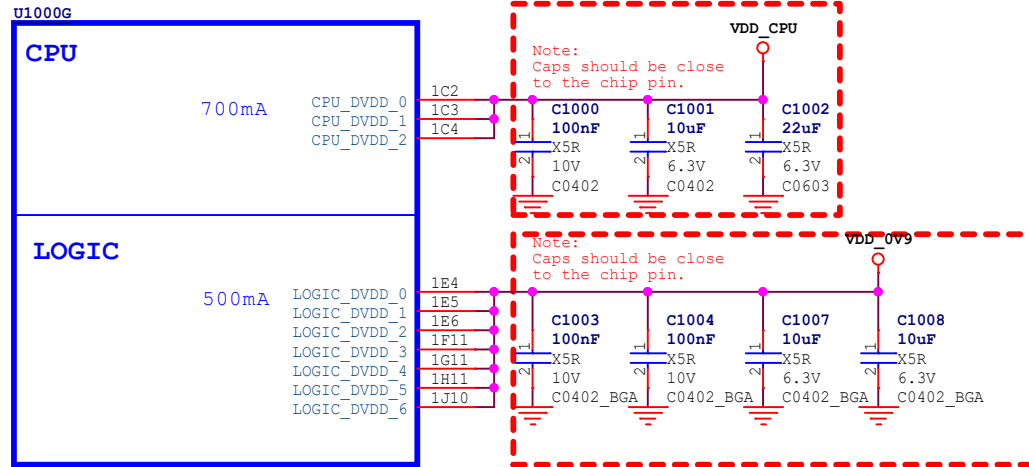
Other IC



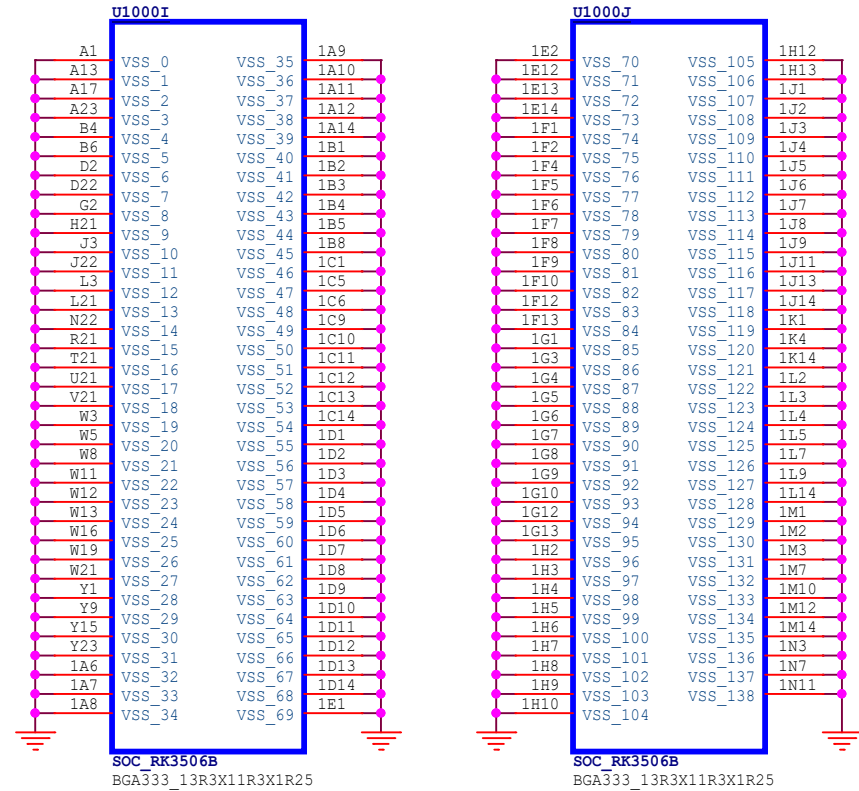


Power-on Sequence				
Power Name	PMIC Channel	Time Slot	Default voltage	Peak Current
VDD 0V9	DC-DC BUCK	Slot: 1	0.9V	
VDD CPU	DC-DC BUCK	Slot: 1	0.95V	
VCC DDR	DC-DC BUCK	Slot: 2	1.35V	
VCC 1V8	LDO	Slot: 2a	1.8V	
VCC 3V3	DC-DC BUCK	Slot: 3	3.3V	
RESET				
Finally , nPOR RESET 10ms after PMUIO VCC3V3 is ready				





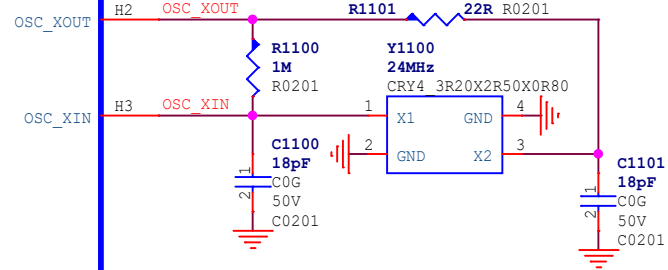
SOC_RK3506B
BGA333_13R3X11R3X1R25



U1000A

OSC/PLL

Operating Voltage=1.8V Only



REF_CLK0_OUT/OSC_CLK_OUT/GPIO0_D0_d

RFU

20mA SYS_PLL_AVDD1V8

PMUIO Domain

Operating Voltage=3.3V Only



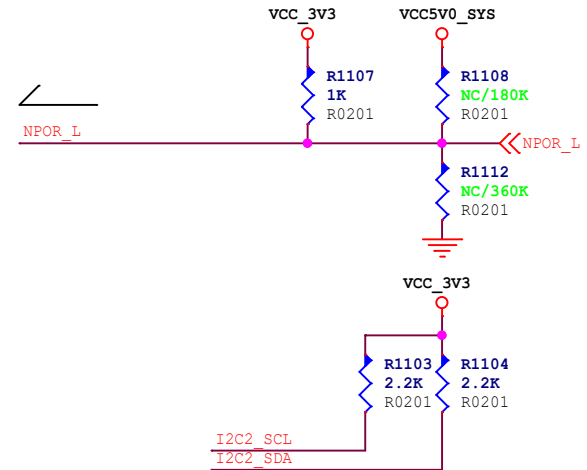
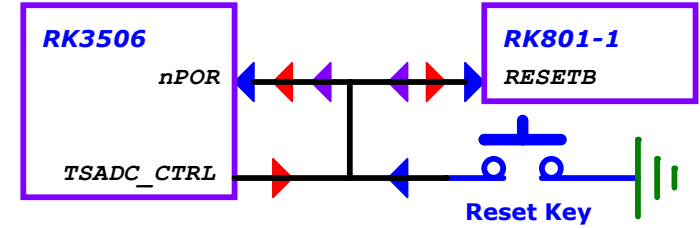
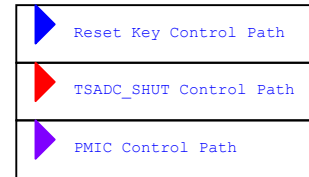
200mA PMU_LOGIC_VDD0V9

PMUIO_VCC3V3

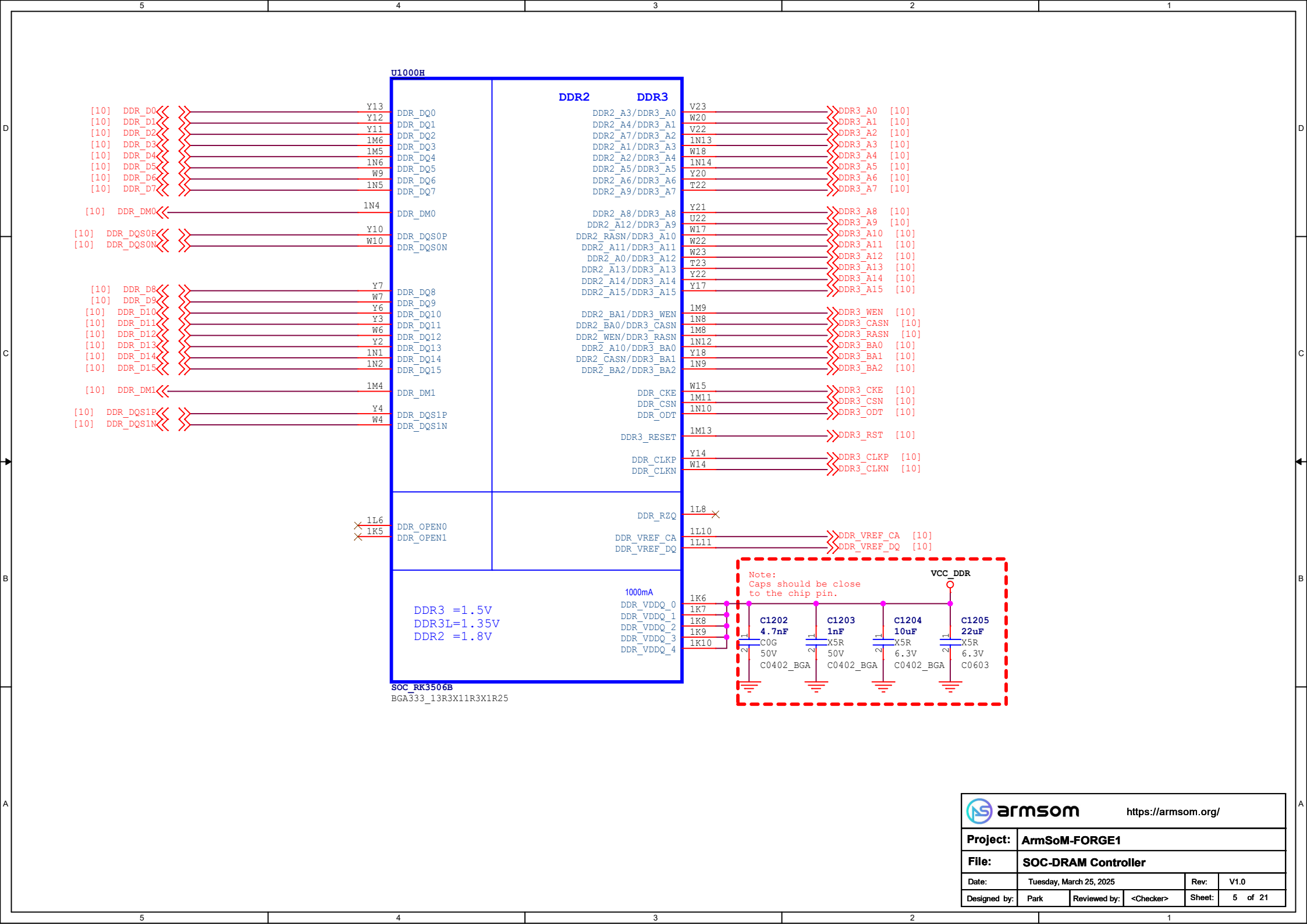
SOC RK3506B

BGA333_13R3X11R3X1R25

Note:



		https://armsom.org/	
Project:	ArmSoM-FORGE1		
File:	SOC-OSC/PLL/PMUIO		
Date:	Tuesday, March 25, 2025		Rev: V1.0
Designed by:	Park	Reviewed by: <Checker>	Sheet: 4 of 21



<https://armsom.org/>

Project: ArmSoM-FORGE1			
File: SOC-DRAM Controller			
Date:	Tuesday, March 25, 2025	Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>
Sheet:	5	of	21

U1000C

VCCIO2 Domain

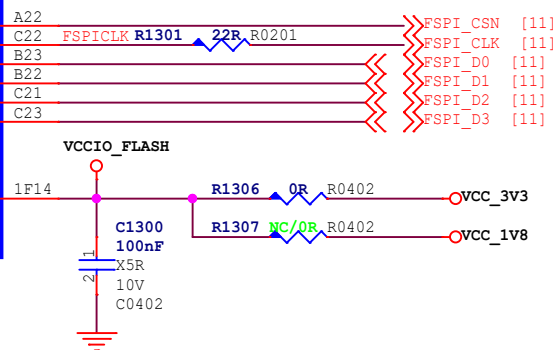
Operating Voltage=1.8V/3.3V

FSPI_CSN/GPIO2_A0_u
FSPI_CLK/GPIO2_A1_d
FSPI_D0/GPIO2_A2_u
FSPI_D1/GPIO2_A3_u
FSPI_D2/GPIO2_A4_u
FSPI_D3/GPIO2_A5_u

VCCIO2_VCC

SOC_RK3506B

BGA333_13R3X11R3X1R25



 armsom		https://armsom.org/	
Project:	ArmSoM-FORGE1		
File:	SOC-Flash Controller		
Date:	Tuesday, March 25, 2025		Rev: V1.0
Designed by:	Park	Reviewed by: <Checker>	Sheet: 6 of 21

U1000F

MIPI

Operating Voltage=1.8V
GPO is output only

MIPI_DPHY_DSI_TX_D0N/GPO4_A0_z
MIPI_DPHY_DSI_TX_D0P/GPO4_A1_z
MIPI_DPHY_DSI_TX_D1N/GPO4_A2_z
MIPI_DPHY_DSI_TX_D1P/GPO4_A3_z
MIPI_DPHY_DSI_TX_CLKN/GPO4_A4_z
MIPI_DPHY_DSI_TX_CLKP/GPO4_A5_z

20mA MIPI_DPHY_AVDD0V9
50mA MIPI_DPHY_AVDD1V8

USB2.0 OTG0

HS/FS/LS
(Download Port)

USB20_OTG0_DP [14]
USB20_OTG0_DM [14]
USB20_OTG0_ID [14]
USB20_OTG0_VBUSDET [14]

USB2.0 OTG1

HS/FS/LS

USB20_OTG1_DP [14]
USB20_OTG1_DM [14]

USB2.0 PHY Power for OTG0/1

5mA USB20_OTG_AVDD0V9
30mA USB20_OTG_AVDD1V8
10mA USB20_OTG_AVDD3V3

SARADC

Operating Voltage=1.8V

SARADC_IN0/GPIO4_B0_z
SARADC_IN1/GPIO4_B1_z
SARADC_IN2/GPIO4_B2_z
SARADC_IN3/GPIO4_B3_z

60mA OTP_AVDD1V8/SARADC_AVDD1V8

TSADC

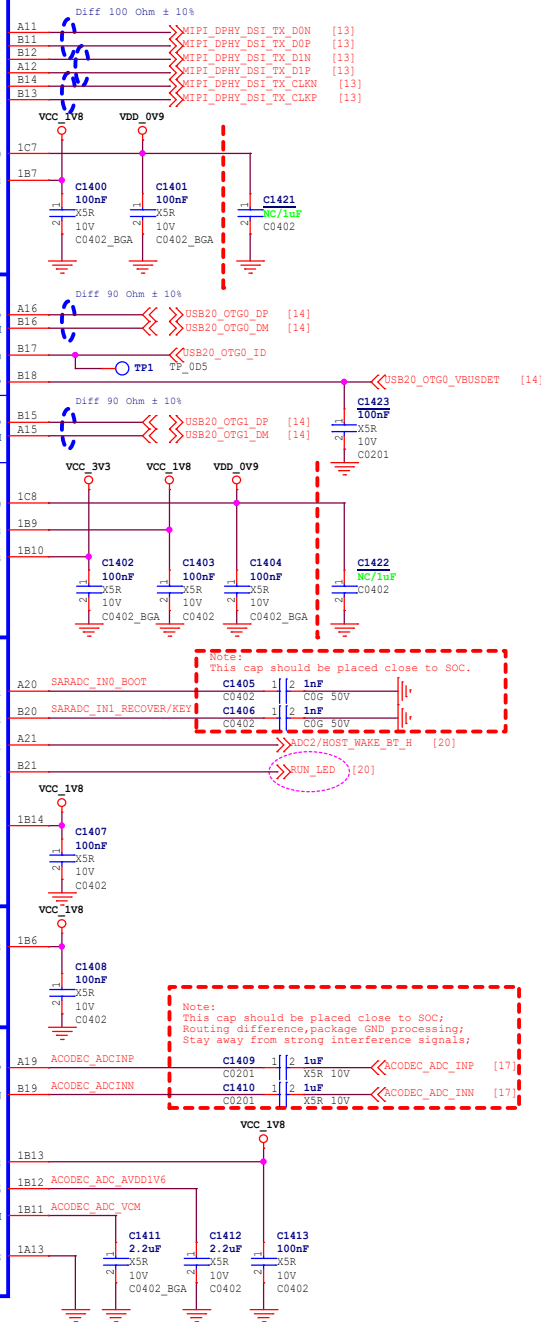
1.5mA TSADC_VCC1V8

ACODEC

ACODEC_ADC_INP [17]
ACODEC_ADC_INN [17]

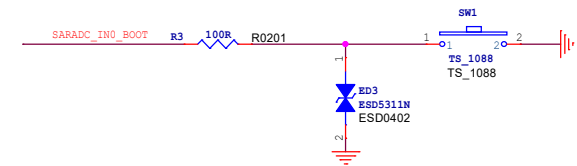
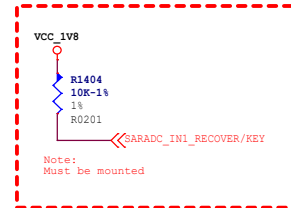
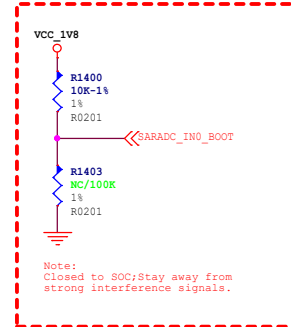
10mA ACODEC_ADC_AVDD1V8
ACODEC_ADC_AVDD1V6
ACODEC_ADC_VCM
ACODEC_ADC_AVSS

SOC_RK3506B
BGA333_13R3X11R3X1R25



SARADC_IN0_BOOT TABLE

Item	Rup	Rdown	ADC	BOOT MODE
LEVEL1	DNP	100K	0	USB (Maskrom mode)/SPI2APB
LEVEL2	100K	12K	110	SPI2APB
LEVEL3	100K	27K	217	FSPI--USB/SPI2APB
LEVEL4	100K	51K	345	
LEVEL5	100K	82K	461	
LEVEL6	100K	120K	558	SDMMC(eMMC/SD Card)--USB/SPI2APB
LEVEL7	100K	200K	682	
LEVEL8	100K	330K	785	
LEVEL9	100K	820K	912	
LEVEL10	10K	DNP	1023	FSPI--SDMMC(eMMC/SD Card)--USB/SPI2APB



VCCIO1 Domain

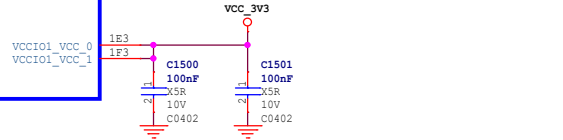
Operating Voltage=1.8V/3.3V

FLEXBUS1_D0/DSMC_CLKP/VO_LCDC_DEN/GPI01_A0_d B10
DSMC_SLV_INT/DSMC_INT0/FLEXBUS1_D1/DSMC_CLKN/VO_LCDC_VSYNC/GPI01_A1_d 1A5
FLEXBUS1_D2/DSMC_DQ00/VO_LCDC_HSYNC/GPI01_A2_d A9
FLEXBUS1_D3/DSMC_D0/VO_LCDC_CLK/GPI01_A3_d B9
FLEXBUS1_D4/DSMC_D1/VO_LCDC_D23/GPI01_A4_d B8
FLEXBUS1_D5/DSMC_D2/VO_LCDC_D22/GPI01_A5_d 1A4
FLEXBUS1_D6/DSMC_D3/VO_LCDC_D21/GPI01_A6_d A7
FLEXBUS1_D7/DSMC_D4/VO_LCDC_D20/GPI01_A7_d B7
FLEXBUS0_CSN_M0/FLEXBUS1_D8/DSMC_D5/VO_LCDC_D19/GPI01_B0_d 1A3
RM_IO24/UART5_CTSN_M1/FLEXBUS1_CSN_M0/FLEXBUS1_D9/DSMC_CSN1/VO_LCDC_D18/GPI01_B1_d 1A2
RM_IO25/SAI2_SCLK_M1/FLEXBUS0_CSN_M1/FLEXBUS0_D15/FLEXBUS1_D10/DSMC_INT2/VO_LCDC_D17/GPI01_B2_d A5
RM_IO26/SAI2_LCK_M1/FLEXBUS1_CSN_M1/FLEXBUS0_D14/FLEXBUS1_D11/DSMC_INT3/VO_LCDC_D16/GPI01_B3_d B5
FLEXBUS0_CSN_M2/FLEXBUS0_D13/FLEXBUS1_D12/DSMC_D6/VO_LCDC_D15/GPI01_B4_d 1A1
FLEXBUS1_CSN_M2/FLEXBUS0_D12/FLEXBUS1_D13/DSMC_D7/VO_LCDC_D14/GPI01_B5_d C3
FLEXBUS0_CSN_M3/FLEXBUS0_D11/FLEXBUS1_D14/DSMC_CSN0/VO_LCDC_D13/GPI01_B6_d A3
FLEXBUS1_CSN_M3/FLEXBUS0_D10/FLEXBUS1_D15/DSMC_RDYN/VO_LCDC_D1/GPI01_B7_d B3
DSMC_SLV_CLK/FLEXBUS0_CSN_M4/DSMC_INT1/FLEXBUS1_CLK/DSMC_RESETN/VO_LCDC_D11/GPI01_C0_d A2
DSMC_SLV_DQ00/SAI2_MCLK_M1/FLEXBUS1_CSN_M4/DSM_AUD_RM_M0/FLEXBUS0_CLK/DSMC_D8/VO_LCDC_D10/GPI01_C1_d B2
DSMC_SLV_D0/RM_IO27/SAI2_SDI_M1/FLEXBUS0_CSN_M5/DSM_AUD_RM_M0/FLEXBUS0_D9/VO_LCDC_D9/GPI01_C2_d B1
DSMC_SLV_D1/RM_IO28/SAI2_SDO_M1/FLEXBUS1_CSN_M5/FLEXBUS0_D8/DSMC_D10/VO_LCDC_D8/GPI01_C3_d C2
DSMC_SLV_D2/FLEXBUS0_D7/DSMC_D11/VO_LCDC_D7/GPI01_C4_d C1
DSMC_SLV_D3/FLEXBUS0_D6/DSMC_D12/VO_LCDC_D6/GPI01_C5_d D3
DSMC_SLV_D4/FLEXBUS0_D5/DSMC_D13/VO_LCDC_D5/GPI01_C6_d E3
DSMC_SLV_D5/FLEXBUS0_D4/DSMC_D14/VO_LCDC_D4/GPI01_C7_d E2
DSMC_SLV_D6/DSM_AUD_LN_M0/FLEXBUS0_D3/DSMC_D15/VO_LCDC_D3/GPI01_D0_d E1
DSMC_SLV_D7/RM_IO29/UART5_RTSN_M1/DSM_AUD_LP_M0/FLEXBUS0_D2/DSMC_DQ01/VO_LCDC_D2/GPI01_D1_d F3
DSMC_SLV_CSN0/RM_IO30/UART5_TX_M1/FLEXBUS0_D1/DSMC_CSN2/VO_LCDC_D1/GPI01_D2_d F2
DSMC_SLV_RDYN/RM_IO31/UART5_RX_M1/FLEXBUS0_D0/DSMC_CSN3/VO_LCDC_D0/GPI01_D3_d G3

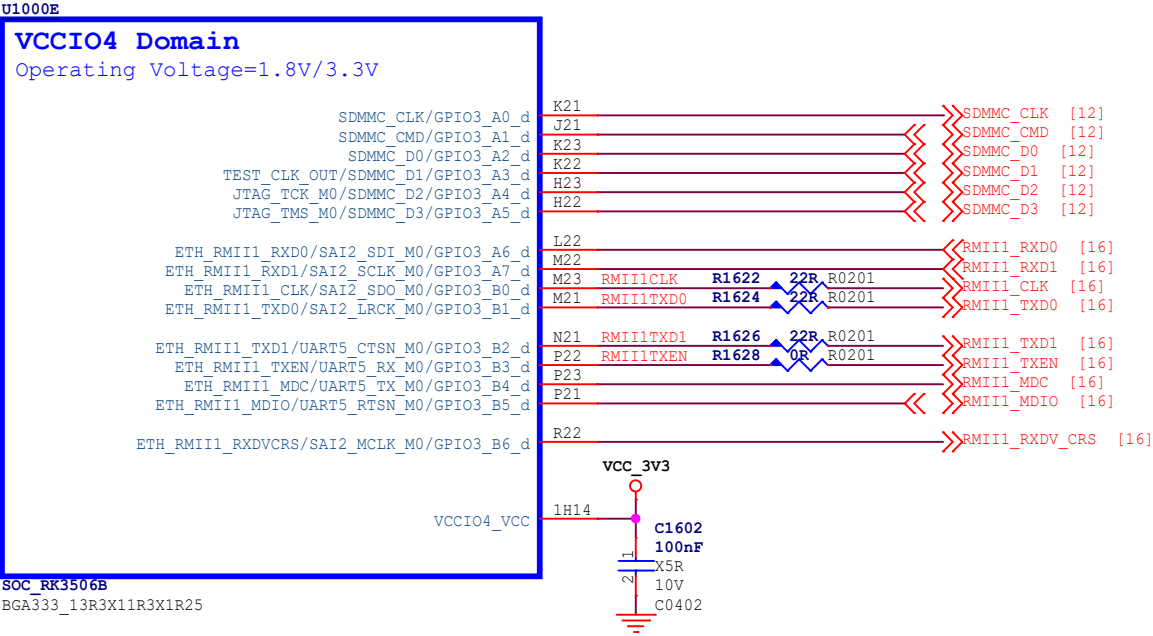
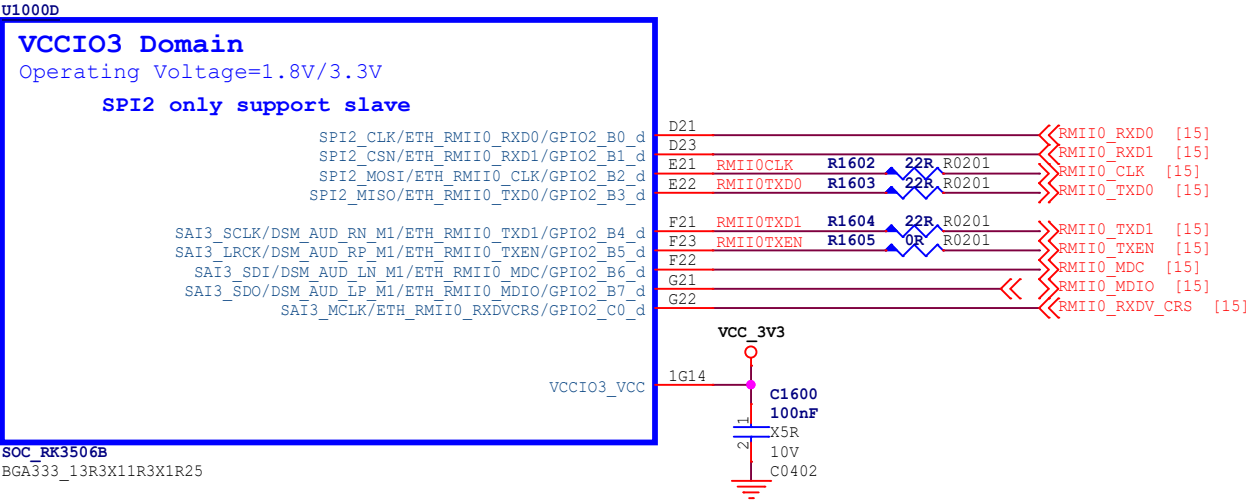
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CAN1_TX/FLEXBUS1_D10 [20]
CAN1_RX/FLEXBUS1_D11 [20]
DSMC_D6/FLEXBUS1_D12 [20]
DSMC_D7/FLEXBUS1_D13 [20]
DSMC_CSN0/FLEXBUS1_D14 [20]
DSMC_RDYN/FLEXBUS1_D15 [20]
DSMC_RESETN/FLEXBUS1_CLK [20]
GPI01_C1/DSM_AUD_RM [20]
GPI01_C2/DSM_AUD_RM [20]
GPI01_C3/MIP1_DPHY_DSI_TE [20]
GPI01_C4/USB20_OTG0_DRV_H [20]
GPI01_C5/WIFI_REG_ON_H [20]
DSMC_CTSN [17]
RMII1_RStn [16]
USB20_OTG1_DRV_H [14]
UART4_RTSN [20]
UART4_RX [20]
UART4_TX [20]

SOC_RK3506B

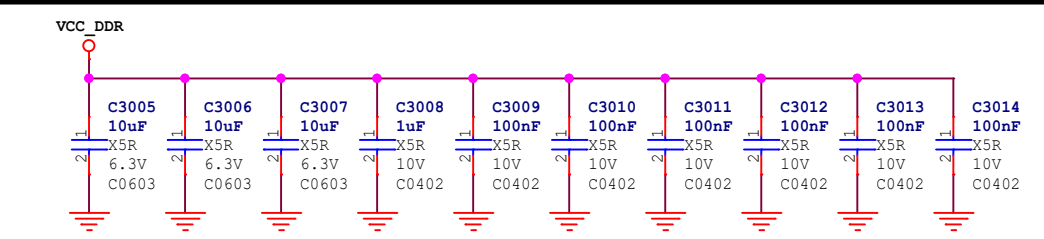
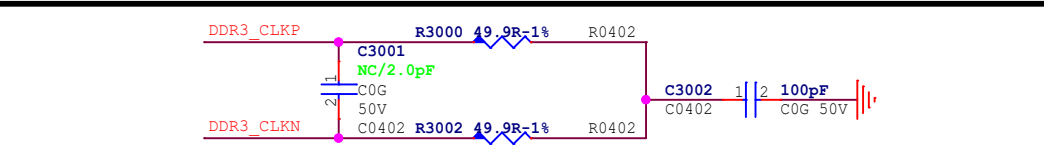
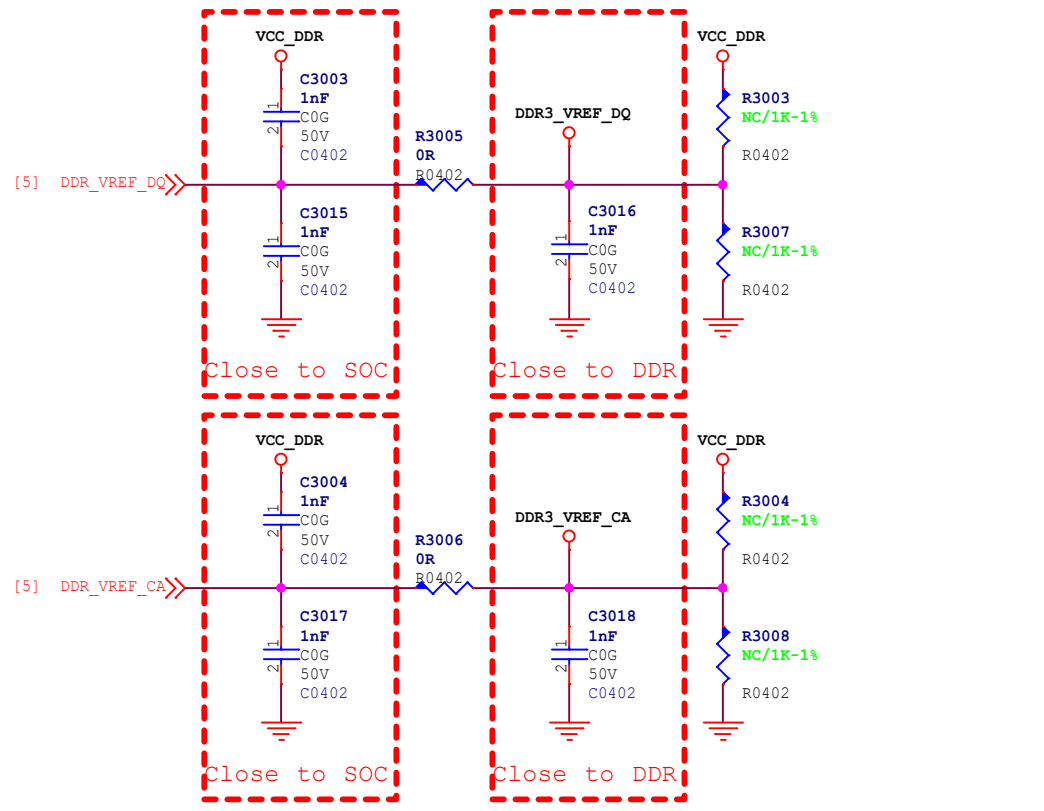
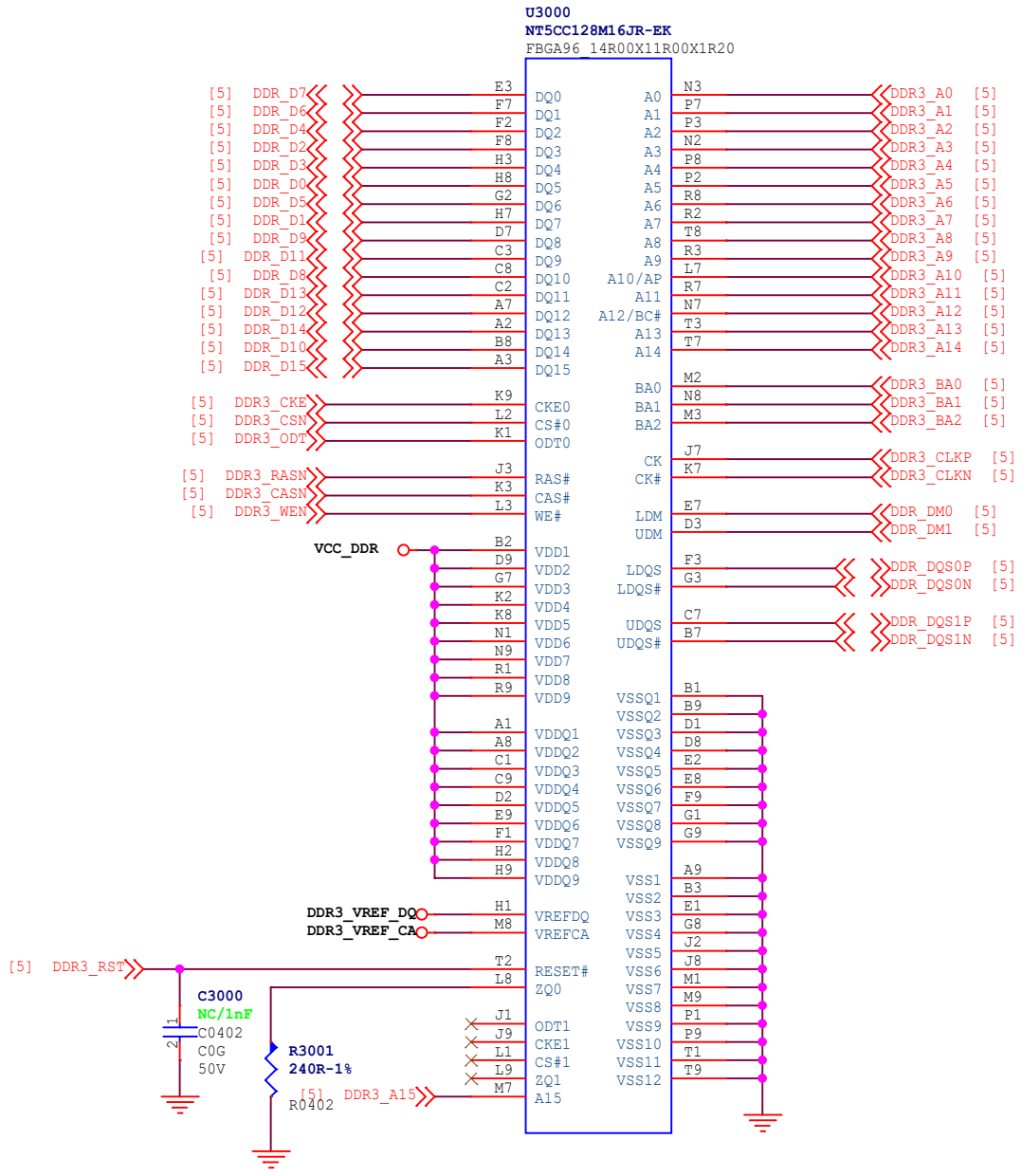
BGA333_13R3X11R3X1R25



Mode	RGB					BT1120	BT656	MCU				
	24bit	18bit	16bit	8bit	6bit	16bit	8bit	24bit	18bit	16bit	8bit	6bit
LCDC_DEN	DEN	DEN	DEN	DEN	DEN	--	--	RDN	RDN	RDN	RDN	RDN
LCDC_VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	--	--	CSN	CSN	CSN	CSN	CSN
LCDC_HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	--	--	WRN	WRN	WRN	WRN	WRN
LCDC_CLK	CLK	CLK	CLK	CLK	CLK	CLK	CLK	RS	RS	RS	RS	RS
LCDC_D23	D23	D17	D15	D7_m1	D5_m1	D15	D7_m1	D23	D17	D15	D7_m1	D5_m1
LCDC_D22	D22	D16	D14	D6_m1	D4_m1	D14	D6_m1	D22	D16	D14	D6_m1	D4_m1
LCDC_D21	D21	D15	D13	D5_m1	D3_m1	D13	D5_m1	D21	D15	D13	D5_m1	D3_m1
LCDC_D20	D20	D14	D12	D4_m1	D2_m1	D12	D4_m1	D20	D14	D12	D4_m1	D2_m1
LCDC_D19	D19	D13	D11	D3_m1	D1_m1	D11	D3_m1	D19	D13	D11	D3_m1	D1_m1
LCDC_D18	D18	D12	--	--	--	--	--	D18	D12	--	--	--
LCDC_D17	D17	--	--	--	--	--	--	D17	--	--	--	--
LCDC_D16	D16	--	--	--	--	--	--	D16	--	--	--	--
LCDC_D15	D15	D11	D10	D2_m1	D0_m1	D10	D2_m1	D15	D11	D10	D2_m1	D0_m1
LCDC_D14	D14	D10	D9	D1_m1	--	D9	D1_m1	D14	D10	D9	D1_m1	--
LCDC_D13	D13	D9	D8	D0_m1	--	D8	D0_m1	D13	D9	D8	D0_m1	--
LCDC_D12	D12	D8	D7	D7_m0	D5_m0	D7	D7_m0	D12	D8	D7	D7_m0	D5_m0
LCDC_D11	D11	D7	D6	D6_m0	D4_m0	D6	D6_m0	D11	D7	D6	D6_m0	D4_m0
LCDC_D10	D10	D6	D5	D5_m0	D3_m0	D5	D5_m0	D10	D6	D5	D5_m0	D3_m0
LCDC_D9	D9	--	--	--	--	--	--	D9	--	--	--	--
LCDC_D8	D8	--	--	--	--	--	--	D8	--	--	--	--
LCDC_D7	D7	D5	D4	D4_m0	D2_m0	D4	D4_m0	D7	D5	D4	D4_m0	D2_m0
LCDC_D6	D6	D4	D3	D3_m0	D1_m0	D3	D3_m0	D6	D4	D3	D3_m0	D1_m0
LCDC_D5	D5	D3	D2	D2_m0	D0_m0	D2	D2_m0	D5	D3	D2	D2_m0	D0_m0
LCDC_D4	D4	D2	D1	D1_m0	--	D1	D1_m0	D4	D2	D1	D1_m0	--
LCDC_D3	D3	D1	D0	D0_m0	--	D0	D0_m0	D3	D1	D0	D0_m0	--
LCDC_D2	D2	D0	--	--	--	--	--	D2	D0	--	--	--
LCDC_D1	D1	--	--	--	--	--	--	D1	--	--	--	--
LCDC_D0	D0	--	--	--	--	--	--	D0	--	--	--	--



DDR3/DDR3L 1x16bit



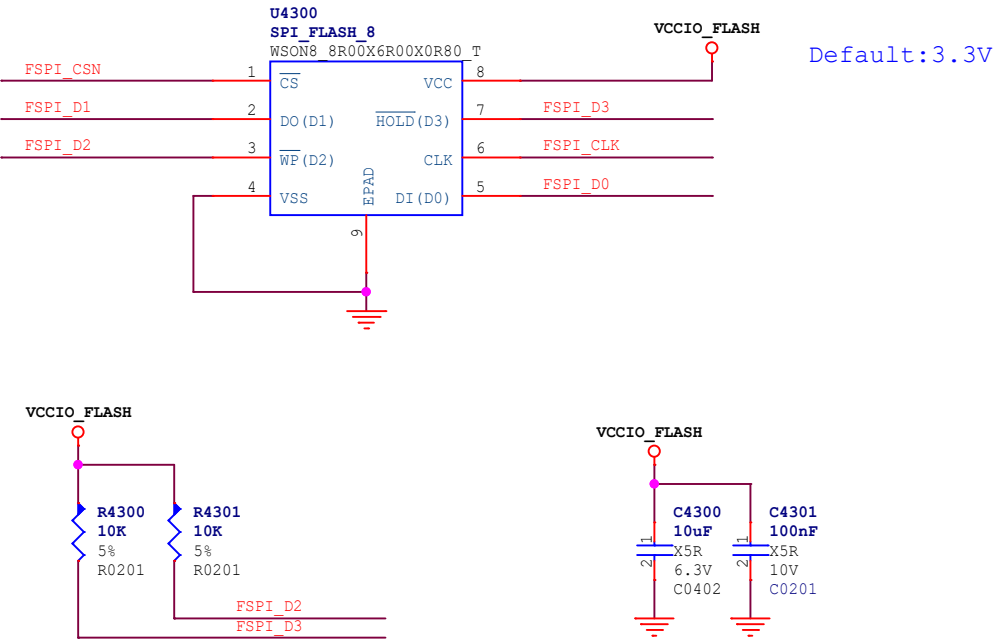
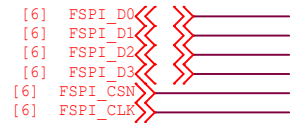
Note: All the Power filter capacitors should be placed close to the power pins of DDR

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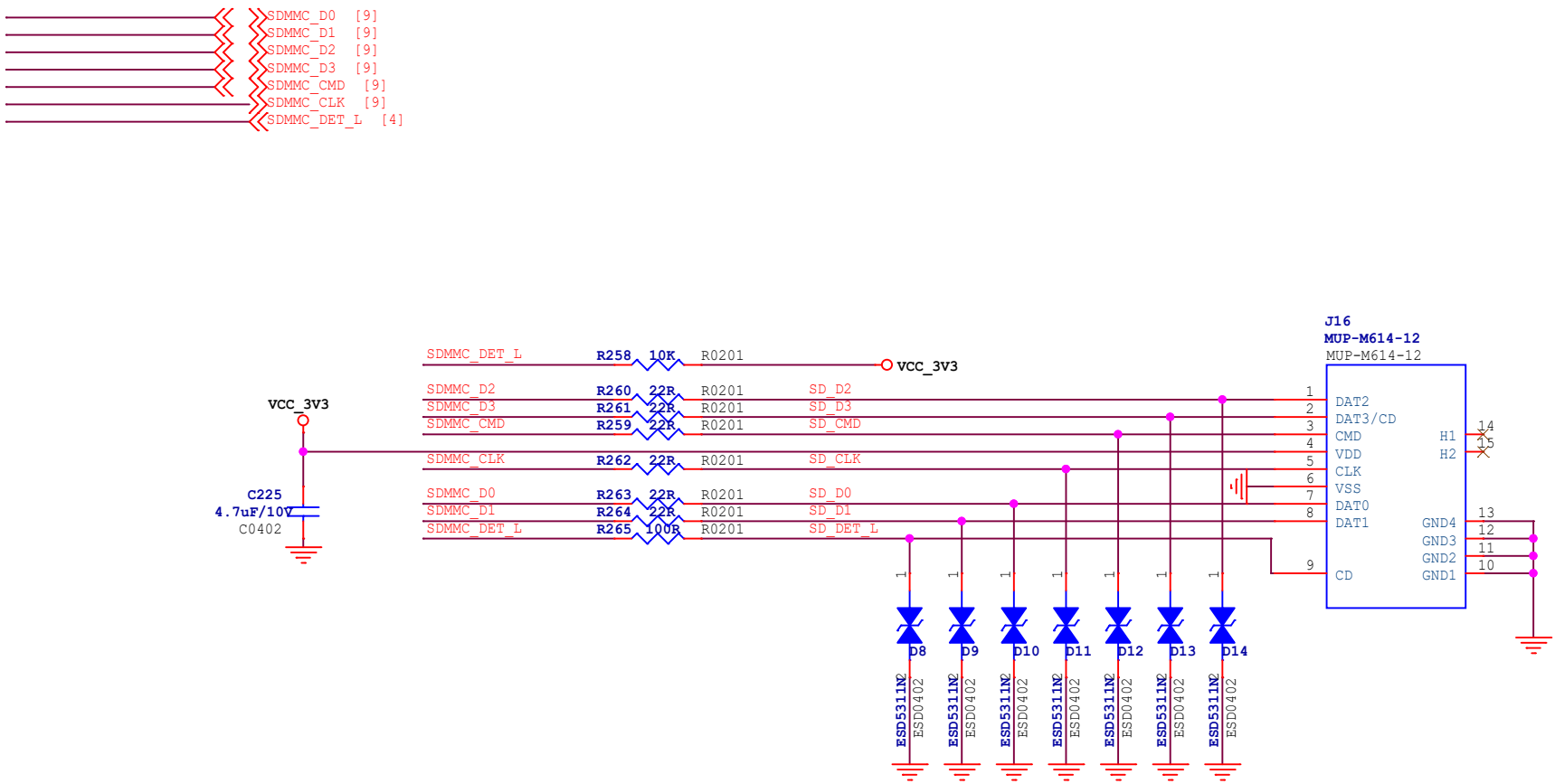
Project:	ArmSoM-FORGE1		
File:	DRAM_DDR3/DDR3L_96P_1X16bit		
Date:	Tuesday, March 25, 2025	Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>
Sheet:	10 of 21		

SPI Flash

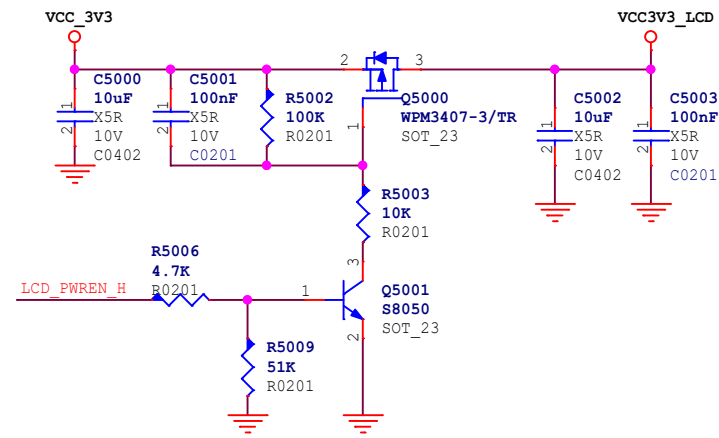
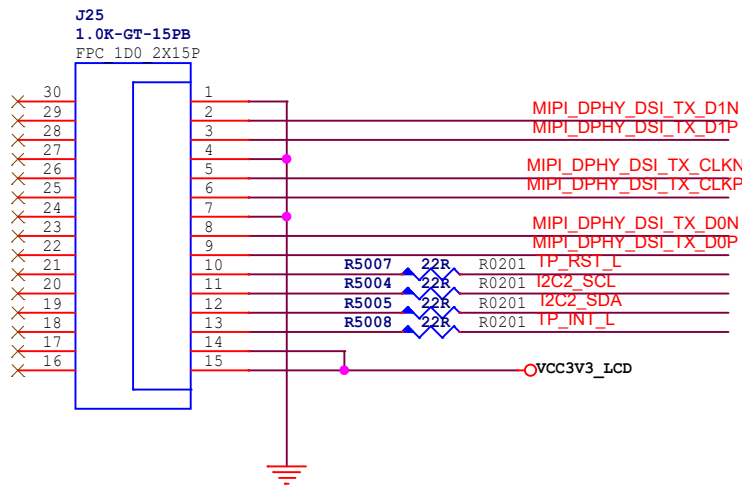
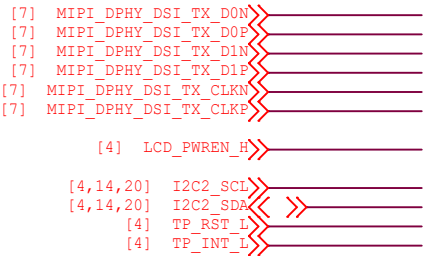
NOTE:
Refer to the latest AVL for parts selection.



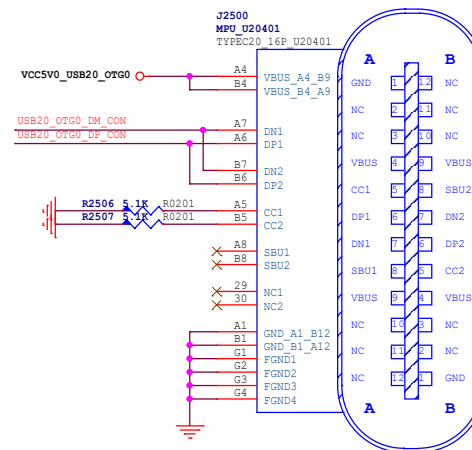
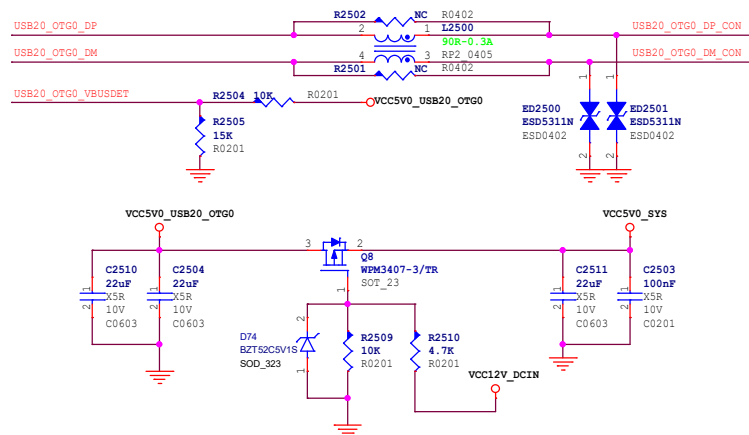
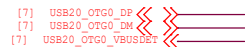
TF Card



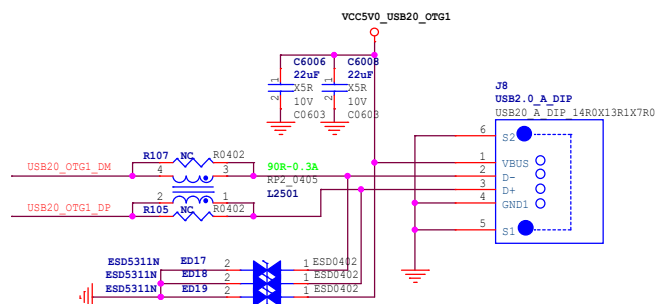
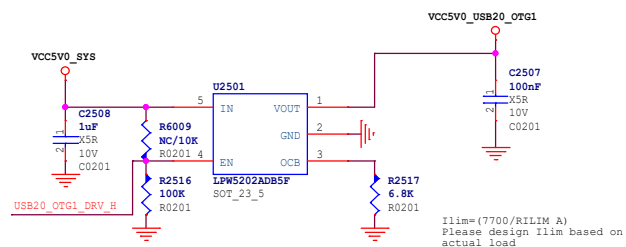
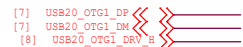
MIPI Panel Interface



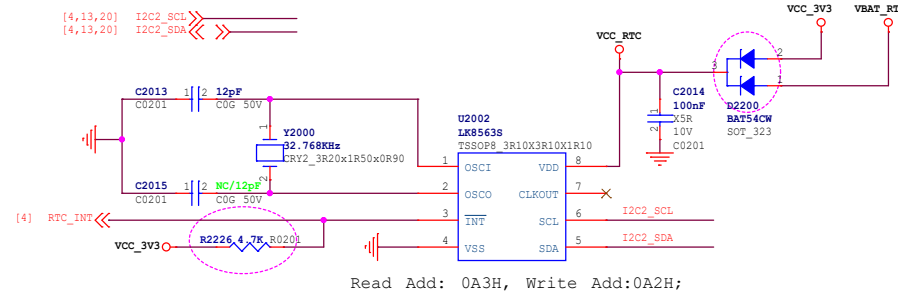
USB2.0 OTG0



USB2.0 OTG1

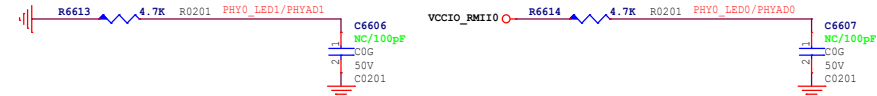
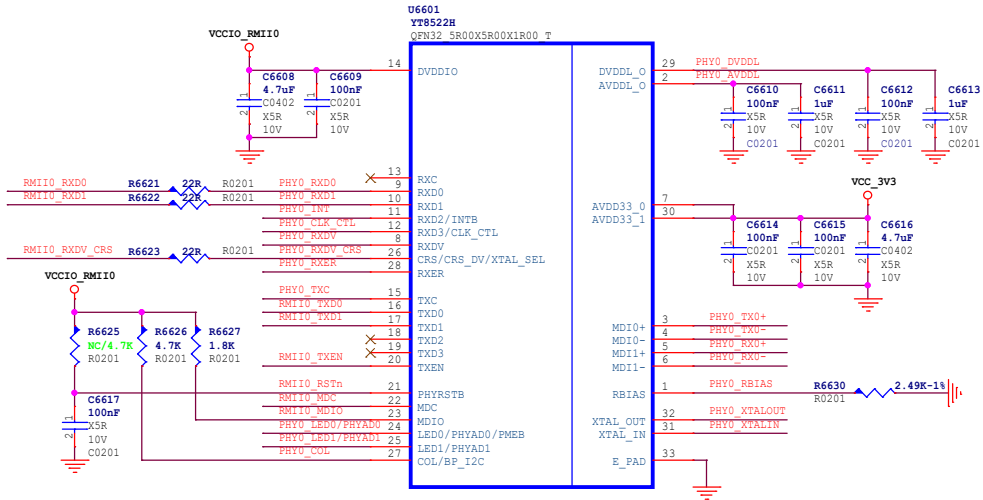
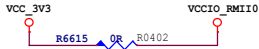
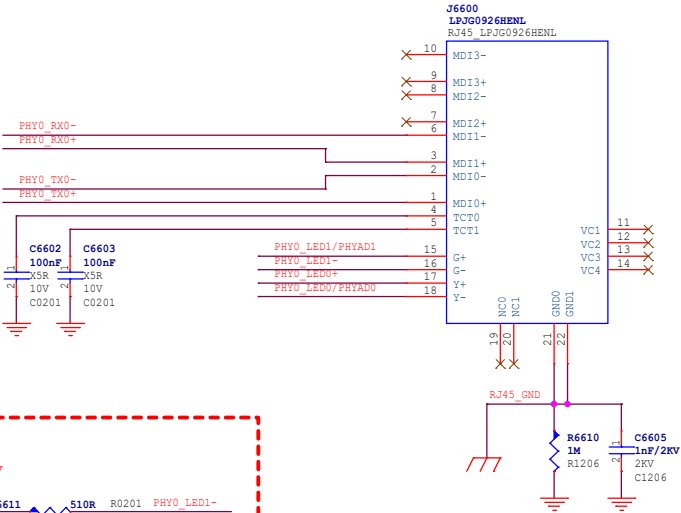
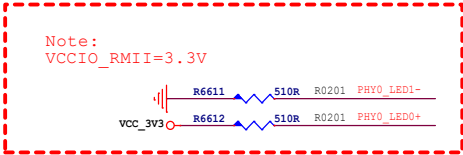
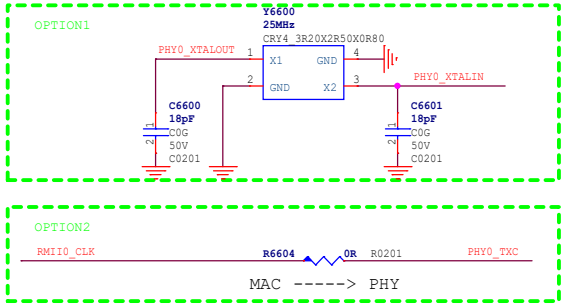
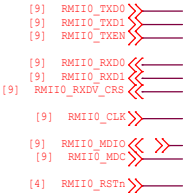


RTC



 armsom		https://armsom.org/	
Project:	ArmSoM-FORGE1		
File:	USB-Port-RTC		
Date:	Tuesday, March 25, 2025	Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>
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FEPHYO



PHY Address Config

RMII REF_CLK direction:
(0 = RMII REF_CLK PHY Output mode; 1 = RMII REF_CLK PHY Input mode)

Reference Clock input selection:
(0 = Reference Clock from XTAC; 1 = Reference Clock from TXC)

This pin is pulled high by an external 4.7Kohm.
This pin is used for the interrupt function only when in the RMII mode.

MII/RMII Selection: (Pull High for RMII mode(default))

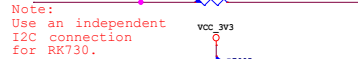
WOL/LED0 Selection: (0 = LED0 Mode(default); 1 = WOL(Wake-on-LAN) Mode)

UTP / Fiber Selection: (0 = UTP Mode(default); 1 = Fiber Mode)

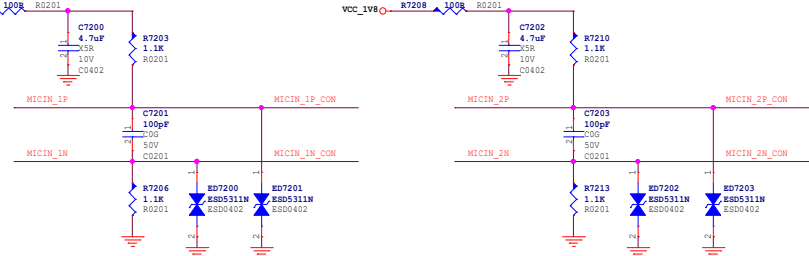
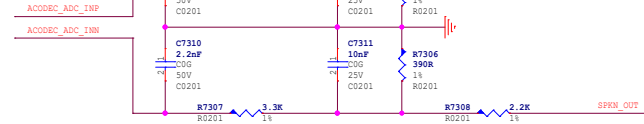
armsom		https://armsom.org/	
Project:	ArmSoM-FORGE1		
File:	Ethernet-FEPHY_RMII0		
Date:	Tuesday, March 25, 2025	Rev:	V1.0
Designed by:	Park	Reviewed by:	<Checker>
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```
[4] SAI1_MCLK >>>
[4] SAI1_SCLK >>>
[4] SAI1_LRCK >>>
[4] SAI1_SDI <<<
[4] SAI1_SDO0 <<<
[4] I2C1_SCL <<<
[4] I2C1_SDA <<>>

[4] PHONE_DET_L_1V8 >>>
```

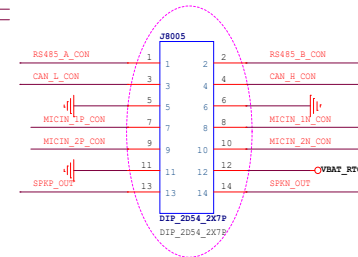


SPEAKER



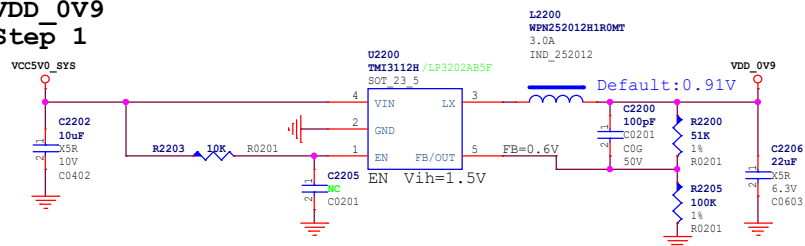
```
[20] RS485_A_CON >>>
[20] RS485_B_CON >>>

[20] CAN_L_CON >>>
[20] CAN_H_CON >>>
```

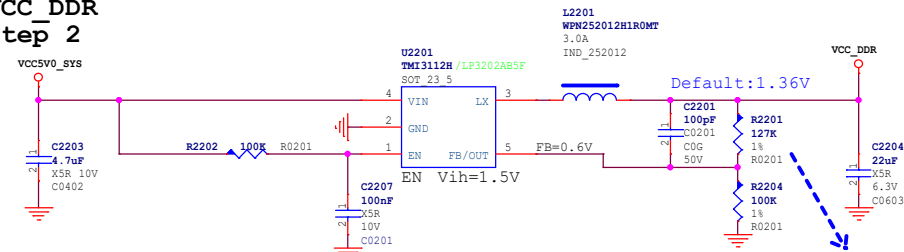


[4] PWM0_CH0_CPU

VDD_0V9 Step 1

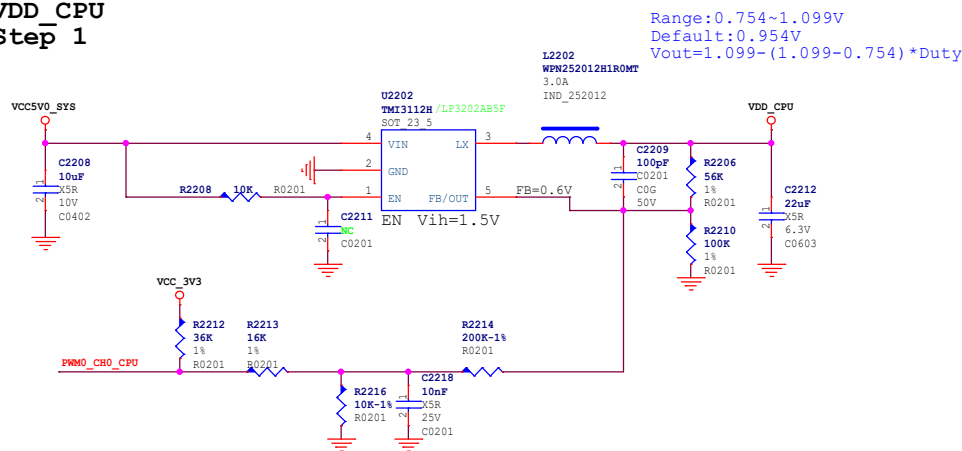


VCC_DDR Step 2

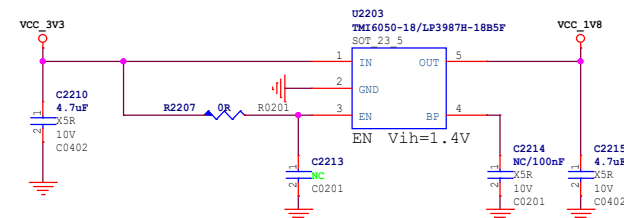


DDR2	1.81V	200K
DDR3	1.50V	150K
DDR3L	1.36V	127K

VDD_CPU Step 1



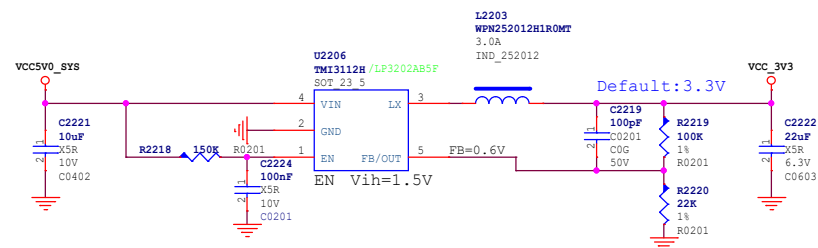
VCC_1V8 Step 2a



Note:
1.Do not have a soft opening inside the LDO.
2.Star line, distinguish between analog and digital power supply

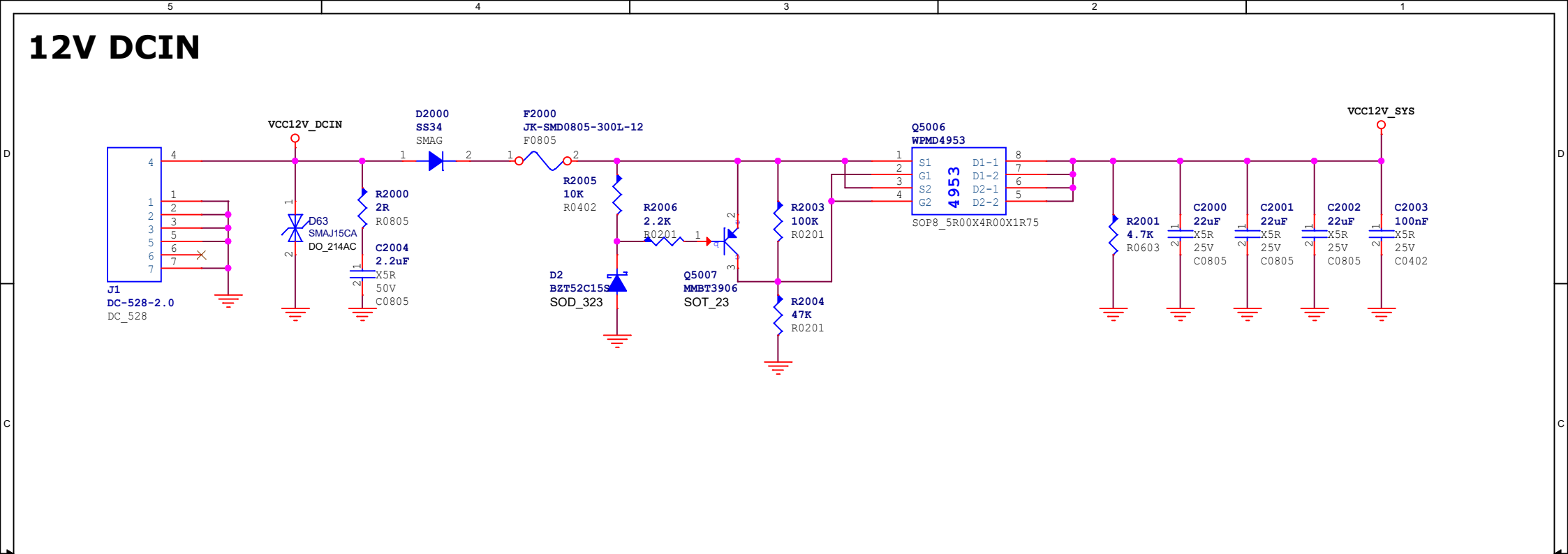
VCC_1V8 → Digital Power:SOC IO,WIFI eMMC...
→ Analog Power:SOC USB,MIC...
→ Analog Power:SOC PLL/OSC(ONLY)

VCC_3V3 Step 3



12V DCIN

The schematic diagram illustrates a 12V DC input circuit. The input is connected to a DC source (J1, DC-528-2.0) and passes through a diode (D63, SMAJ15CA) and a network of resistors (R2000, R2005, R2006, R2003, R2004) and capacitors (C2004, C2000, C2001, C2002, C2003). The circuit includes a MOSFET driver stage with a MOSFET (D2000, SS34) and a BJT (Q5007, MMBT3906). The output is connected to a 12V DC system output (VCC12V_SYS) through a 4953 component (Q5006, WPMD4953). The circuit is powered by a 12V DC source and includes various passive components for filtering and protection.



VCC5V0_SYS

VCC12V_SYS

4.5V<VIN<18V

U2207
TMI3252SH
SOT_23_6

VIN SW 6

GND BOOT 1

EN FBK 3

FB=0.6V

L2204
MWSA0503S-2R2MT
IND_545228

C2228
100pF
C0G
50V
C0201

R2222
75K
1%
R0201

R2225
10K
1%
R0201

C2229
22uF
X5R
10V
C0805

C2230
22uF
X5R
10V
C0805

C2231
100nF
X5R
10V
C0402

R2223
4.7K
R0603

C2501
22uF
X5R
10V
C0805

C2502
22uF
X5R
10V
C0805

C2509
22uF
X5R
10V
C0805

VCC5V0_SYS

C2226
22uF
X5R
25V
C0805

C2227
100nF
X5R
25V
C0402

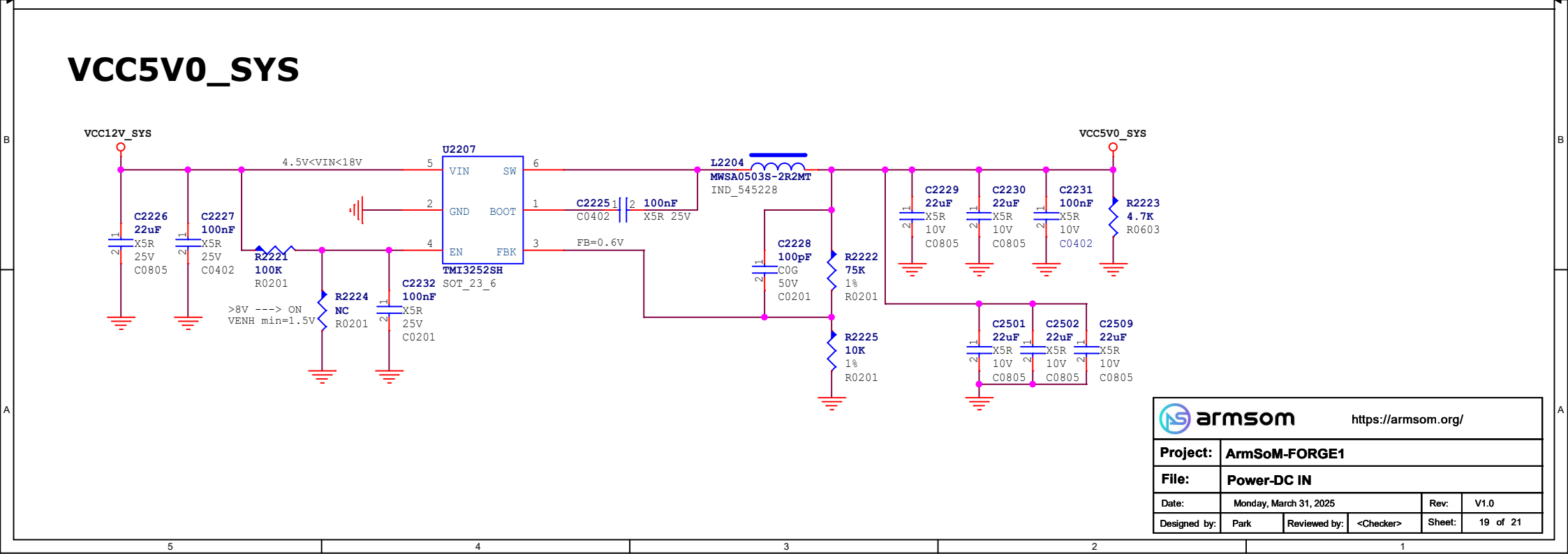
R2221
100K
R0201

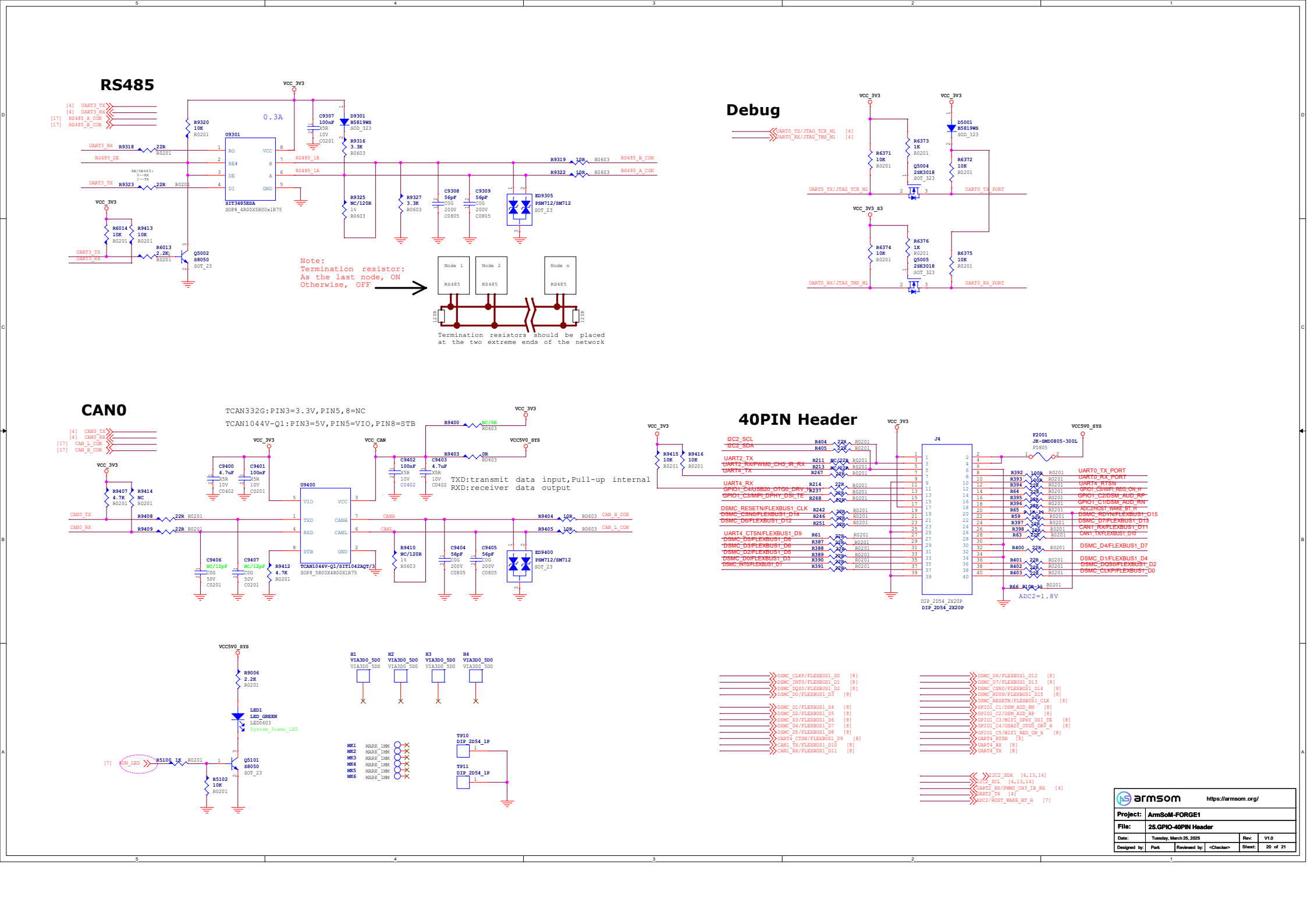
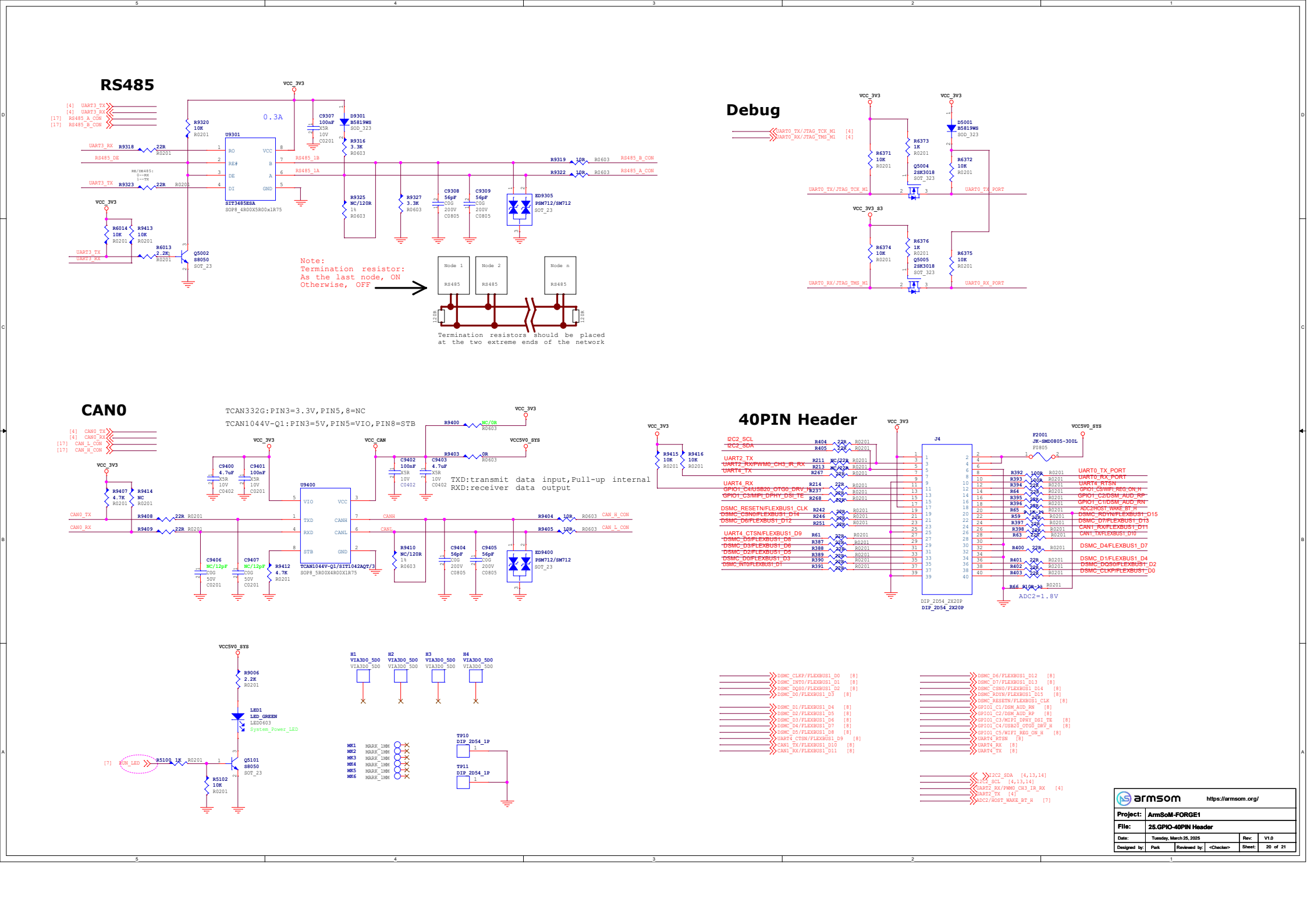
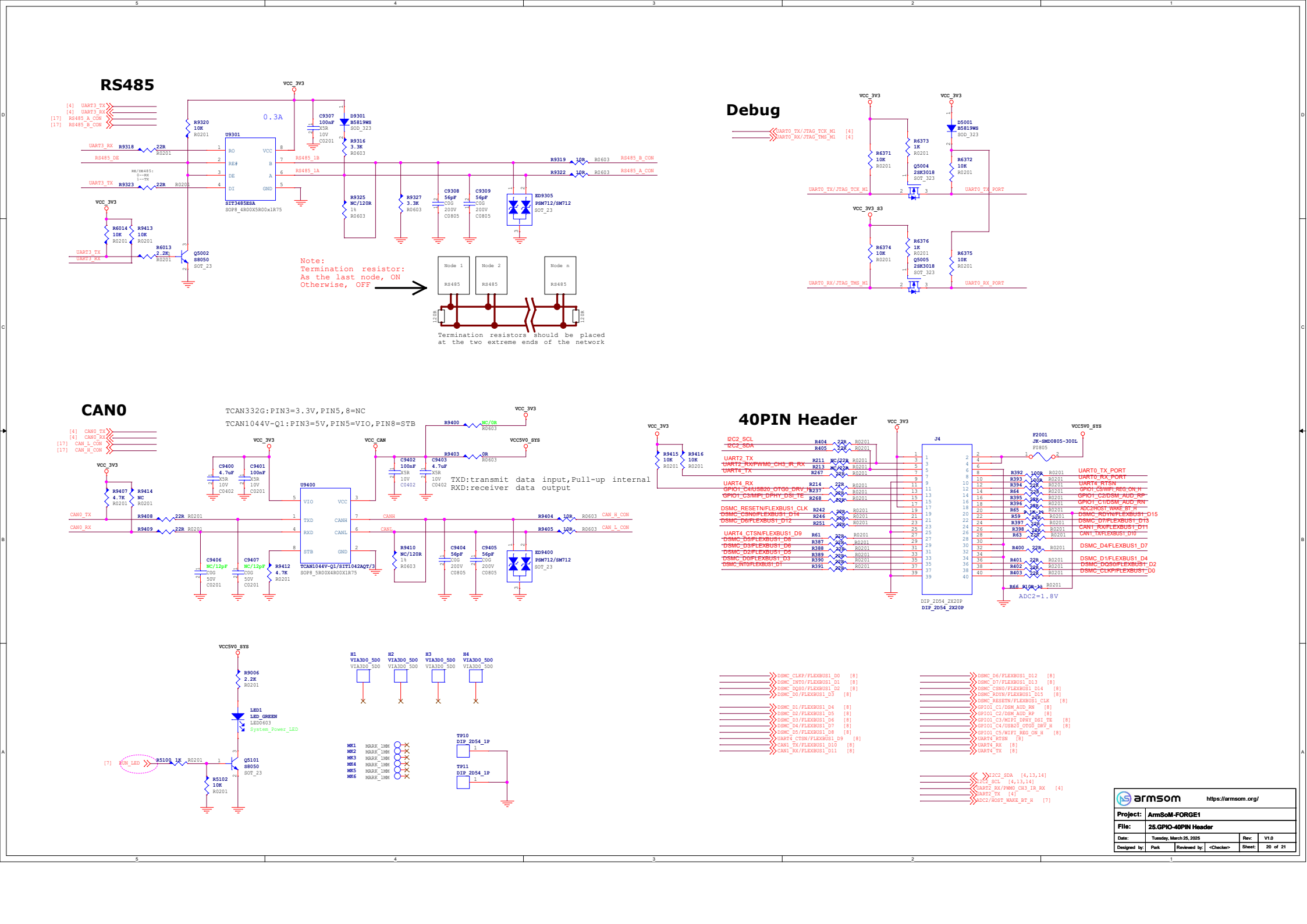
R2224
NC
R0201

C2232
100nF
X5R
25V
C0201

>8V ---> ON
VENH min=1.5V

 https://armsom.org/	
Project:	ArmSoM-FORGE1
File:	Power-DC IN
Date:	Monday, March 31, 2025
Designed by:	Park
Reviewed by:	<Checker>
Rev:	V1.0
Sheet:	19 of 21





RS485

0.3A

Note: Termination resistor: As the last node, ON Otherwise, OFF

Node 1 Node 2 Node n

Termination resistors should be placed at the two extreme ends of the network

CAN0

TCAN332G: PIN3=3.3V, PIN5=NC
TCAN1044V-Q1: PIN3=5V, PIN5=VIO, PIN8=STB

TXD: transmit data input, Pull-up internal
RXD: receiver data output

40PIN Header

Debug

VCCSV0_SYS

ADC2=1.8V

ARM SOM FORGE1

Project: ArmSOM-FORGE1

File: 25.GPIO-40PIN Header

Date: Tuesday, March 25, 2025

Designed by: Park

Reviewed by: <Checker>

Rev: V1.0

Sheet: 20 of 21

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A