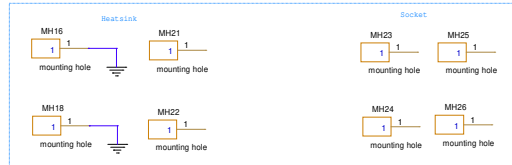


AGILEX™ 5 FPGA E-SERIES 065B PREMIUM DEVELOPMENT KIT (PRODUCTION)

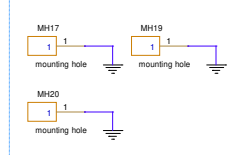
REV	DATE	PAGES	DESCRIPTION
A1	05/30/2024	All	Initial Release
A2	09/23/2024	All	Update to Altera logo, and Altera copy right declaration
A3	06/23/2025	13-16 8, 16, 19, 44	Update QLK_SEL, UART0 default state to Low status Update IO98B CDR assignment per A5ED065B pinout Clean up unused circuitry
	09/17/2025	All	Dev Kit Production Version, Update Altera Schematic Template

PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	Cover, Table of Contents, Notes	38	SFP1
2	Block Diagram	39	SFP2
3	Power Tree Diagram	40	XCVR SMAs
4	Power Sequence Diagram	41	FMC+ PIN TABLE
5	Clock Diagram	42	FMC+ CONNECTOR
6	I2C Diagram	43	10/100/1G/2.5G SGMII ENET1
7	JTAG Diagram	44	BLANK
8	MAX10 SYS Control 1/2	45	10/100/1G RGMII ENET
9	MAX10 SYS Control 2/2	46	USB Diagram
10	AVST Config Flash & HyperRAM	47	USB HUB, BLASTER, UART
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15	HSIO 3ALR - DDR4 COMP_HPS	52	CLOCKS 1 - PTP 1588
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29	DDR4 COMP1 ECC	66	VCCIO_2A, 2V5_SYS, 1V8LP4
30	HPS DDR4 COMP BYTE 0-1	67	DDR4 VREF, VTT
31	HPS DDR4 COMP BYTE 2-3		
32	HPS DDR4 COMP ECC		
33	BLANK		
34	ARDUCAM MIPI		
35	HPS Connector		
36	QSFP1		
37	QSFP2		

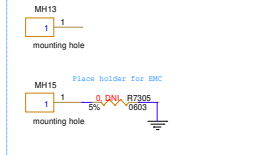
Mounting hole for FPGA



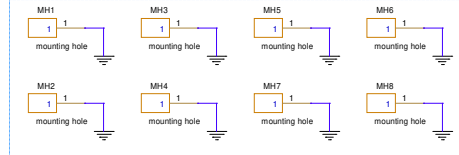
Mounting hole for HPS DC



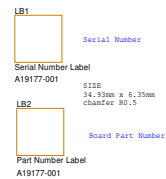
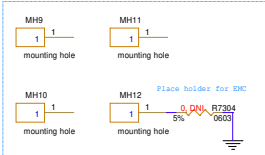
Mounting hole for top VR heatsink



Mounting hole for board



Mounting hole for bottom VR heatsink

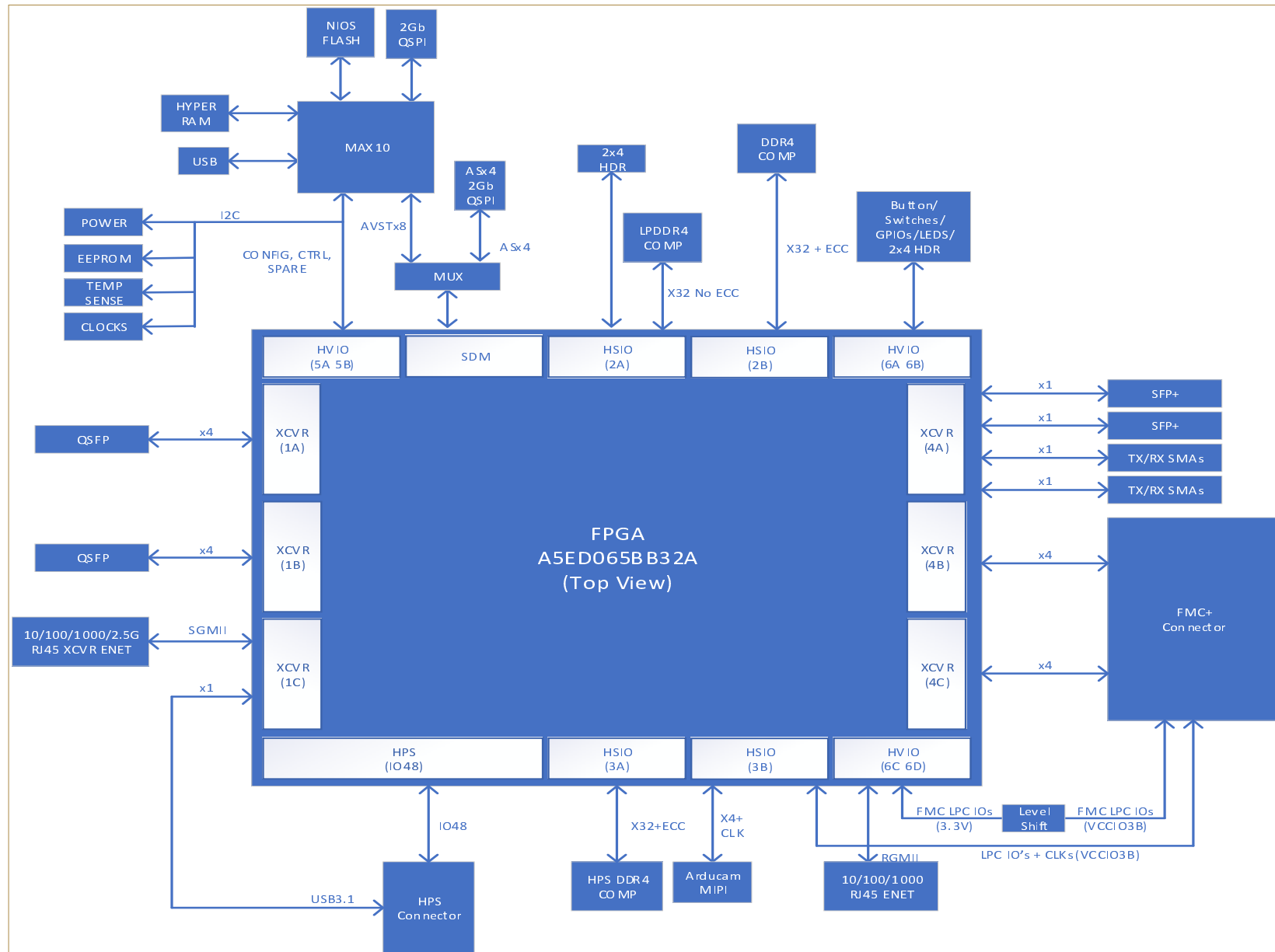


Board Name	Board OPN/ Board MMID	Device OPN/ Device MMID	TA/ PBA/ PB/ PCB MPN
Agilex TM 5 FPGA E-Series 065B Premium Development Kit (ES)	DK-A5E065BB32AES1/ 99CA36	A5ED065BB32AE6SR0/ 99CNCG	N20886-002/ N11816-101 N18468-002/ 100-0330713-A2
Agilex TM 5 FPGA E-Series 065B Premium Development Kit (PRODUCTION)	DK-A5E065BB32AEA/ 99D001	A5ED065BB32AE4S/ 99D56X	N56395-001/ N65908-101 N18468-003/ 100-0330713-A3

Pin information reference:
A5ED065B Device
B32A Version: 2025-06-06

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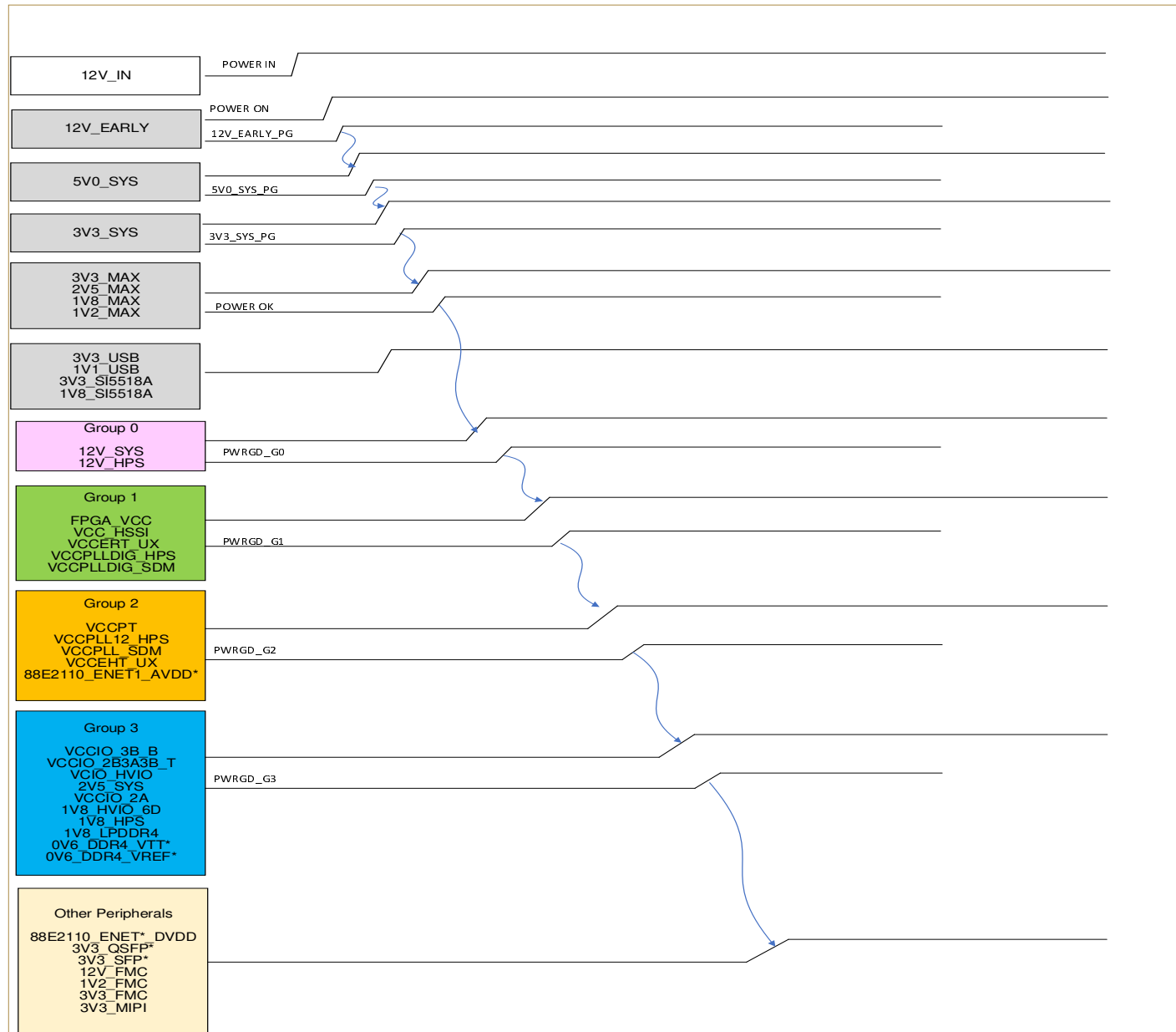
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```

graph LR
    PWR_ON_SWITCH[PWR_ON SWITCH] --> Delay(( ))
    Delay --> Group1((Group1))
    Group1 --> Group2((Group2))
    Group2 --> Group3((Group3))
    Group3 --> Group4((Group4))
    Group4 --> Group5((Group5))
    subgraph FPGA
        Group2
        Group3
        Group4
    end

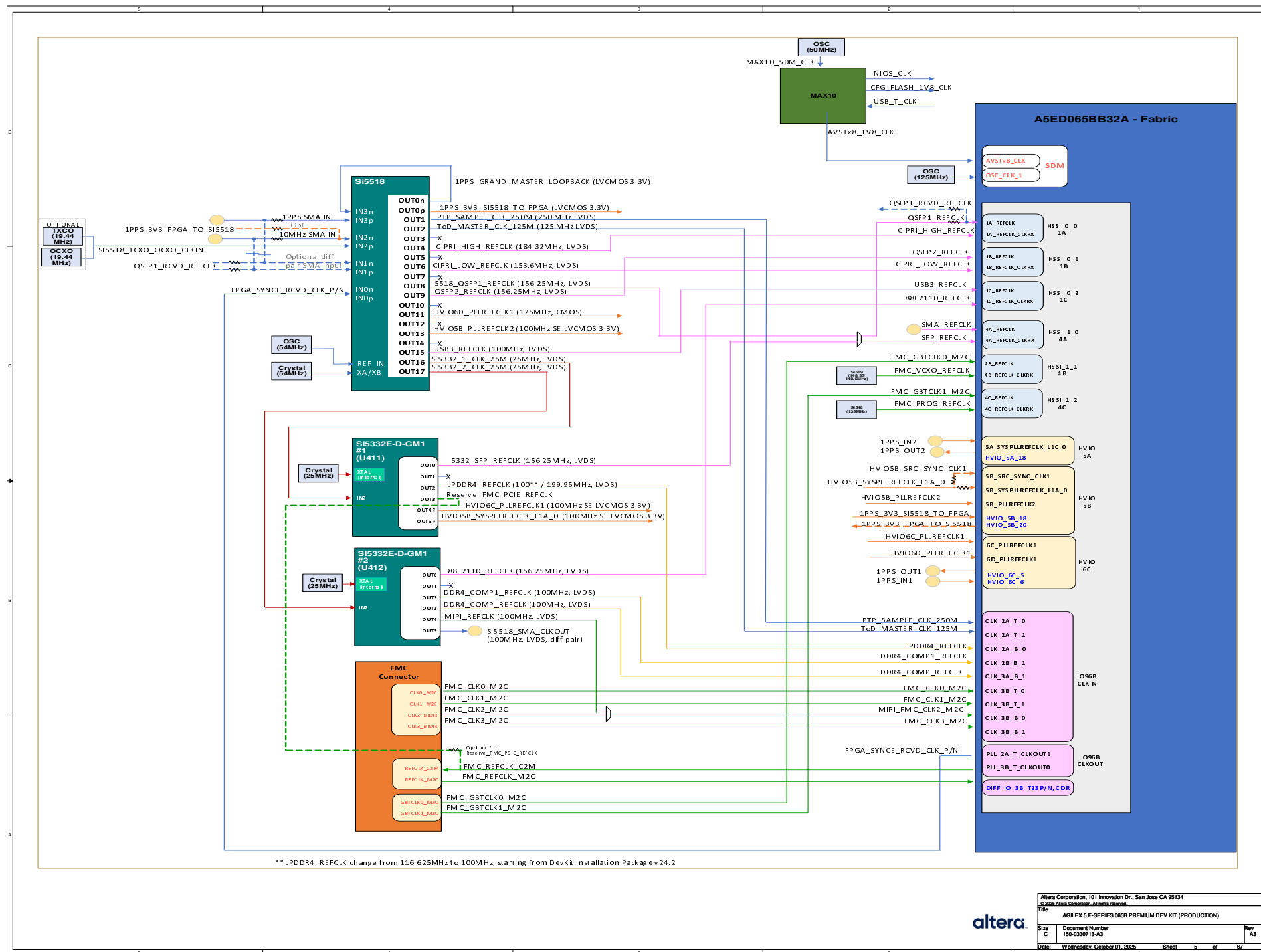
```

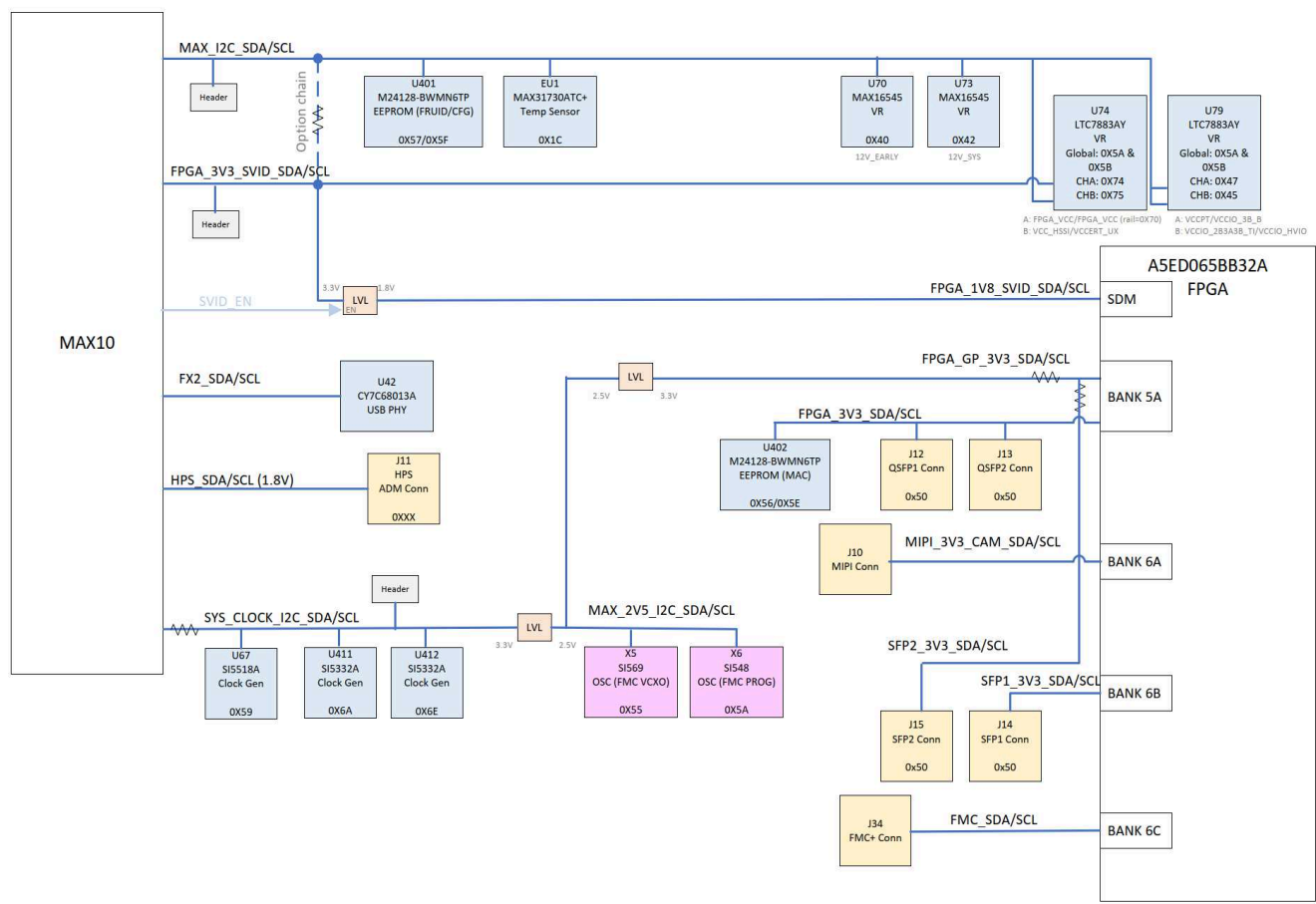




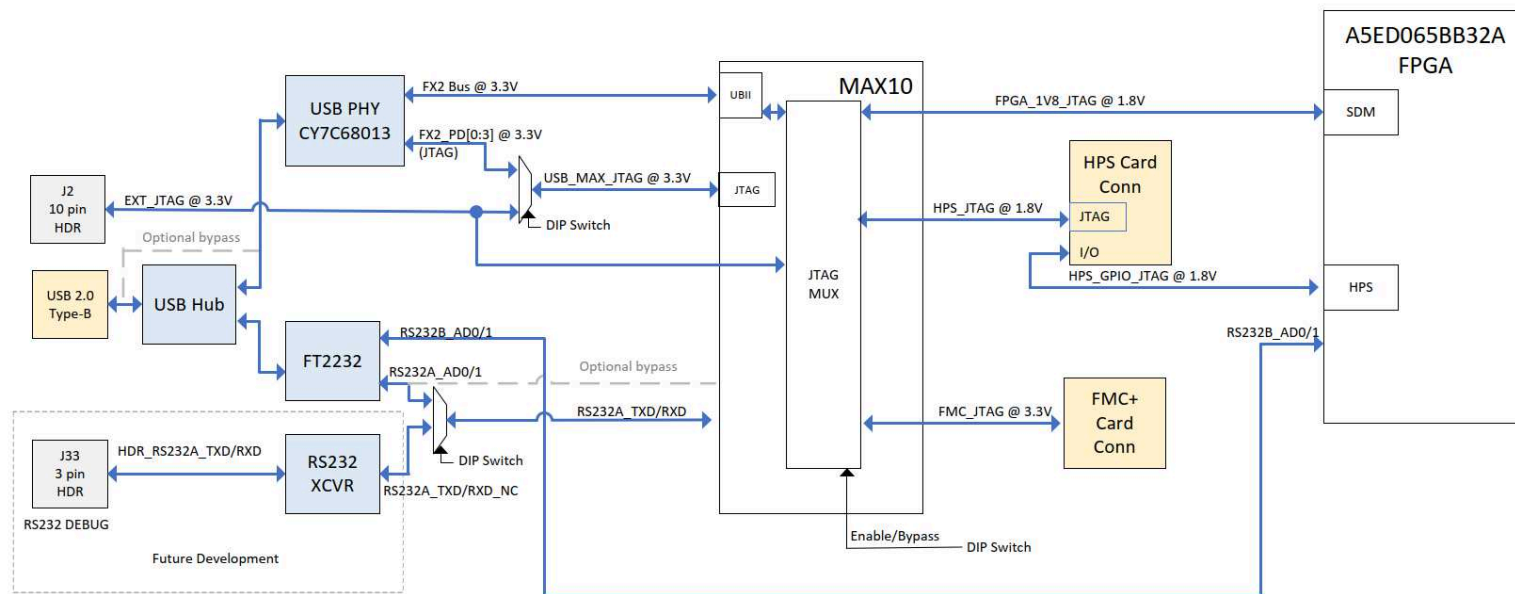
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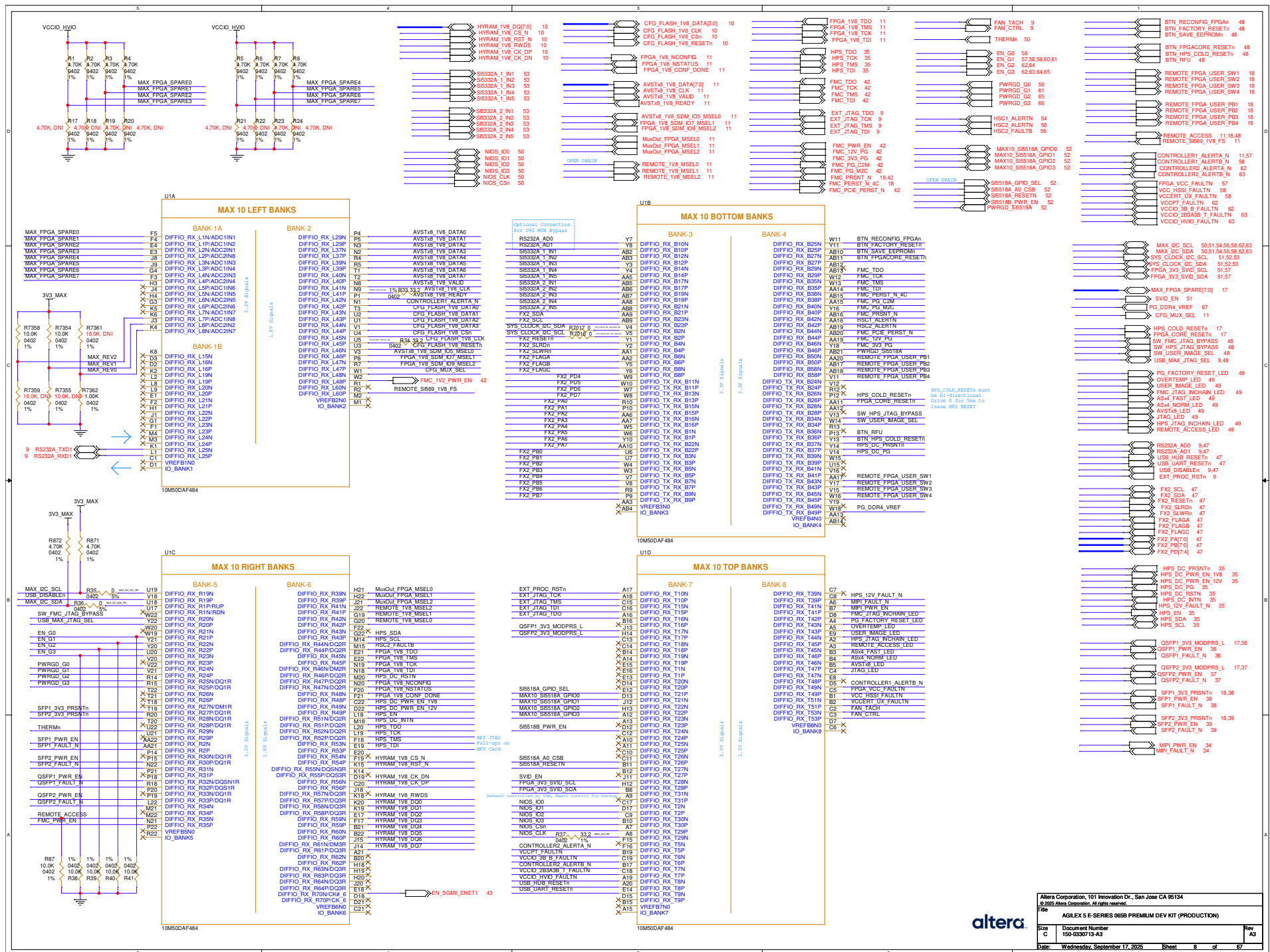


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File	AGILEX 5 E-SERIES 905B PREMIUM DEV KIT (PRODUCTION)		
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C	150-0300715-A3	A3	
Date:	Wednesday, September 17, 2015	Sheet	6 of 67

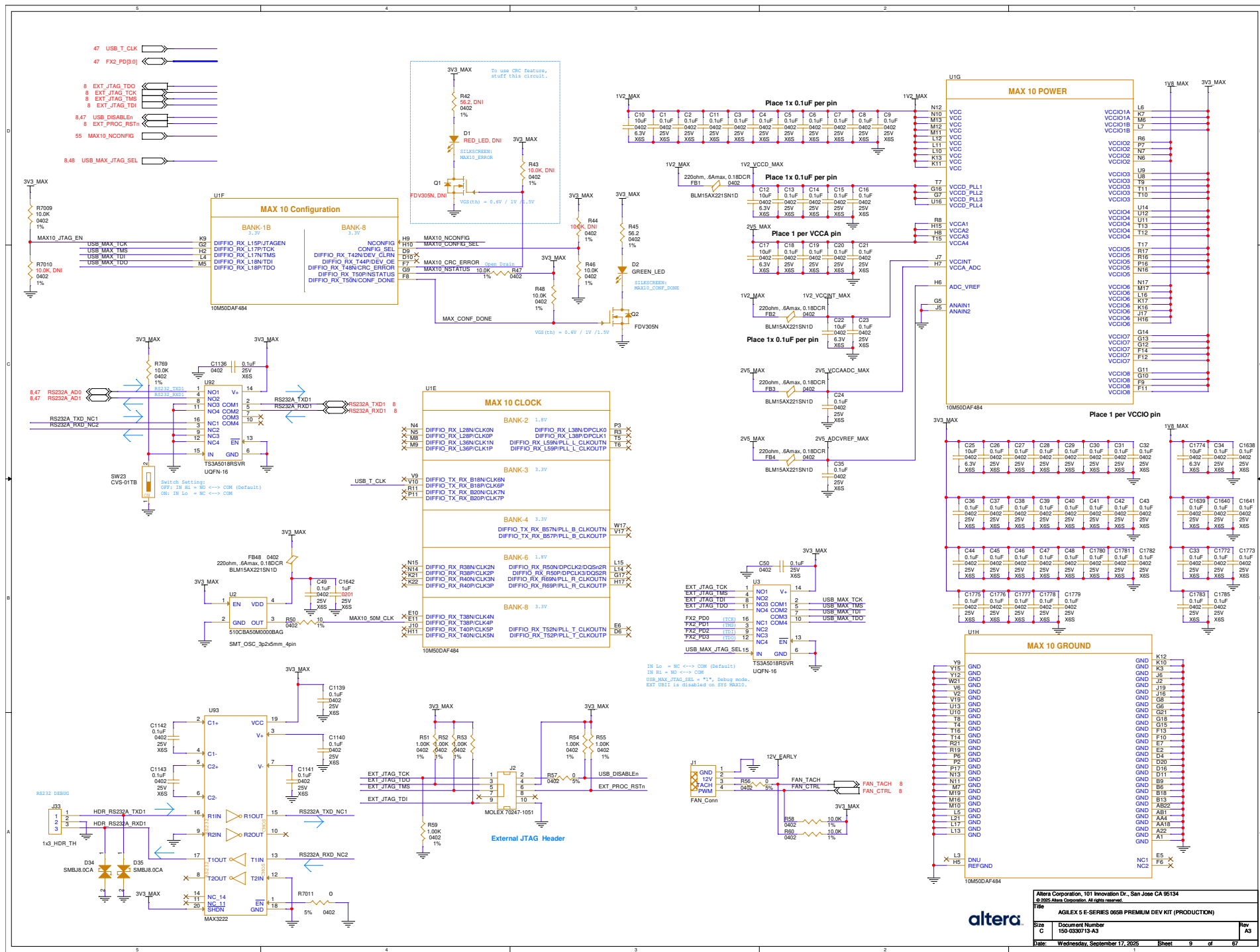


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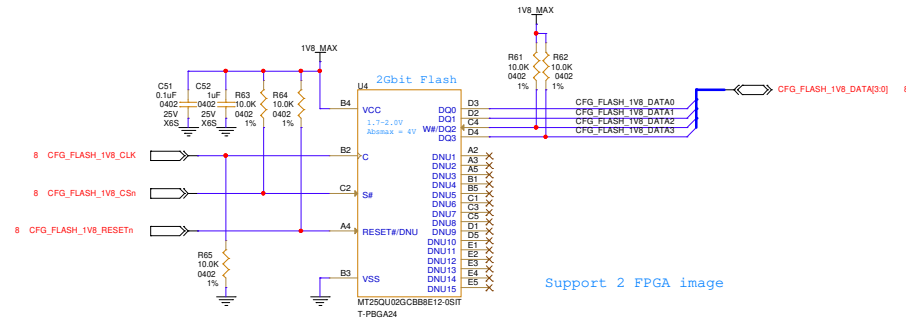
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File	AGILEX 5 E-SERIES 905B PREMIUM DEV KIT (PRODUCTION)		
Size	Document Number	Rev	
C	150-0300713-A3	A3	
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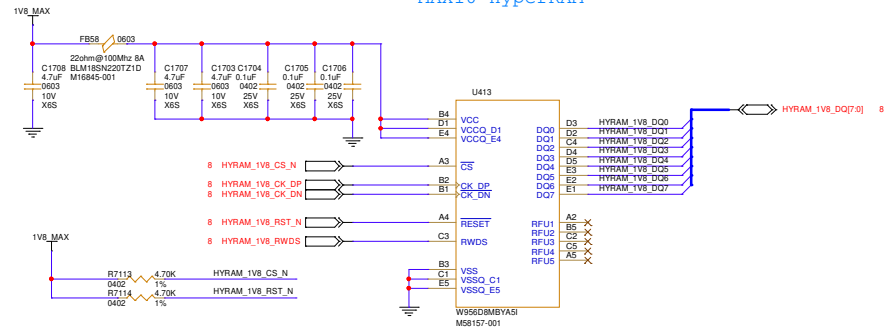
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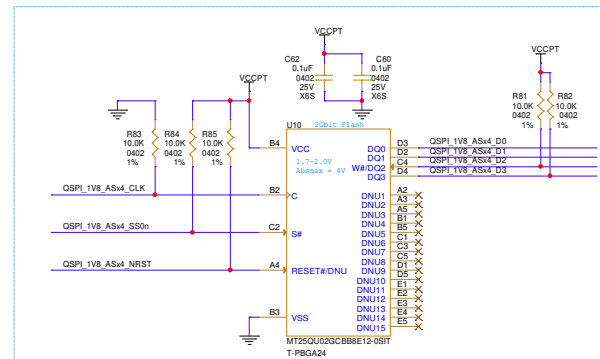
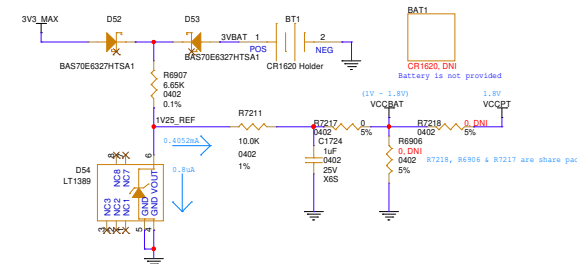
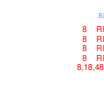
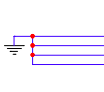
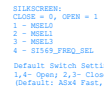
AVST CFG Flash



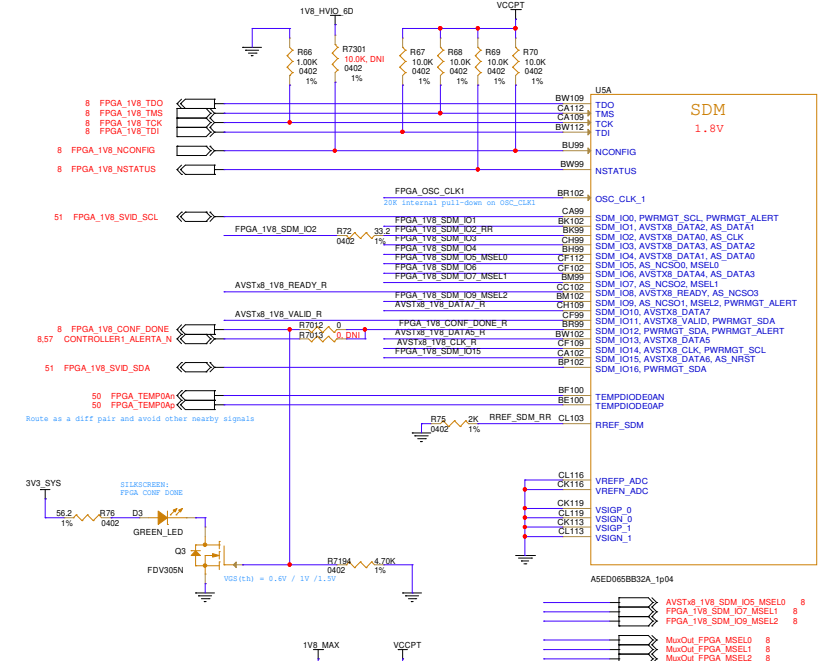
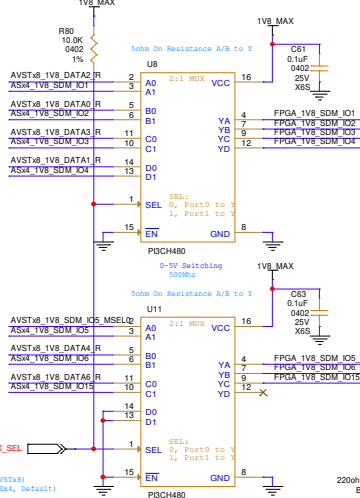
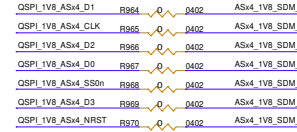
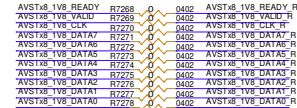
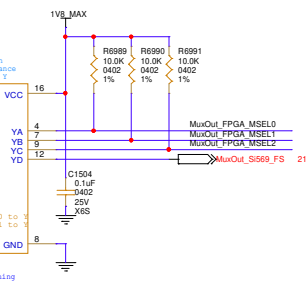
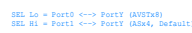
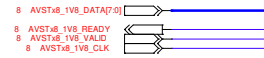
MAX10 HyperRAM



SDM CONFIGURATION



ASx4 QSPI Flash



		CFG_MUX_SEL = 0	CFG_MUX_SEL = 1
Pins	MSEL	Avalon-ST x8	AS (normal mode)
SDM_I00		PWR_SCL	PWR_SCL
SDM_I01		AVSTx8_DATA2	AS_DATA1
SDM_I02		AVSTx8_DATA0	AS_CLK
SDM_I03		AVSTx8_DATA3	AS_DATA2
SDM_I04		AVSTx8_DATA1	AS_DATA0
SDM_I05	MSEL0		AS_nCS00
SDM_I06		AVSTx8_DATA4	AS_DATA3
SDM_I07	MSEL1	HPS_COLD_nRESET	AS_nCS02
SDM_I08		AVST_READY	AS_nCS03
SDM_I09	MSEL2		AS_nCS01
SDM_I010		AVSTx8_DATA7	
SDM_I011		AVSTx8_VALID	HPS_COLD_nRESET
SDM_I012		CONF_DONE	CONF_DONE
SDM_I013		AVSTx8_DATA5	
SDM_I014		AVSTx8_CLK	
SDM_I015		AVSTx8_DATA6	AS_nRST
SDM_I016		PWR_SDA	PWR_SDA

CONFIG MODE	MSEL2	MSEL1	MSEL0
ASx4 FAST Default	0	0	1
ASx4 NORM	0	1	1
AVSTx8	1	1	0
JTAG	1	1	1

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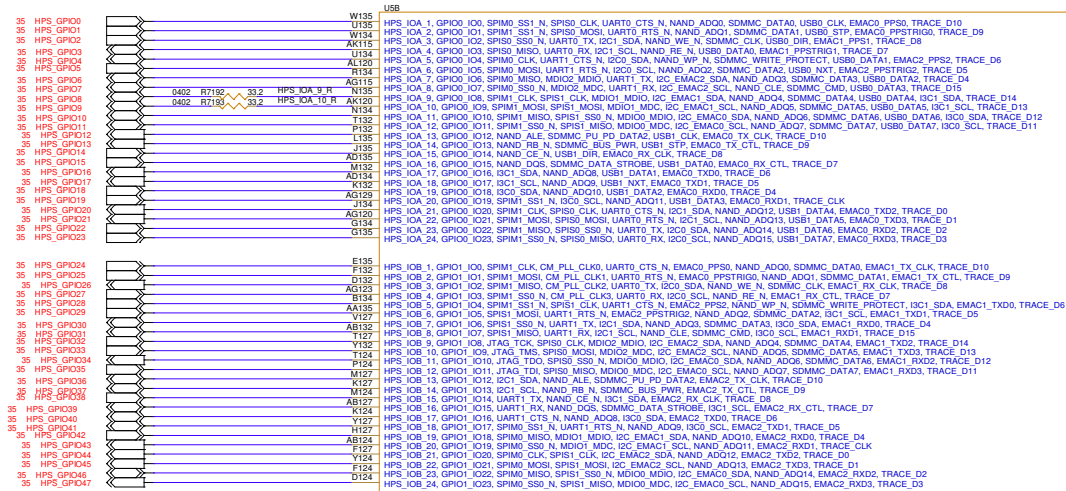
Title AGILEX 5 E-SERIES 065B PREMIUM DEV KIT (PRODUCTION)

AGILEX 5E SERIES 5000 THERMOCALORIMETER (PRODUCTION)

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HPS BANK IO48



1.8V
HPS

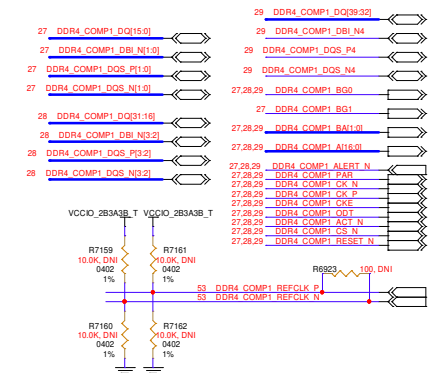
A5ED065BB32A_1p04

Please refer to Agilix EMIF User Guide for pin assignment rules.



HSIO BANKS 2BL AND 2BR

Please refer to Agilex EMIF User Guide for pin assinging rules.



SWAP RULES:
 1) Entire Byte lanes can be swapped.
 2) Q0 bits within a byte lane can be swapped.
 3) DQS_P/N, DBI signals are fixed locations.
 4) ECC byte must be connected to Byte Lane 7.
 5) For x16 device, DQ0 & DQ1 must be connected to one x16 device and placed on adjacent Byte Lane unless they are separated by ADD/ODD lane.

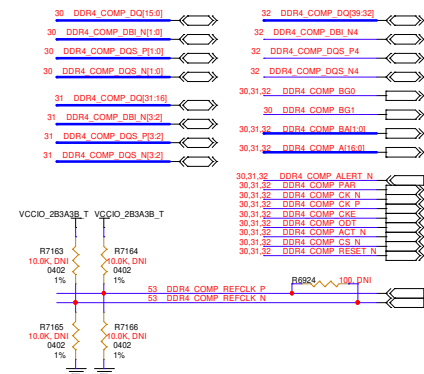
SWIZZLE RULES:
 BYTE_SWIZZLE_C0[0]=0, X,X,X,1,2,3, R0C0;
 PIN_SWIZZLE_C0_DQ0[0]=1, 7,5,6,4,6,2;
 PIN_SWIZZLE_C0_DQ1[1]=5,15,13,12,14,8,10;
 PIN_SWIZZLE_C0_DQ2[2]=17,21,19,23,16,22,18,20;
 PIN_SWIZZLE_C0_DQ3[3]=29,31,27,33,30,34,32,34;
 PIN_SWIZZLE_C0_DQ4[4]=3,7,5,6,2,4,0,8;

ASED065B32A_t0p4

BANK 2BT 1.2V		BANK 2BB 1.2V	
Byte Lane 7	Byte Lane 3	Byte Lane 7	Byte Lane 3
Byte Lane 6	Byte Lane 2	Byte Lane 6	Byte Lane 2
Byte Lane 5	Byte Lane 1	Byte Lane 5	Byte Lane 1
Byte Lane 4	Byte Lane 0	Byte Lane 4	Byte Lane 0

SWAP RULES:
 ADDS/ODD/CTRL signal locations are fixed and cannot be swapped

Please refer to Agilex EMIF User Guide for pin assignment rules.

[illegible]

A5ED065BB32A 1p04

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Title	AGILEX 5 E-SERIES 085B PREMIUM DEV KIT (PRODUCTION)
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AGILEX 5 E-SERIES 0838 PREMIUM DEV KIT (PRODUCTION)

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C	150-0330713-A3
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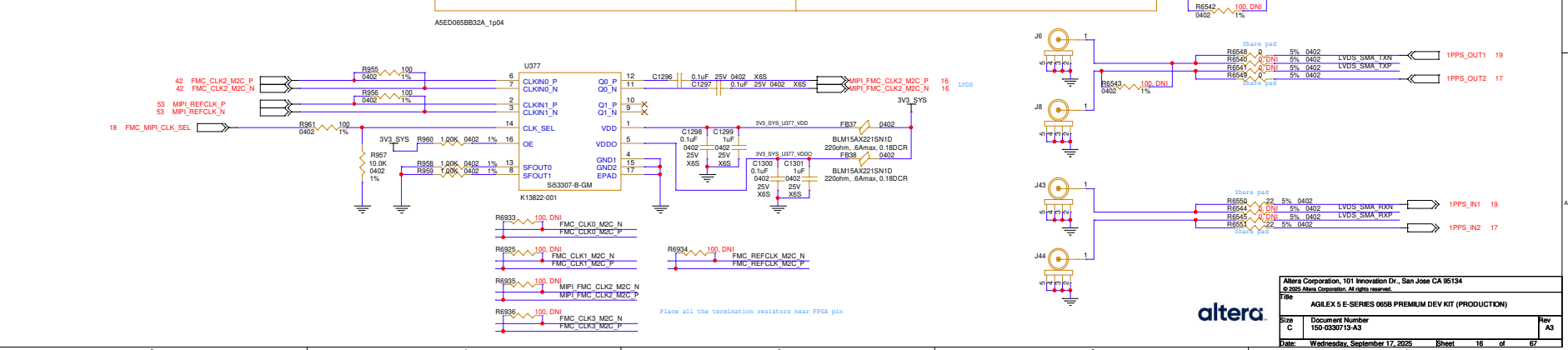
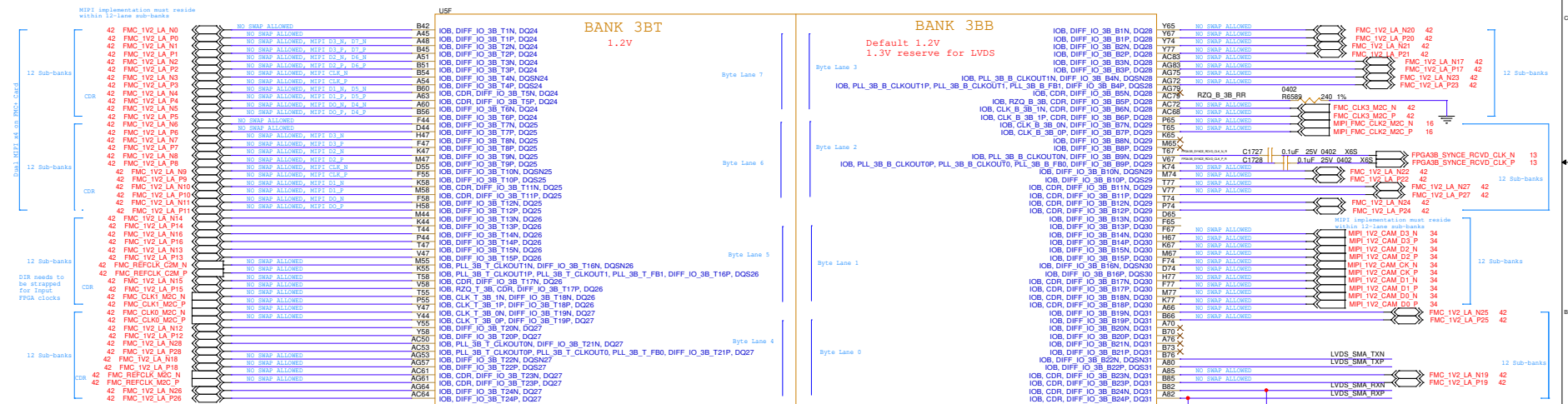
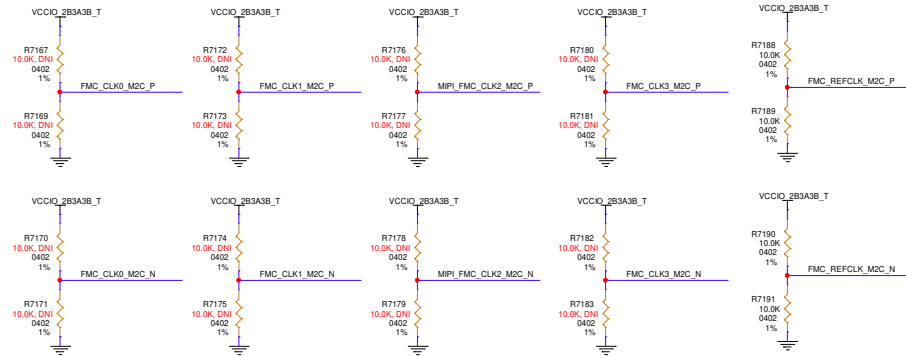
Pin placement restriction for MIPI & LVDS mixing with LVCMOS:

Restricted Pin Used As LVCMOS		Pin Index	Pin Number
IO Lane Used for MIPI	Width	P26	V77
	1 data + 1 clock	P26	V77
	2 data + 1 clock	P26, P10	V77, B66
IO Lane 6	Width	P75, P87	K58, B60
	1 data + 1 clock	P87	B60
	2 data + 1 clock	P87, P70, P82	B60, K44, D44
IO Lane 7	Width	P86; P2 from Bank 3A	A63, B130
	1 data + 1 clock	P77; P2 from Bank 3A	D55, B130
	2 data + 1 clock	P77, P83, P94; P2 from Bank 3A	D55, F44, A45, B130
IO Lane 6 and 7	Width	P70, P82, P83, P89, P94	K44, D44, F44, B54, A45
	8 data + 1 clock		

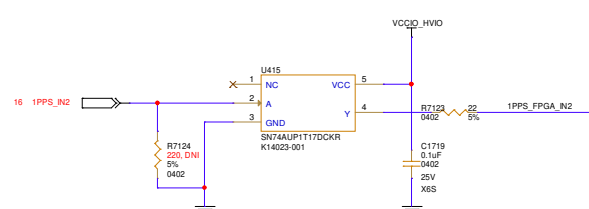
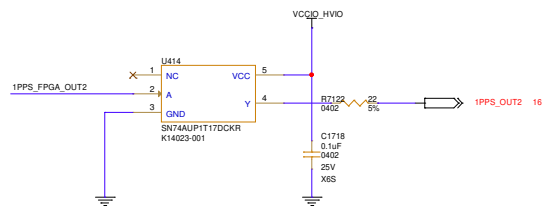
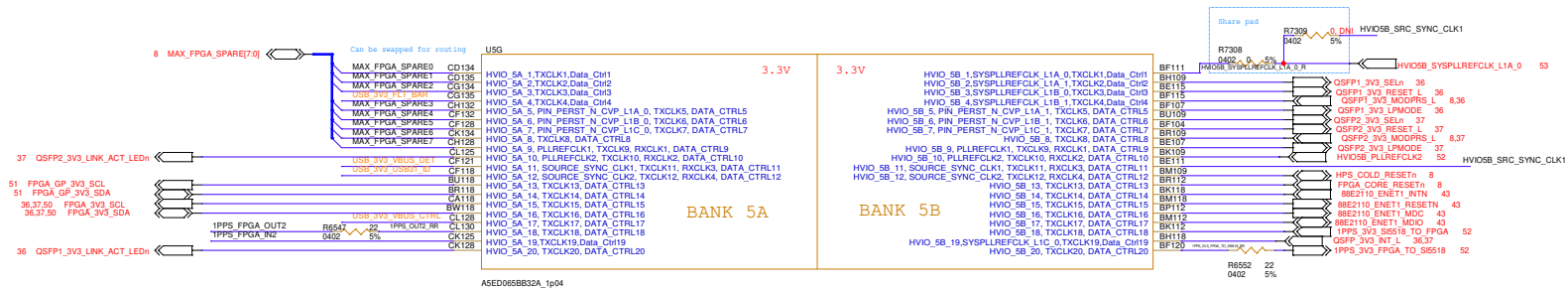
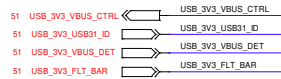
Restricted Pin Used As LVCMOS		Pin Index	Pin Number
IO Lane 0	Function	P3	A85
	LVDS_SMA_RX		
IO Lane 2	Function	P43	AC83
	LVDS_SMA_TX		
IO Lane 3	Function	P38, P41	AC79 (R2Q), AG75
	FPGA3B_SYNCN_RCVD_CLK		
IO Lane 4	Function	P40, P48	AG72, AC64
	FPGA3B_SYNCN_RCVD_CLK		
IO Lane 5	Function	P57, P67	Y55, T47
	FPGA3B_SYNCN_RCVD_CLK		
IO Lane 6	Function	P62	V58
	FPGA3B_SYNCN_RCVD_CLK		
IO Lane 7	Function	P74	M58
	FPGA3B_SYNCN_RCVD_CLK		

NOTES: Please check the detail restriction guide from IO Pinout Guideline Document if any of the FMC_V2_LA_* to be used as LVDS.

HSIO BANKS 3BL AND 3BR



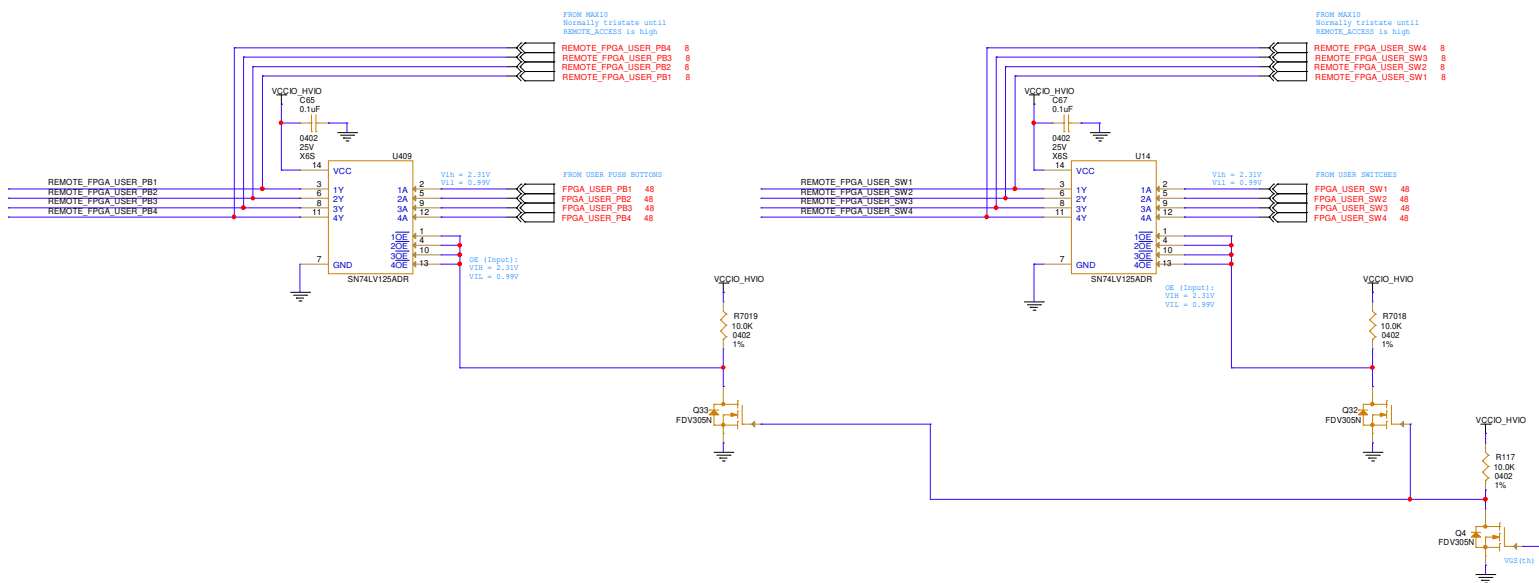
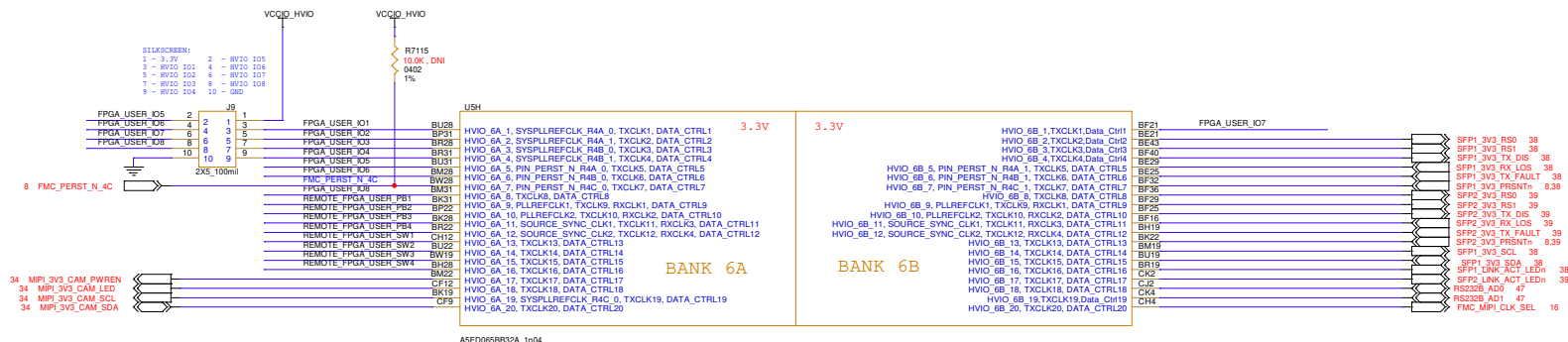
HVIO BANKS 5A AND 5B



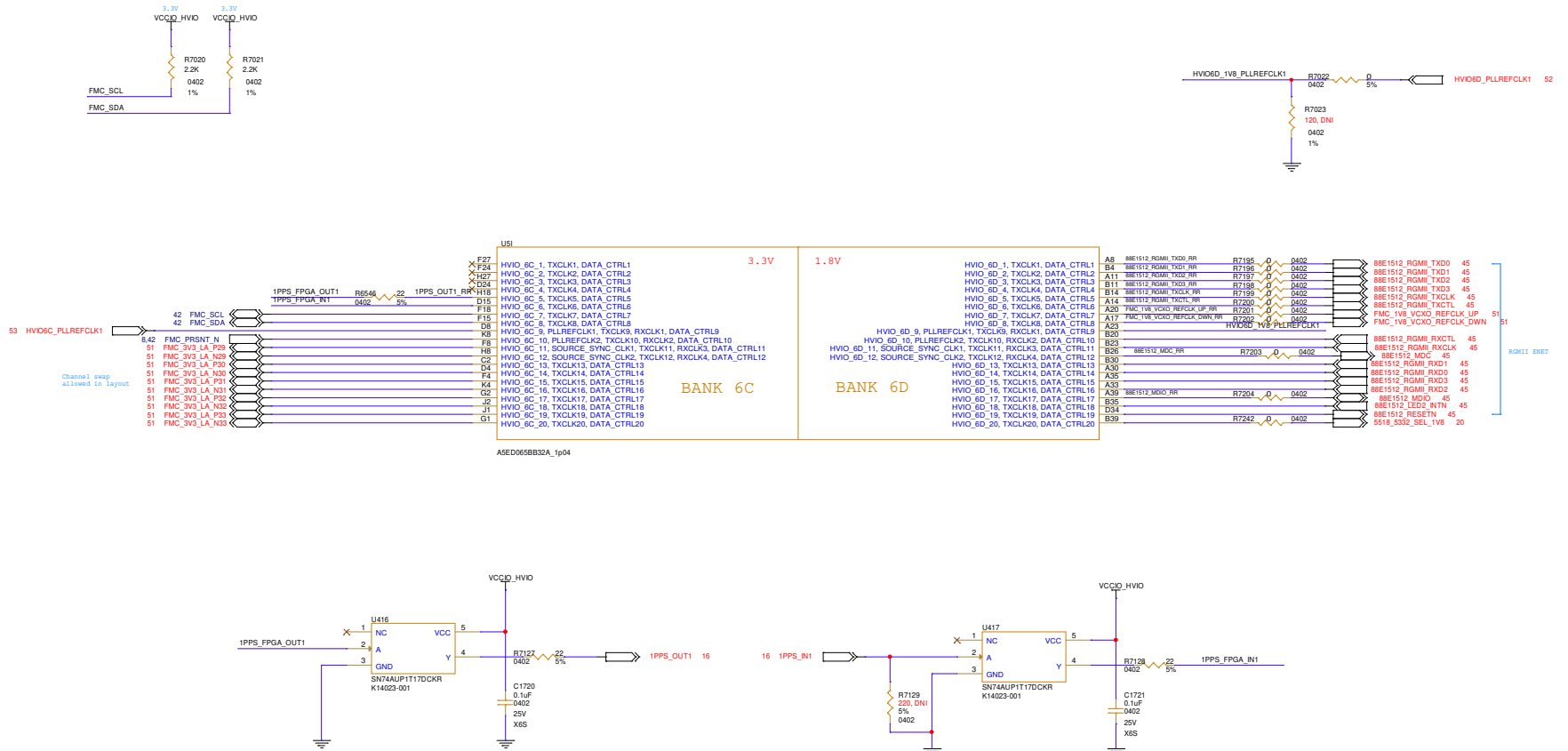
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HVIO BANKS 6A AND 6B



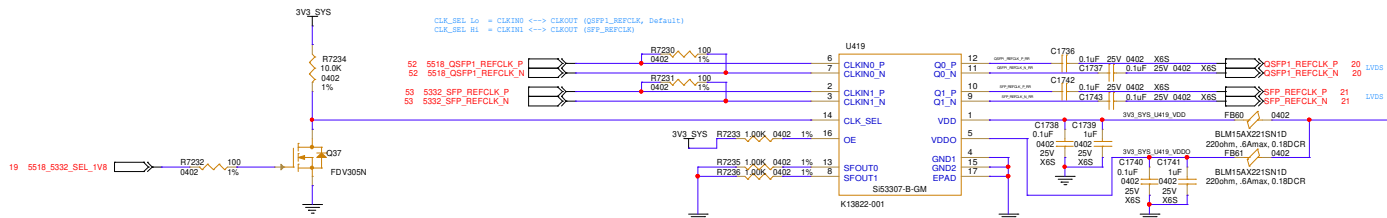
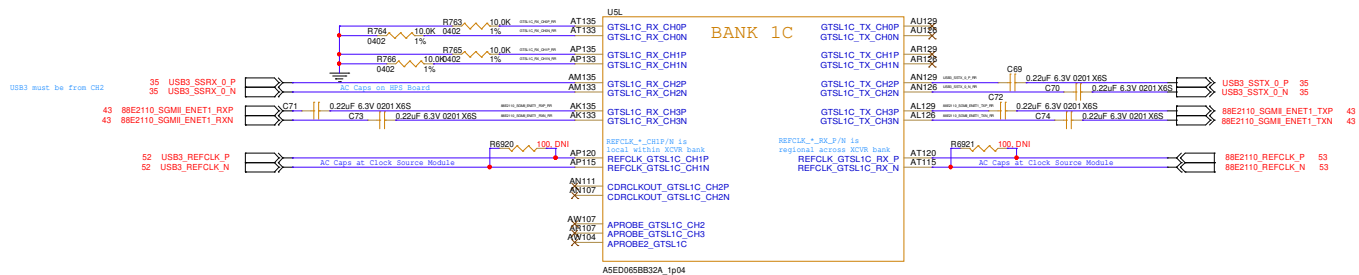
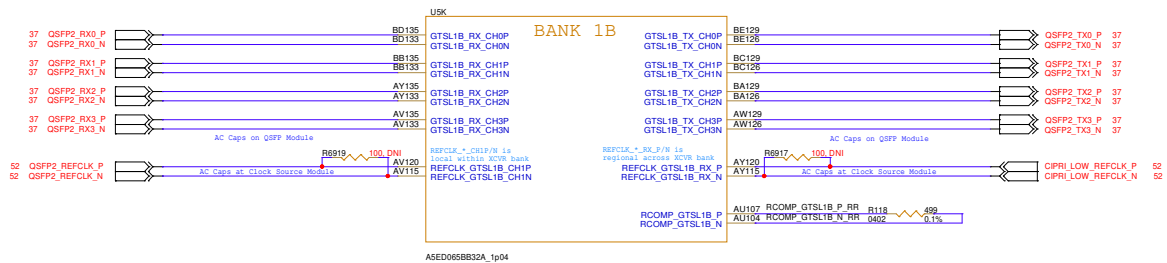
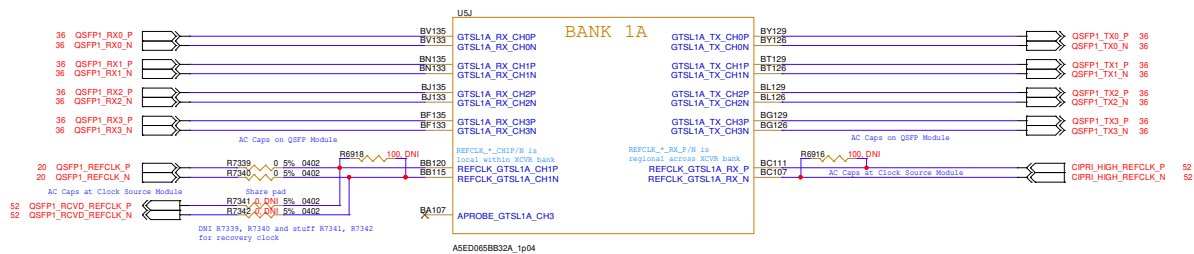
HVIO BANKS 6C AND 6D



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XCVR BANKS 1A, 1B, 1C



	U5M	
B	GTSR4A_RX_CH0P GTSR4A_RX_CH0N	BANK 4A



Pin option for recovery clock out to SMA connector.
It can be input to clock cleaner U67 IN1 with resistor option
Since the SMA already AC couple, C1313/1314 just need a jumper

FMC+ 57.4 SPEC, Rule 5.1.1 9: If AC coupling is required for DP[0..31]_M2C, DP[0..31]C2M signals, this shall be provided on the mezzanine module.

FMC+ 57.4 SPEC, Rule 5.1.1 9: If AC coupling is required for DP[0..31]_M2C, DP[0..31]C2M signals this shall be provided on the mezzanine module.



For GBTCLK input to regional clock
Stuff R7347, R7351, R7352, R7353.
Hwstuff R7345, R7346, R7349, R7350

DNU & NC PINS

USP	
CL101	DNU CL101
CK101	DNU CK101
CK103	DNU CK103
CL106	DNU CL106
AM120	DNU AM120
AL115	DNU AL115
BD64	DNU BD64
BD53	DNU BD53
AL68	DNU AL68
AL57	DNU AL57
BD120	DNU BD120
RC40	DNU RC40
AL43	DNU AL43
BA104	DNU BA104
BA32	DNU BA32
AR104	DNU AR104
AF32	DNU AF32
BD100	DNU BD100
BD36	DNU BD36
BD40	DNU BD40
BC100	DNU BC100
BC36	DNU BC36
AM36	DNU AM36

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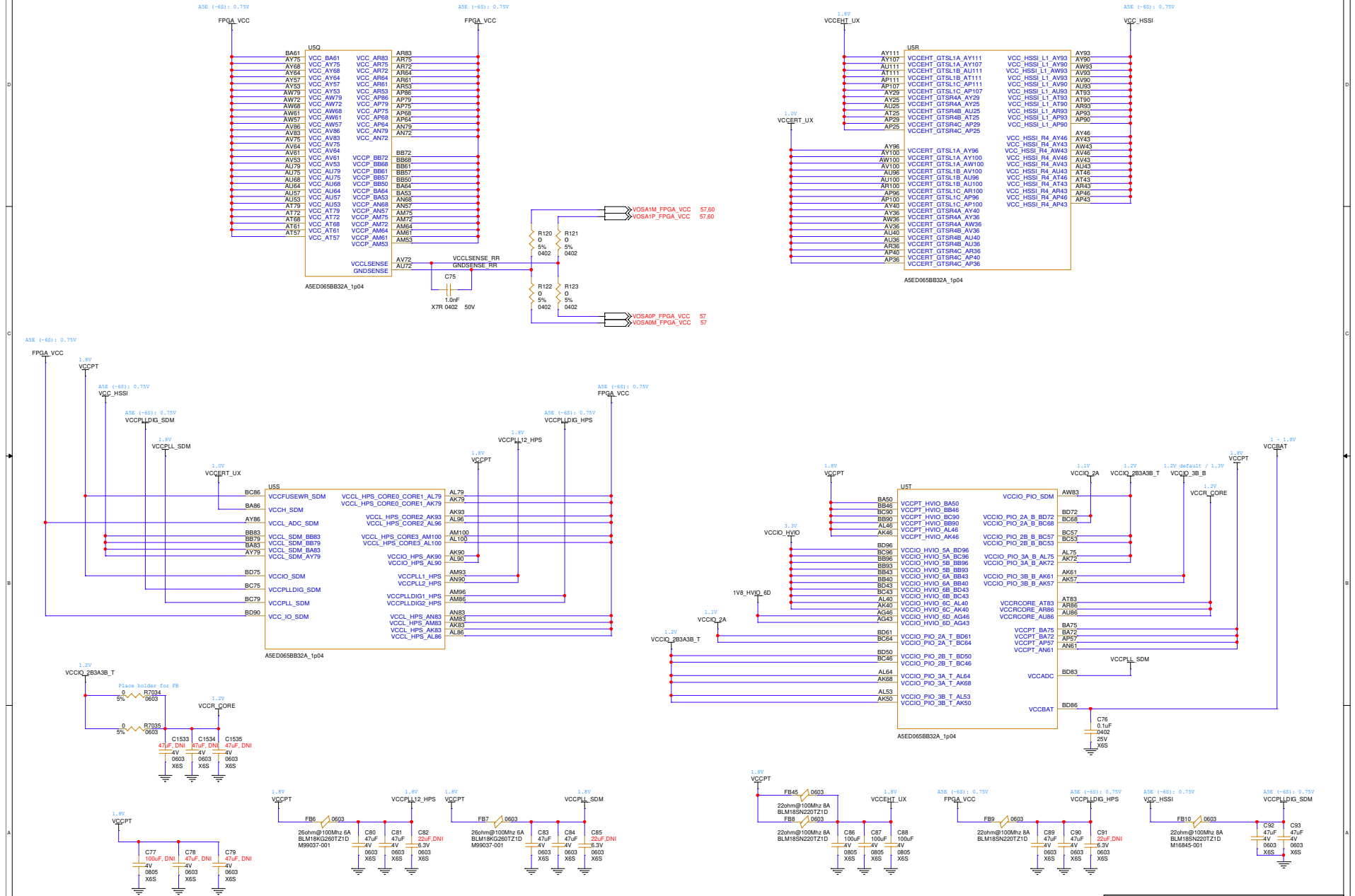
USX	
Y8	NC Y8
Y37	NC Y37
Y34	NC Y34
Y27	NC Y27
Y24	NC Y24
Y18	NC Y18
Y15	NC Y15
W2	NC W2
W1	NC W1
V8	NC V8
V37	NC V37
V34	NC V34
V27	NC V27
V24	NC V24
V18	NC V18
U2	NC U2
U1	NC U1
T8	NC T8
T4	NC T4
T34	NC T34
T27	NC T27
T24	NC T24
T18	NC T18
T15	NC T15
R2	NC R2
P4	NC P4
P24	NC P24
P15	NC P15
N2	NC N2
M8	NC M8
M4	NC M4
M34	NC M34
M27	NC M27
M24	NC M24
M18	NC M18
M15	NC M15
L1	NC L1
K34	NC K34
K27	NC K27
K24	NC K24
K18	NC K18
K15	NC K15
H37	NC H37
H34	NC H34
BD16	NC BD16
AY50	NC AY50
NC AW50	AW50
NC AP53	AP53
NC AP50	AP50
NC AN50	AN50
NC AM50	AM50
NC AM16	AM16
NC AL32	AL32
NC AL28	AL28
NC AL25	AL25
NC AL16	AL16
NC AL104	AL104
NC AK32	AK32
NC AK25	AK25
NC AK21	AK21
NC AJ2	AJ2
NC AJ1	AJ1
NC AH8	AH8
NC AH4	AH4
NC AG4	AG4
NC AG36	AG36
NC AG28	AG28
NC AG21	AG21
NC AG16	AG16
NC AF2	AF2
NC AD2	AD2
NC AD1	AD1
NC AC4	AC4
NC AC36	AC36
NC AB4	AB4
NC AB2	AB2
NC AB1	AB1
NC AB11	AB11
NC AA1	AA1
NC AU50	AU50
NC AT50	AT50
NC AR50	AR50
NC AM40	AM40
NC AM43	AM43

ASED065B32A_1p04

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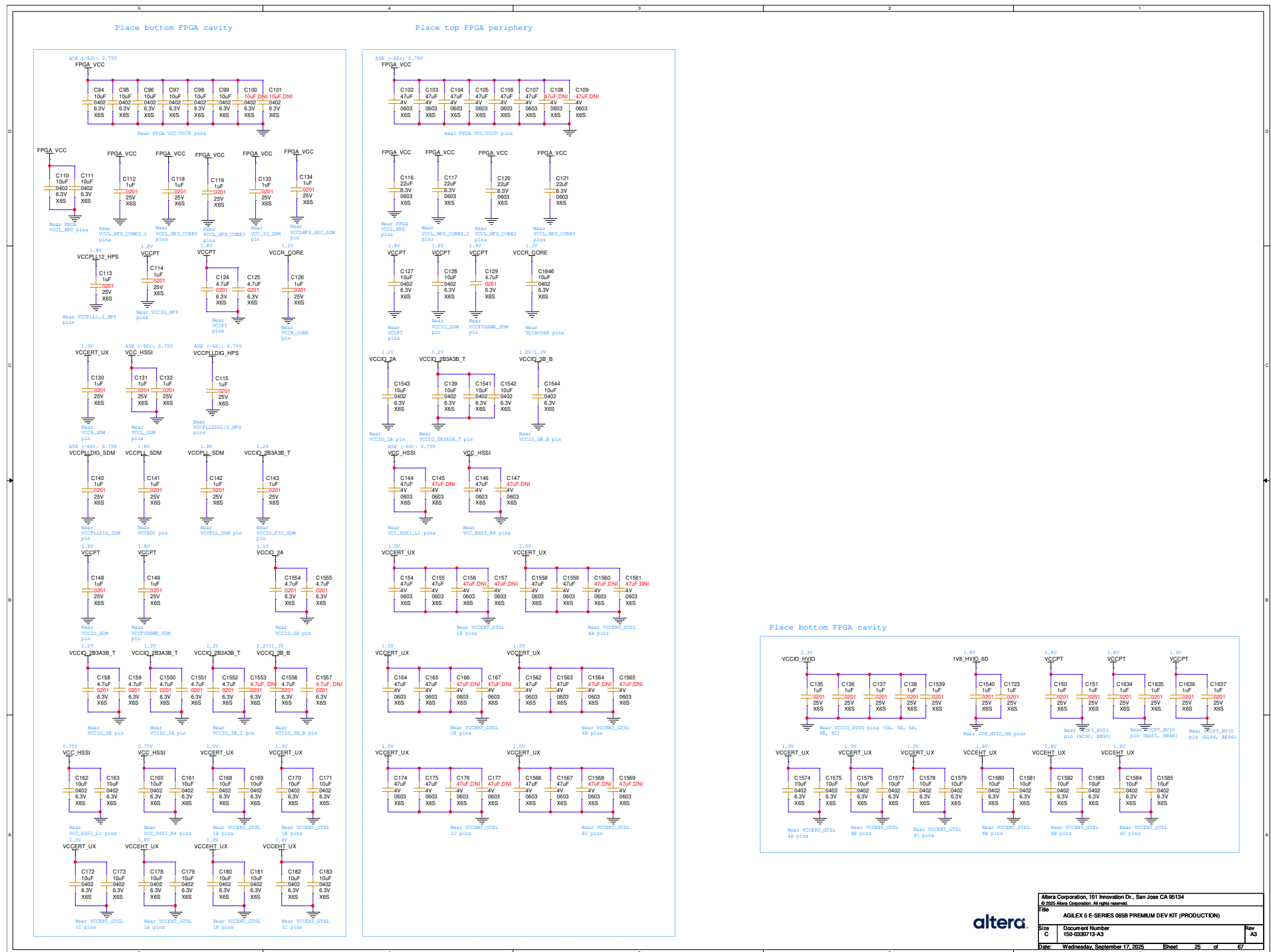
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File AGILEX 5 E-SERIES 065B PREMIUM DEV KIT (PRODUCTION)			
Size C	Document Number 160-0300715-A3	Rev A3	
Date: Wednesday, September 17, 2005	Sheet 22 of 67		

FPGA POWER

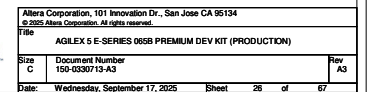


A5ED065BB32A_1p04





LPDDR4_DQ[31:0]	13
LPDDR4_DM[3:0]	13
LPDDR4_DQS_P[3:0]	13
LPDDR4_DQS_N[3:0]	13
LPDDR4_CA[5:0]	13
LPDDR4_CK_P	13
LPDDR4_CK_N	13
LPDDR4_RESET_N	13
LPDDR4_CS_N0	13
LPDDR4_CKE_R0	13



BOM NOTES:

- Mono Die -> DNI
- Twin Die -> stuff 0 Ohm

BOM NOTES:

- Mono Die -> stuff 0 Ohm
- Twin Die -> DNI

BOM NOTES:

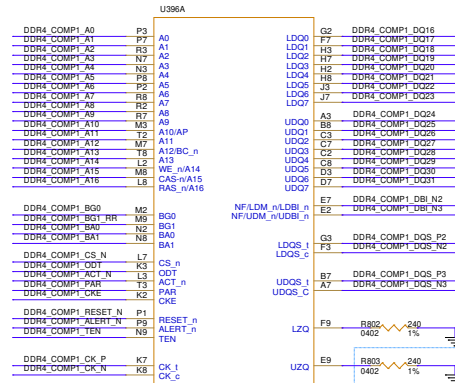
- Mono Die -> stuff 0 Ohm
- Twin Die -> stuff 240 Ohm

Date	Description	Rev
Wednesday, September 17, 2025 <td>Sheet 27 of 67</td> <td>A3</td>	Sheet 27 of 67	A3

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AGILEX E-SERIES 065B PREMIUM DEV KIT (PRODUCTION)
 Document Number 150-0330713-A3
 Date: Wednesday, September 17, 2025 Sheet 27 of 67 Rev A3

8GB DDR4 COMP1 BYTE 2-3

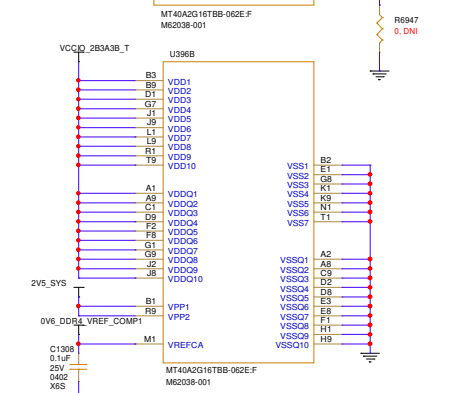
DDR4 COMP1_B00_	14,27,29	DDR4 COMP1_DQ[31:16]	14
DDR4 COMP1_BA[1:0]	14,27,29	DDR4 COMP1_DBI_N[3:2]	14
DDR4 COMP1_A[16:0]	14,27,29	DDR4 COMP1_DQS_P[3:2]	14
DDR4 COMP1_CS_N	14,27,29	DDR4 COMP1_DQS_N[3:2]	14
DDR4 COMP1_ODT	14,27,29	DDR4 COMP1_RESET_N	14,27,29
DDR4 COMP1_A[1:1]	14,27,29	DDR4 COMP1_CK_P	13,27,29
DDR4 COMP1_PAR	14,27,29	DDR4 COMP1_CK_N	14,27,29
DDR4 COMP1_CSE	14,27,29	DDR4 COMP1_TEN	27,29
DDR4 COMP1_TEN	27,29		
DDR4 COMP1_B[1:0]	27,29		



MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)

For Mono Die device, Pin E9 = GND; M9 = GND
For Twin Die device, Pin E9 = U2Q; M9 = B[1].

BCM NOTES:
Mono Die -> stuff 0 Ohm
Twin Die -> stuff 240 Ohm

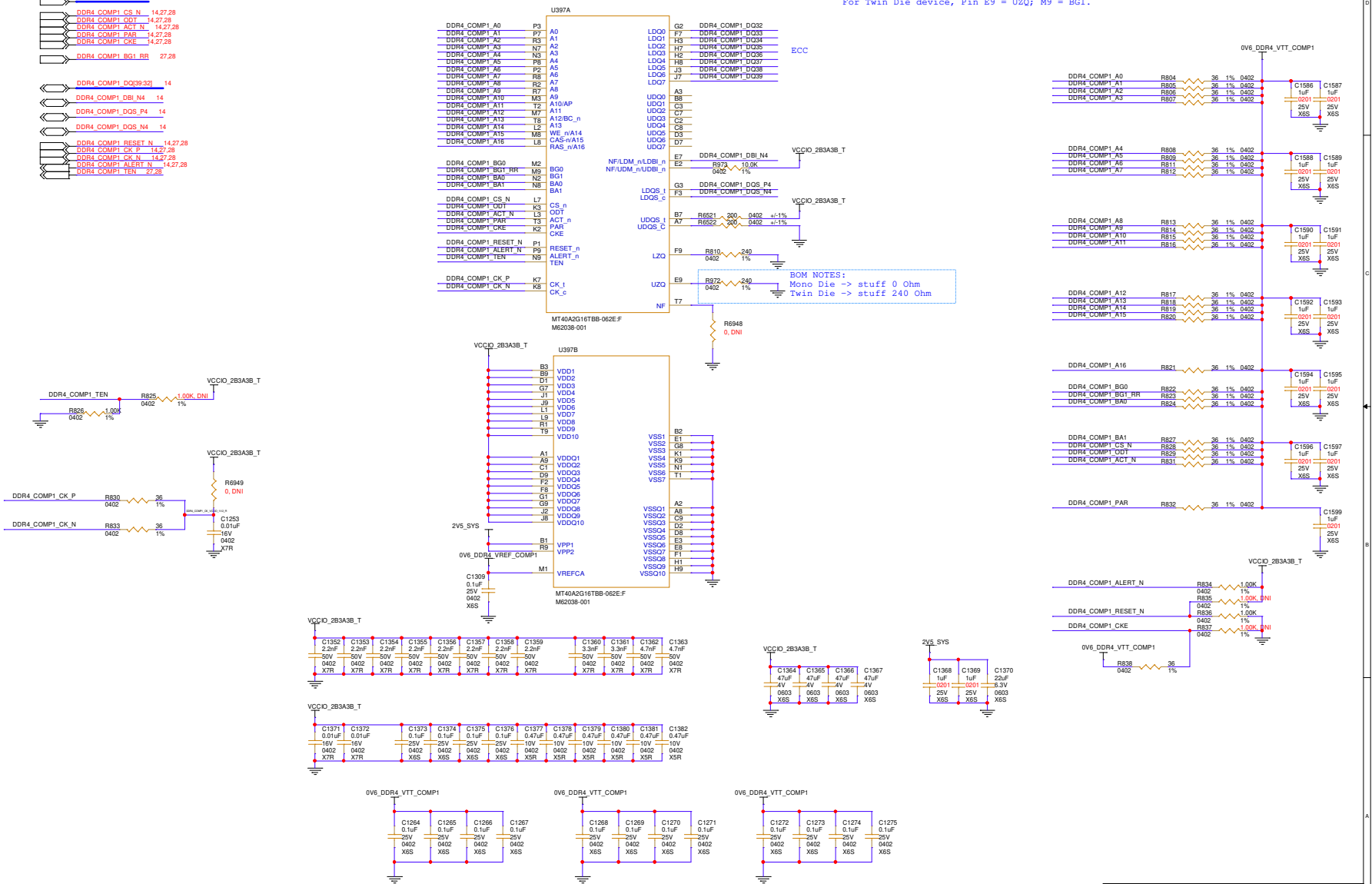


8GB DDR4 COMP1 BYTE ECC

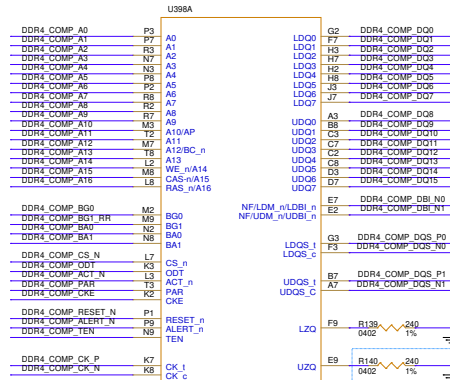
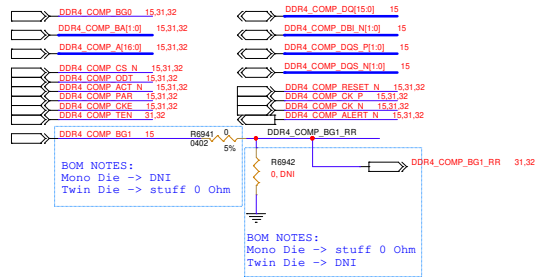
DDR4_COMP1_B0 14,27,28
 DDR4_COMP1_BA[1:0] 14,27,28
 DDR4_COMP1_A[16:0] 14,27,28
 DDR4_COMP1_CS_N 14,27,28
 DDR4_COMP1_ODT 14,27,28
 DDR4_COMP1_ACT_N 14,27,28
 DDR4_COMP1_PAR 14,27,28
 DDR4_COMP1_CKE 14,27,28
 DDR4_COMP1_B01_RR 27,28
 DDR4_COMP1_DQS[3:2] 14
 DDR4_COMP1_DBI_N4 14
 DDR4_COMP1_DQS_P4 14
 DDR4_COMP1_DQS_N4 14
 DDR4_COMP1_RESET_N 14,27,28
 DDR4_COMP1_CK_P 14,27,28
 DDR4_COMP1_CK_N 14,27,28
 DDR4_COMP1_ALERT_N 14,27,28
 DDR4_COMP1_TEN 27,28

MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)

For Mono Die device, Pin E9 = GND; M9 = GND
 For Twin Die device, Pin E9 = U2Q; M9 = BG1.

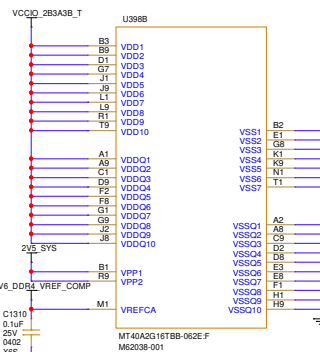


HPS 8GB DDR4 COMPONENT BYTE 0-1

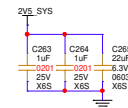
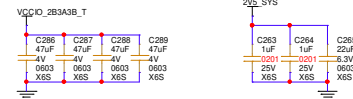
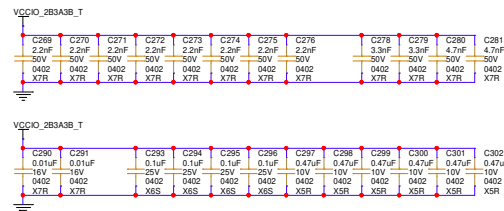


MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)
For Mono Die device, Pin E9 = GND; M9 = GND
For Twin Die device, Pin E9 = UZQ; M9 = BG1.

MT40A2G16TB-062E.F
M62038-001

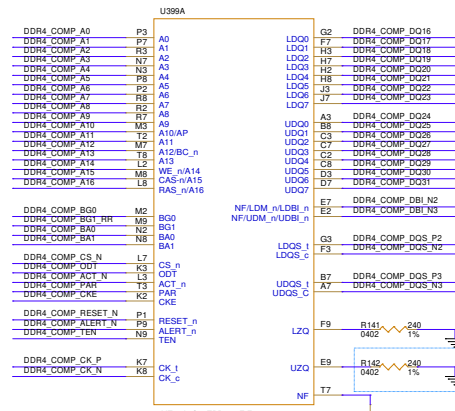
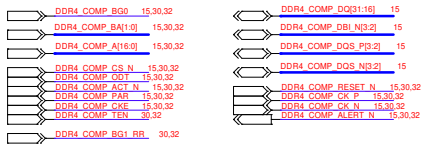


MT40A2G16TB-062E.F
M62038-001



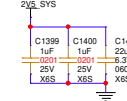
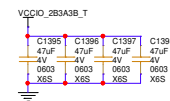
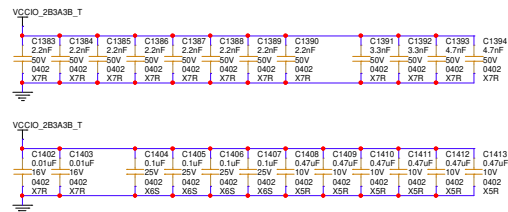
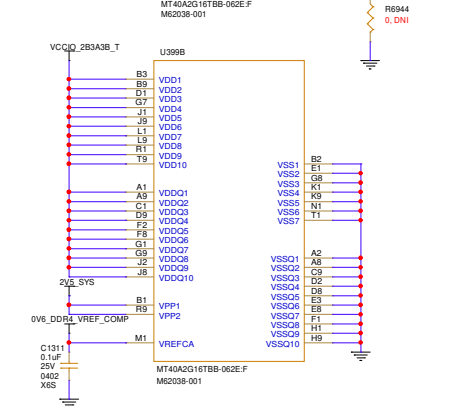
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HPS 8GB DDR4 COMPONENT BYTE 2-3



MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)

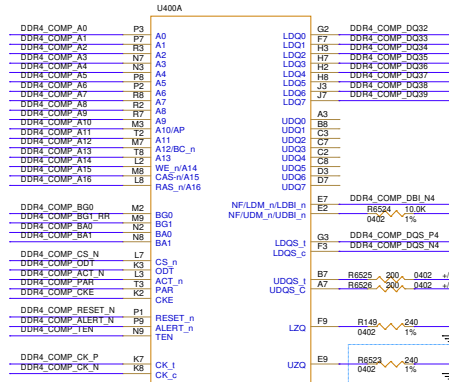
For Mono Die device, Pin E9 = GND; M9 = GND.
For Twin Die device, Pin E9 = UZQ; M9 = BG1.



HPS 8GB DDR4 COMPONENT BYTE ECC

DDR4_COMP_BG0 15,30,31
DDR4_COMP_BA[1:0] 15,30,31
DDR4_COMP_A[16:0] 15,30,31
DDR4_COMP_CS_N 15,30,31
DDR4_COMP_C0[7] 15,30,31
DDR4_COMP_ACT_N 15,30,31
DDR4_COMP_PAB 15,30,31
DDR4_COMP_CKE 15,30,31
DDR4_COMP_BG1_RR 30,31

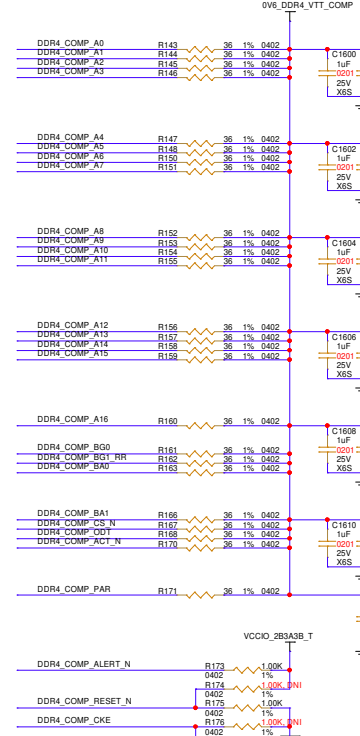
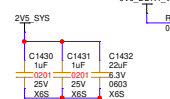
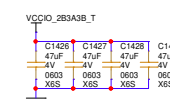
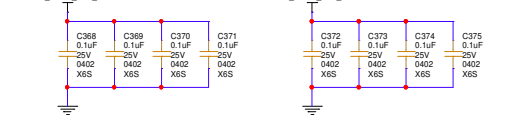
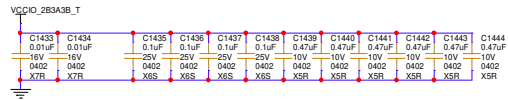
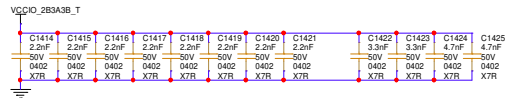
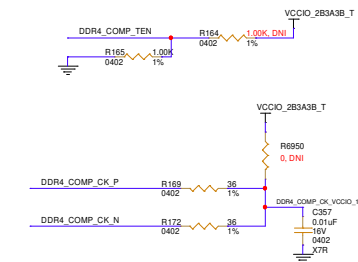
DDR4_COMP_DQ[3:31] 15
DDR4_COMP_DBI_N4 15
DDR4_COMP_DQS_P4 15
DDR4_COMP_DQS_N4 15
DDR4_COMP_RESET_N 15,30,31
DDR4_COMP_CK_P 15,30,31
DDR4_COMP_CK_N 15,30,31
DDR4_COMP_ALERT_N 15,30,31
DDR4_COMP_TEN 30,31



ECC

MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)
For Mono Die device, Pin E9 = GND; M9 = GND
For Twin Die device, Pin E9 = U2Q; M9 = BG1.

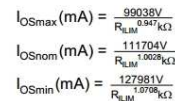
BOM NOTES:
Mono Die -> stuff 0 Ohm
Twin Die -> stuff 240 Ohm



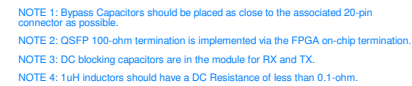
BLANK

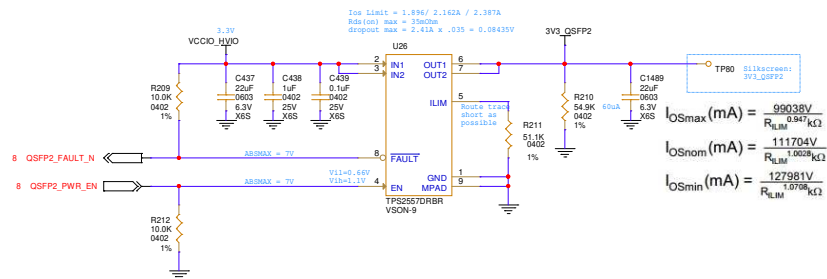


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50ohm Single Ended Z



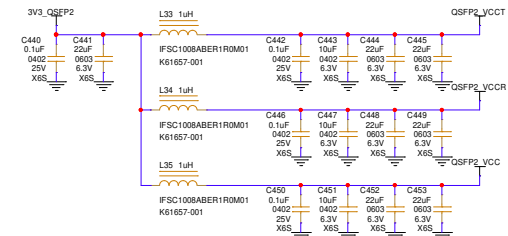


NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

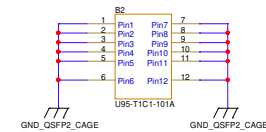
NOTE 2: zQSFP 100-ohm termination is implemented via the FPGA on-chip termination.

NOTE 3: DC blocking capacitors are in the module for RX and TX.

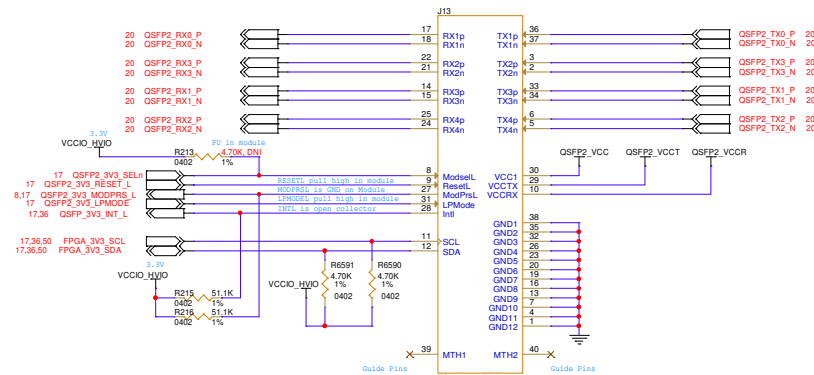
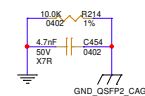
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



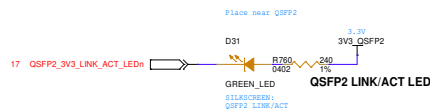
Place close to zQSFP Connector



Amphenol U95-T1C1-101A



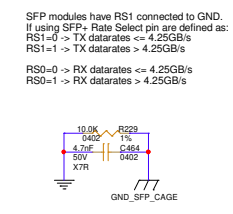
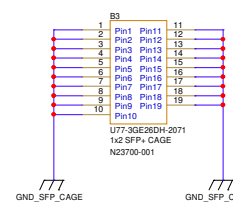
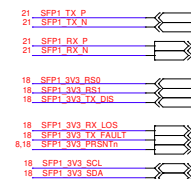
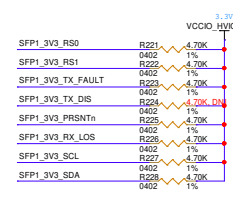
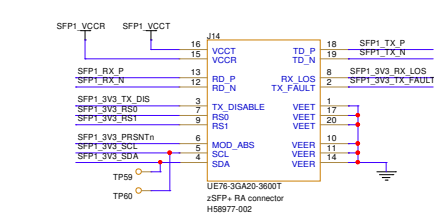
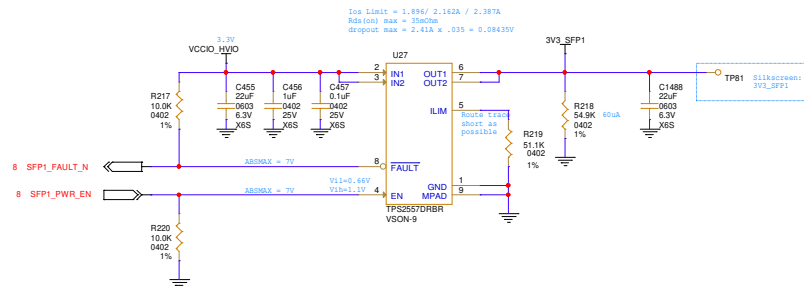
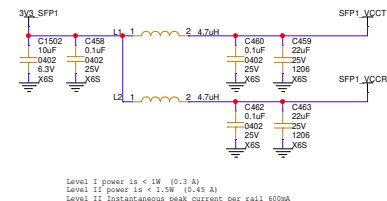
Amphenol FS1-K38-202A-A0



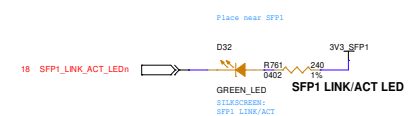
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

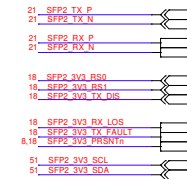
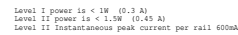
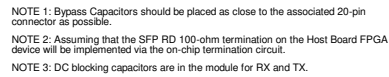
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

NOTE 3: DC blocking capacitors are in the module for RX and TX.



Optical (SFP+) Transceiver Cage 1x2

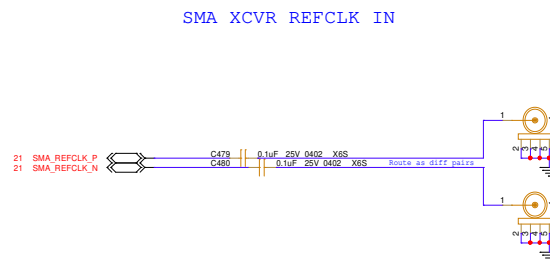
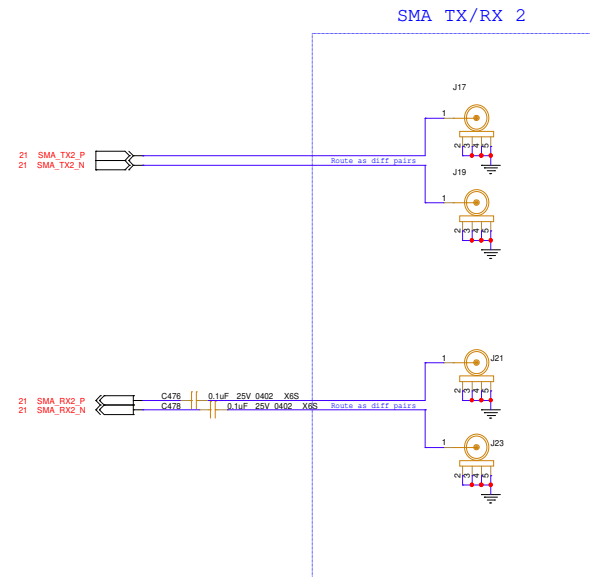
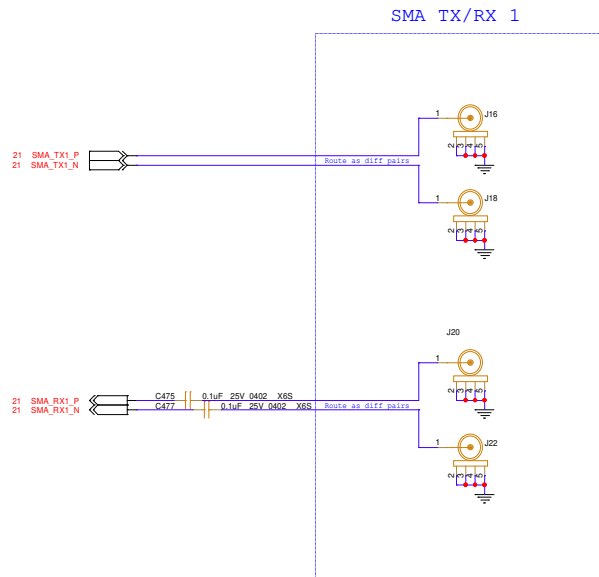




SFP modules have RS1 connected to GND.
If using SFP+ Rate Select pin are defined as:
RS1=0 -> TX datarates <= 4.25GB/s
RS1=1 -> TX datarates > 4.25GB/s

RS0=0 -> RX datarates <= 4.25GB/s
RS0=1 -> RX datarates > 4.25GB/s





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FMC+ Connector (Vita 57.4) Complete Pin Table

FMC Connector (Vita 57.1) Complete Pin Table

14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSN_T_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	GND	HA03_N	GND	LA00_N_CC	GND	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	HA07_N	LA04_N	LA03_N	HA08_N	HA09_N	GND	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	GND	HA11_N	GND	LA08_N	GND	HA13_N	LA05_N	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	GND	HA18_N	GND	LA16_N	GND	HA20_N	LA13_N	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	HA22_N	LA19_N	LA20_N	HB02_N	HB03_N	GND	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	GND	HB01_N	GND	LA22_N	GND	HB05_N	LA23_N	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	HB07_N	LA24_N	LA25_N	HB08_N	HB09_N	GND	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	GND	HB11_N	GND	LA29_N	GND	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	HB15_N	LA30_N	LA31_N	HB16_N	HB19_N	TRST_L	GA1	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	GND	HB18_N	GND	LA33_N	GND	HB21_N	3P3V	GND	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	DP5_C2M_P	GND	DP19_M2C_P	GND
39	DP19_C2M_N	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N	GND
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

FMC+ Voltage Specification

Voltage Supply	Allowable Voltage Range	No Pins	Max Amps	Tolerance	Max Capacitive Load
VADJ	0 - 3.3V	4	4	+/- 5%	1000 uF
VIO_B_M2C	0 - VADJ	2	1.15	+/- 5%	500 uF
VREF_A_M2C	0 - VADJ	1	1mA	+/- 2%	10 uF
VREF_B_M2C	0 - VIO_B_M2C	1	1mA	+/- 2%	10 uF
3P3VAUX	3.3V	1	20mA	+/- 5%	150 uF
3P3V	3.3V	5	3	+/- 5%	1000 uF
12P0V	12V	5	1	+/- 5%	1000 uF

Supported FMC Cards:

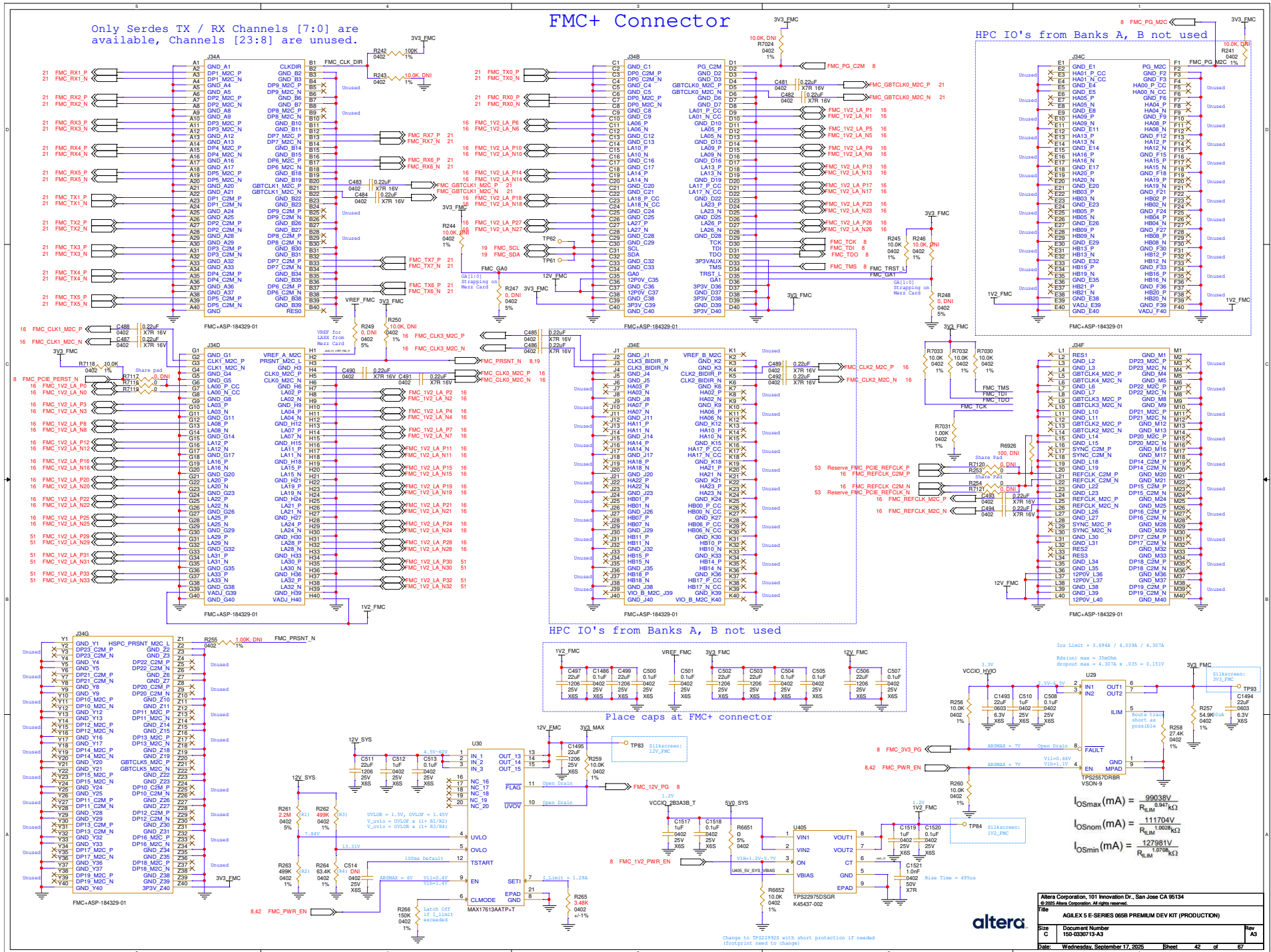
1. FMC+ PCIe Gen4 x16 RootPort Card (HighTech Global)
- ** Note: Only support PCIe Gen4 x4 **
2. FMC+ HDMI 2.1 Card Rev9 (Bitec)
3. FMC+ DP 1.4 Rev12 (Bitec)

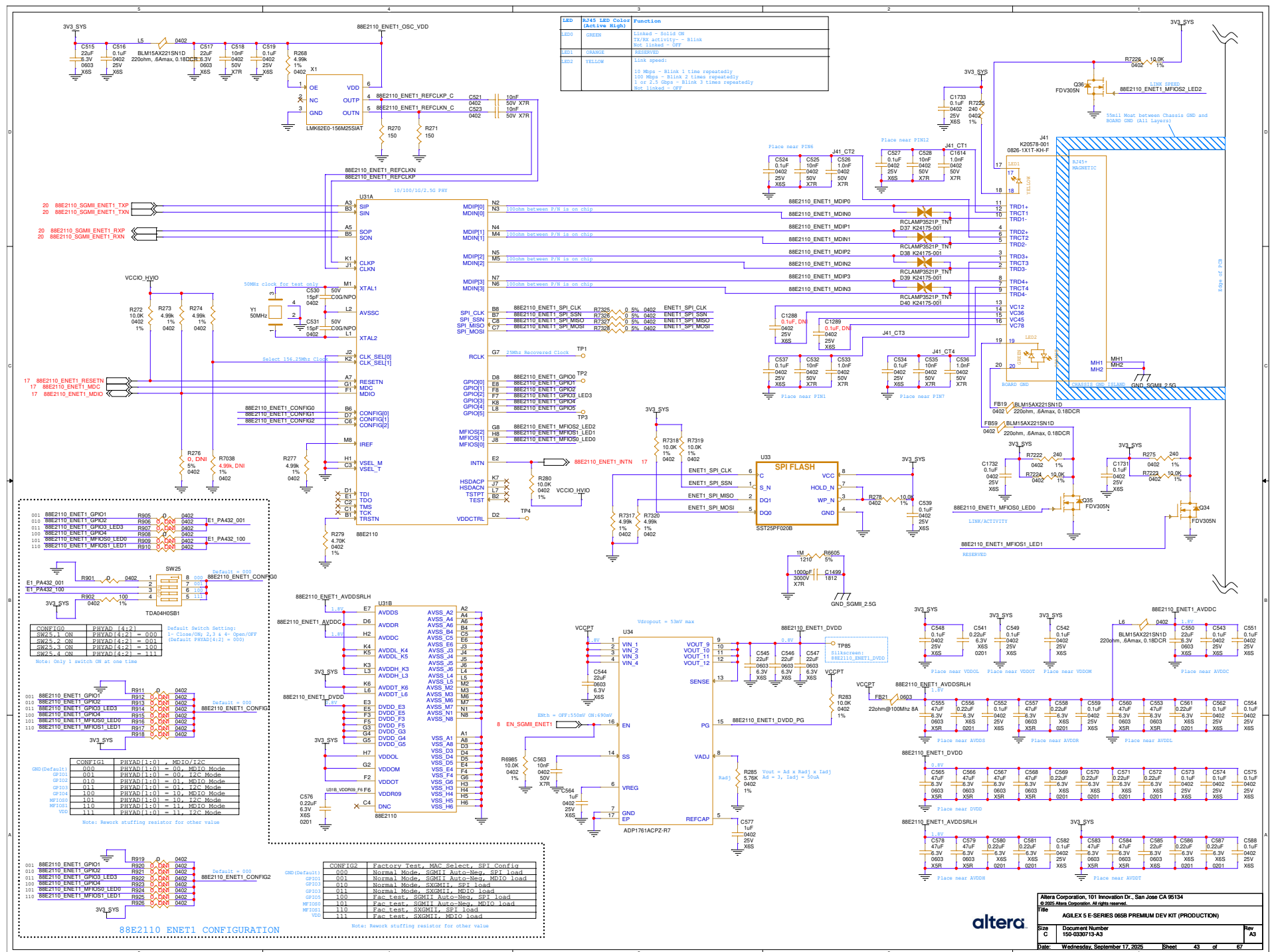
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Only Serdes TX / RX Channels [7:0] are available, Channels [23:8] are unused.

FMC+ Connector

HPC IO's from Banks A, B not used

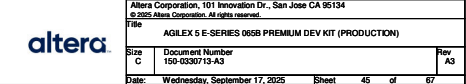


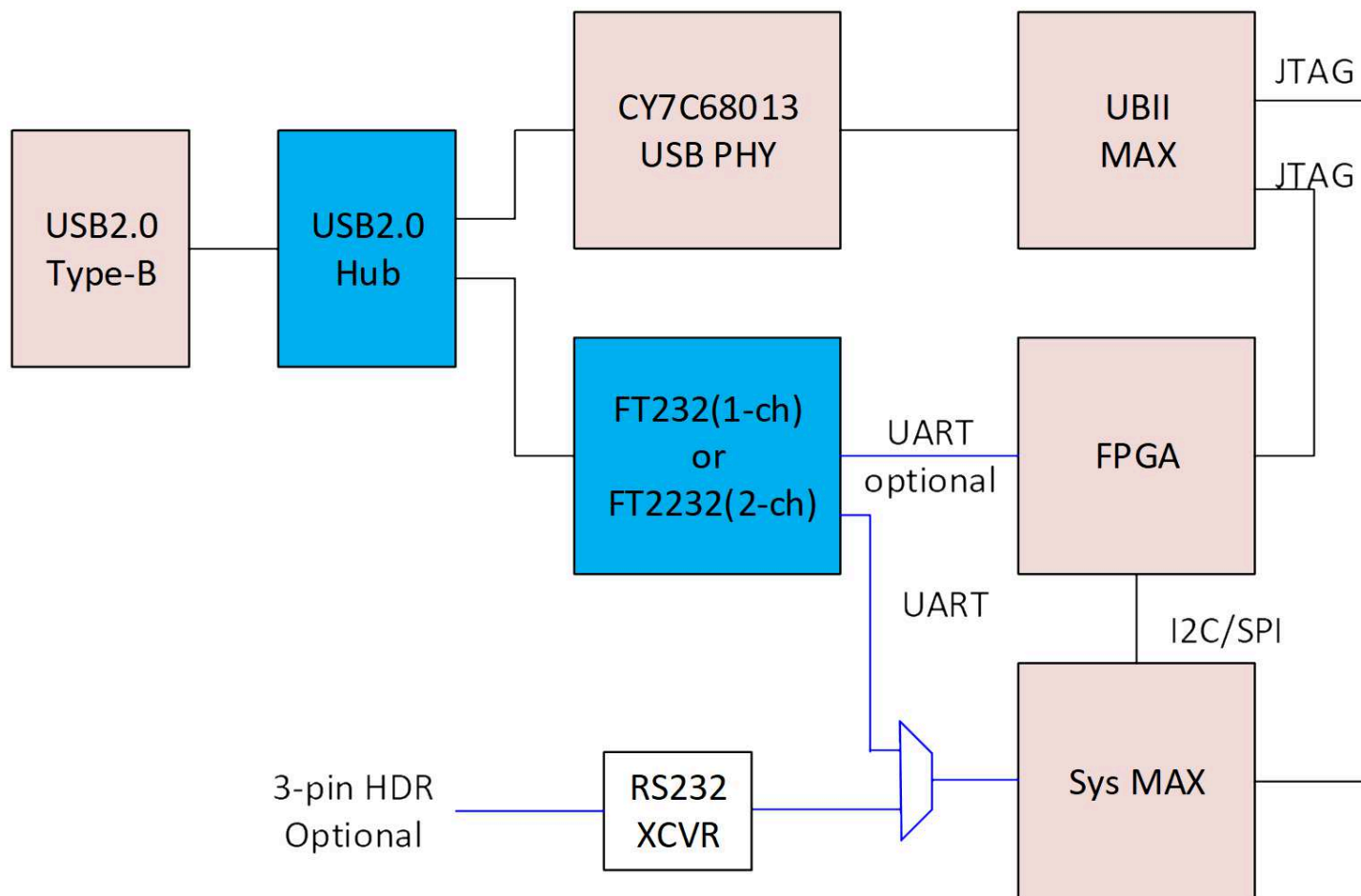


BLANK



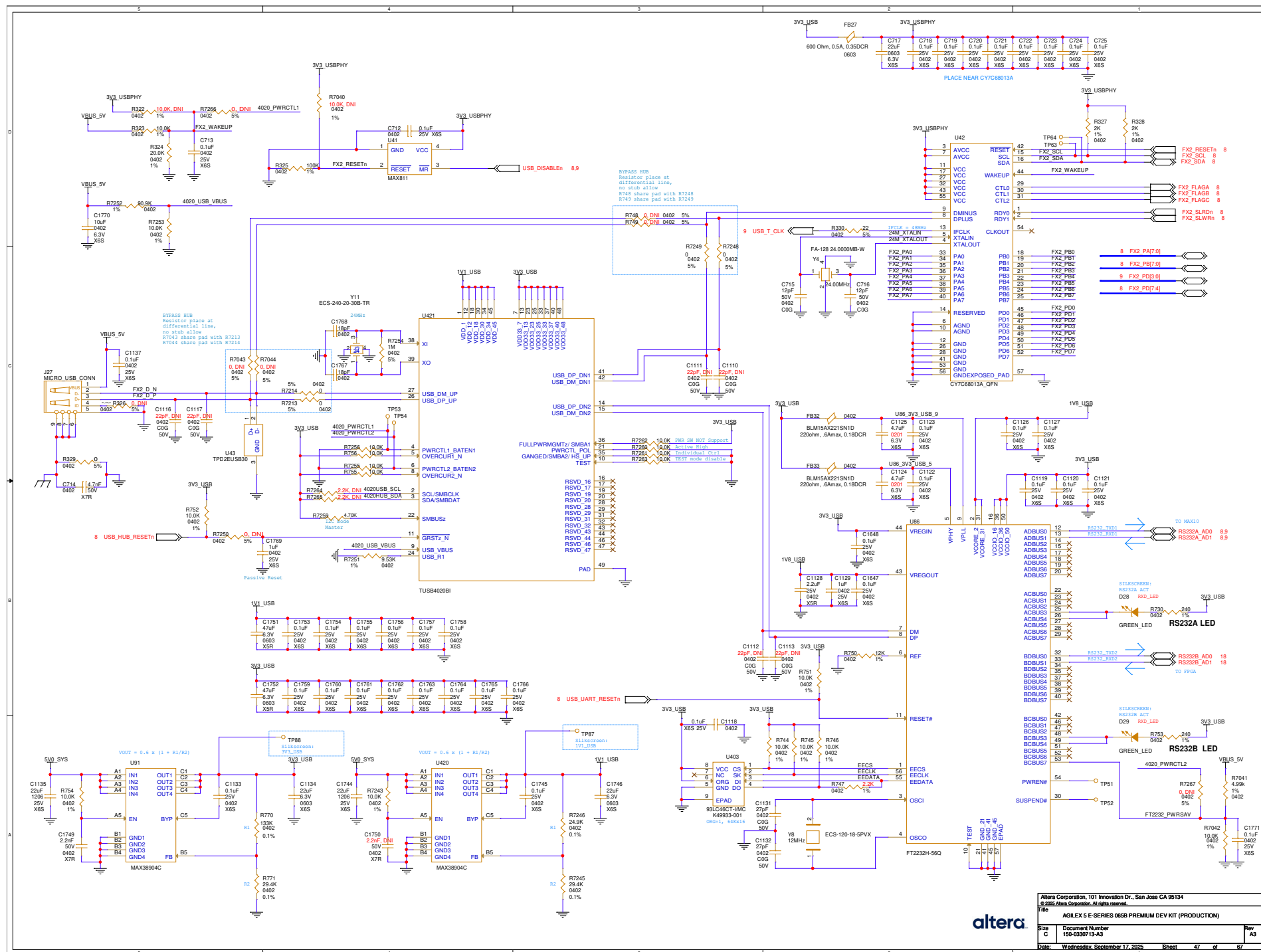
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File			
AGILEX 5 E-SERIES 005B PREMIUM DEV KIT (PRODUCTION)			
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	150-1030713-A3		A3
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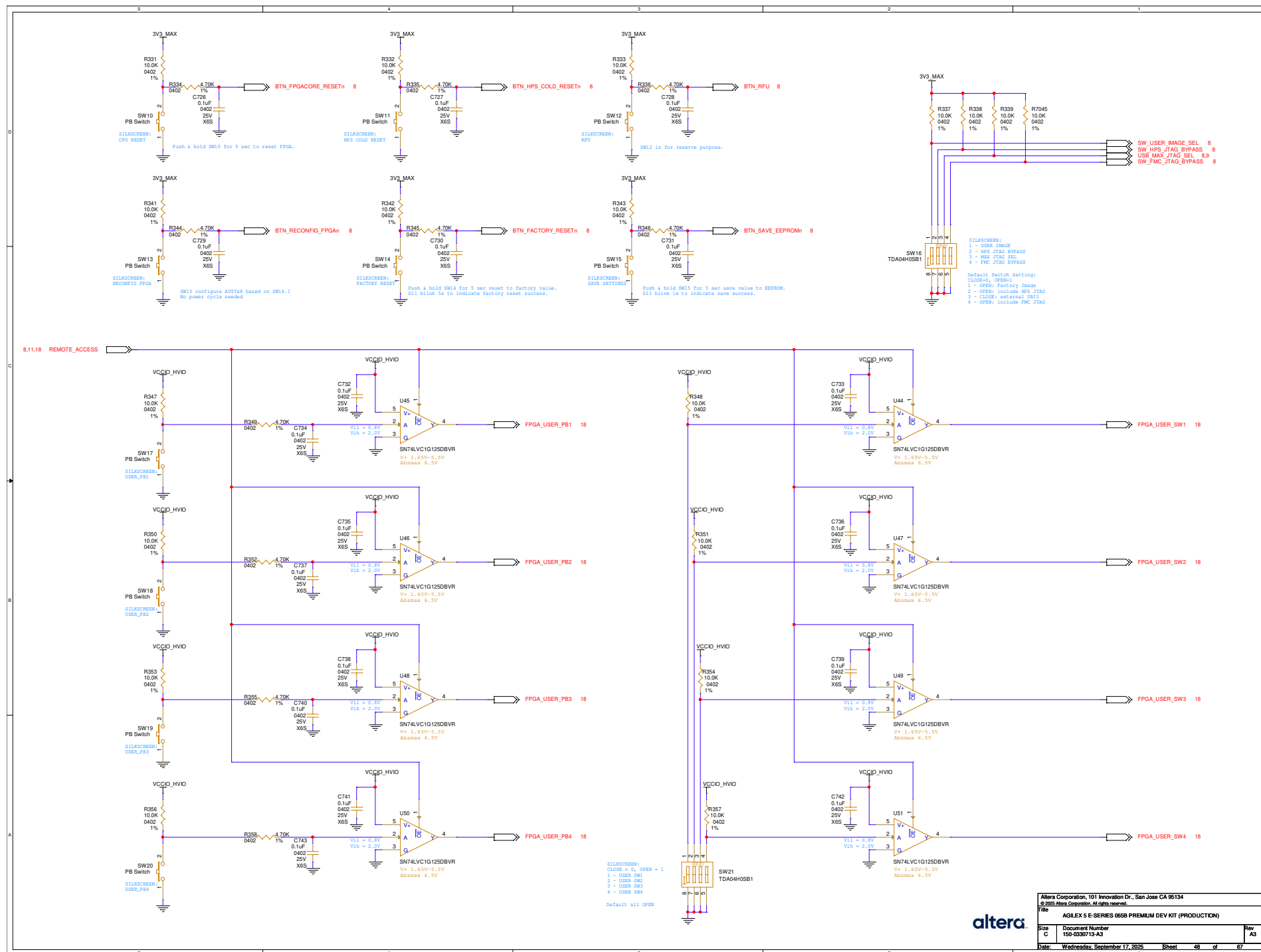


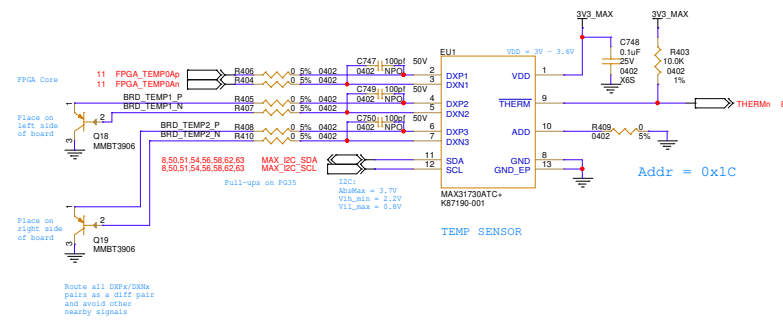
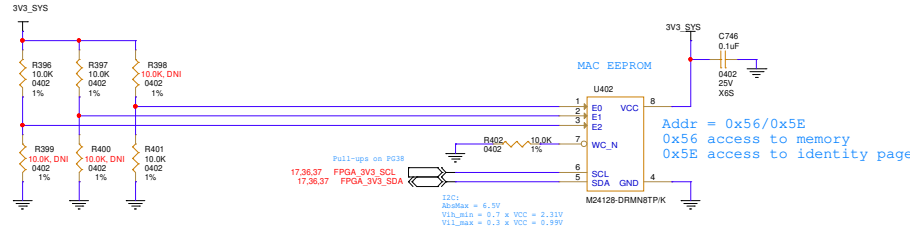
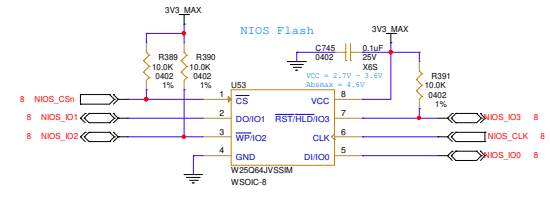
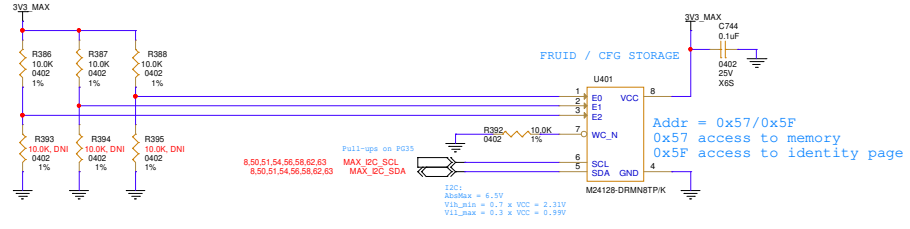


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File: AGILEX 5 E-SERIES 905B PREMIUM DEV KIT (PRODUCTION)			
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C	150-0330713-A3	A3	
Date:	Wednesday, September 17, 2025	Sheet	48 of 67

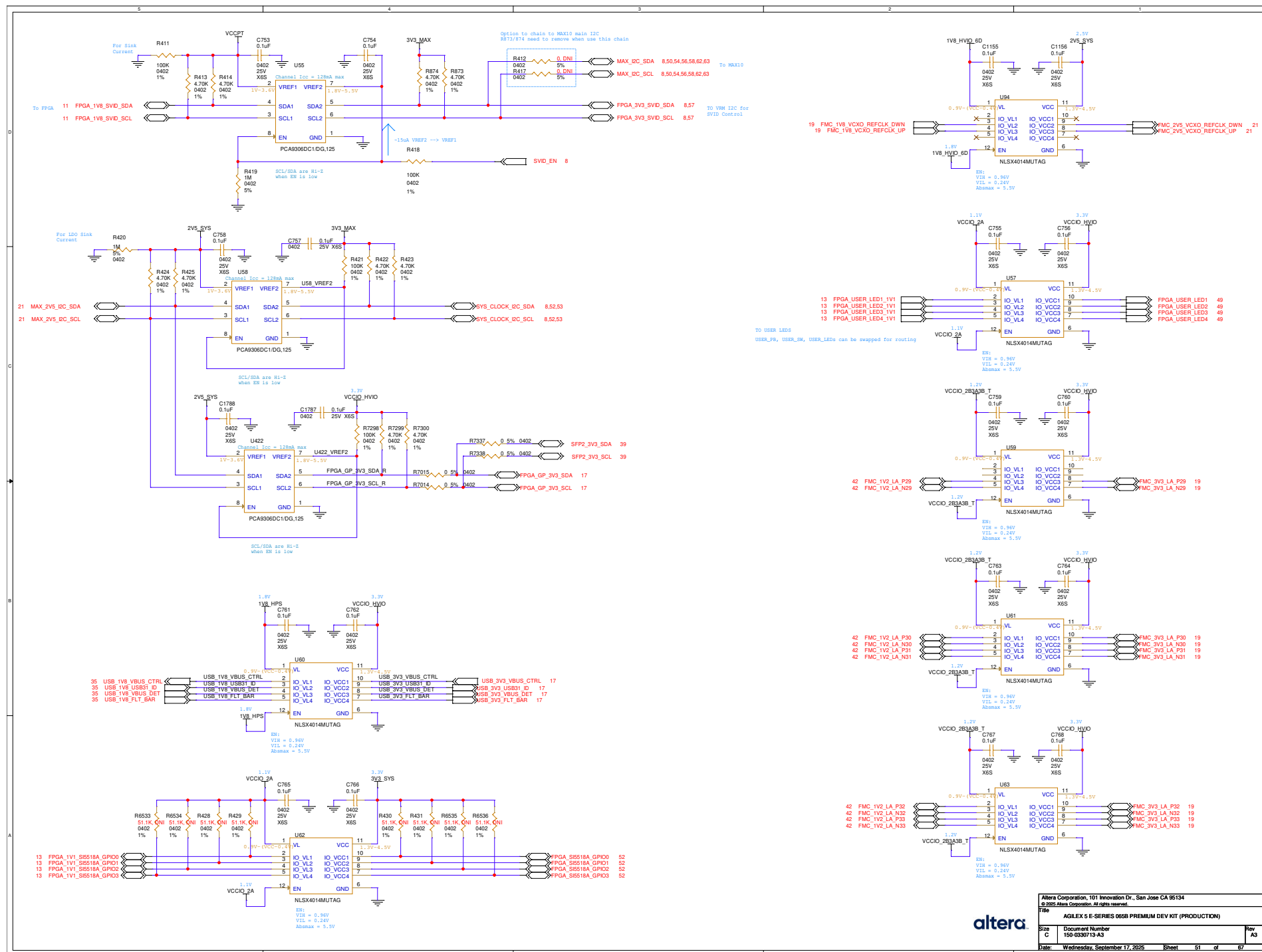


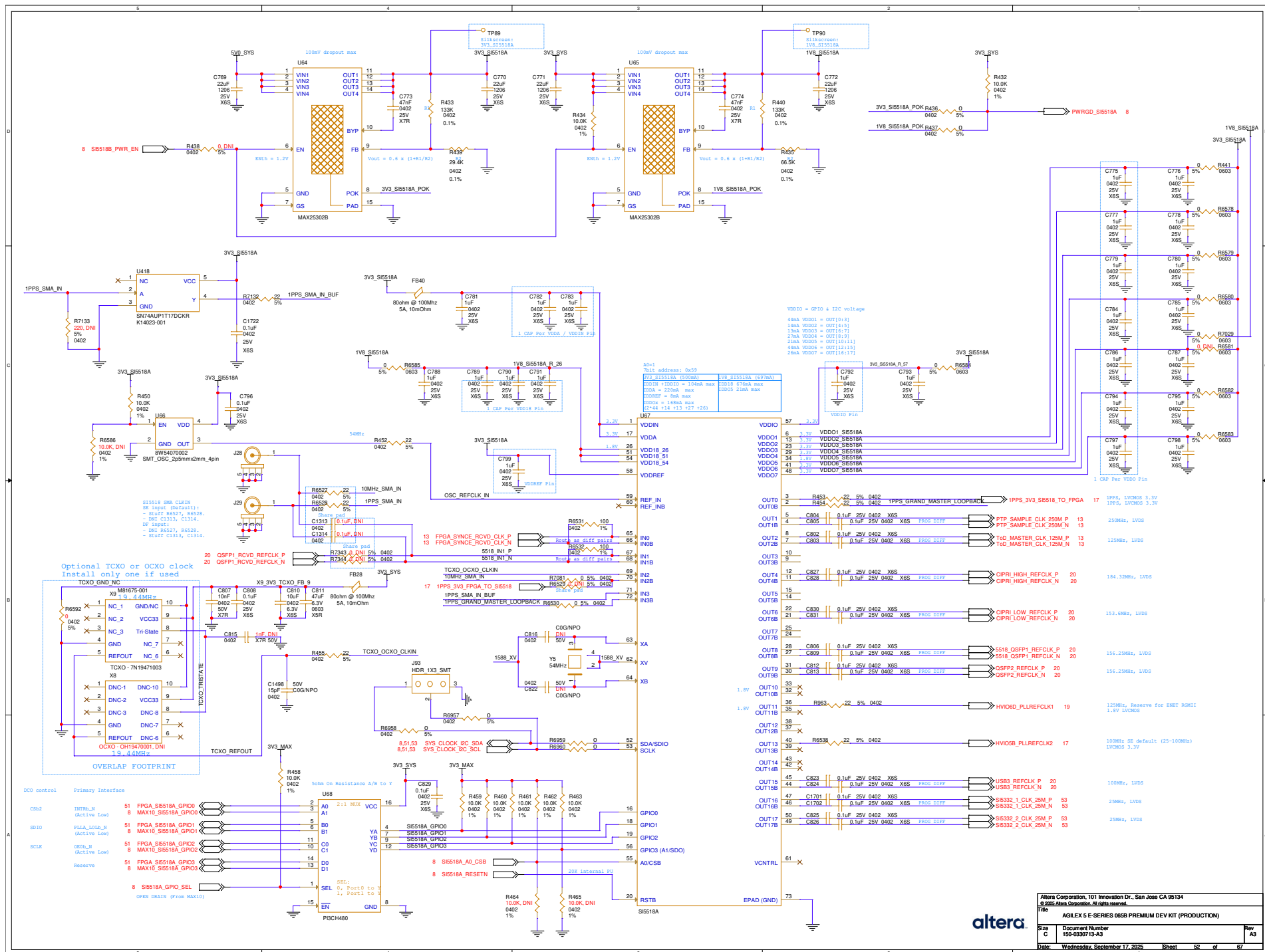




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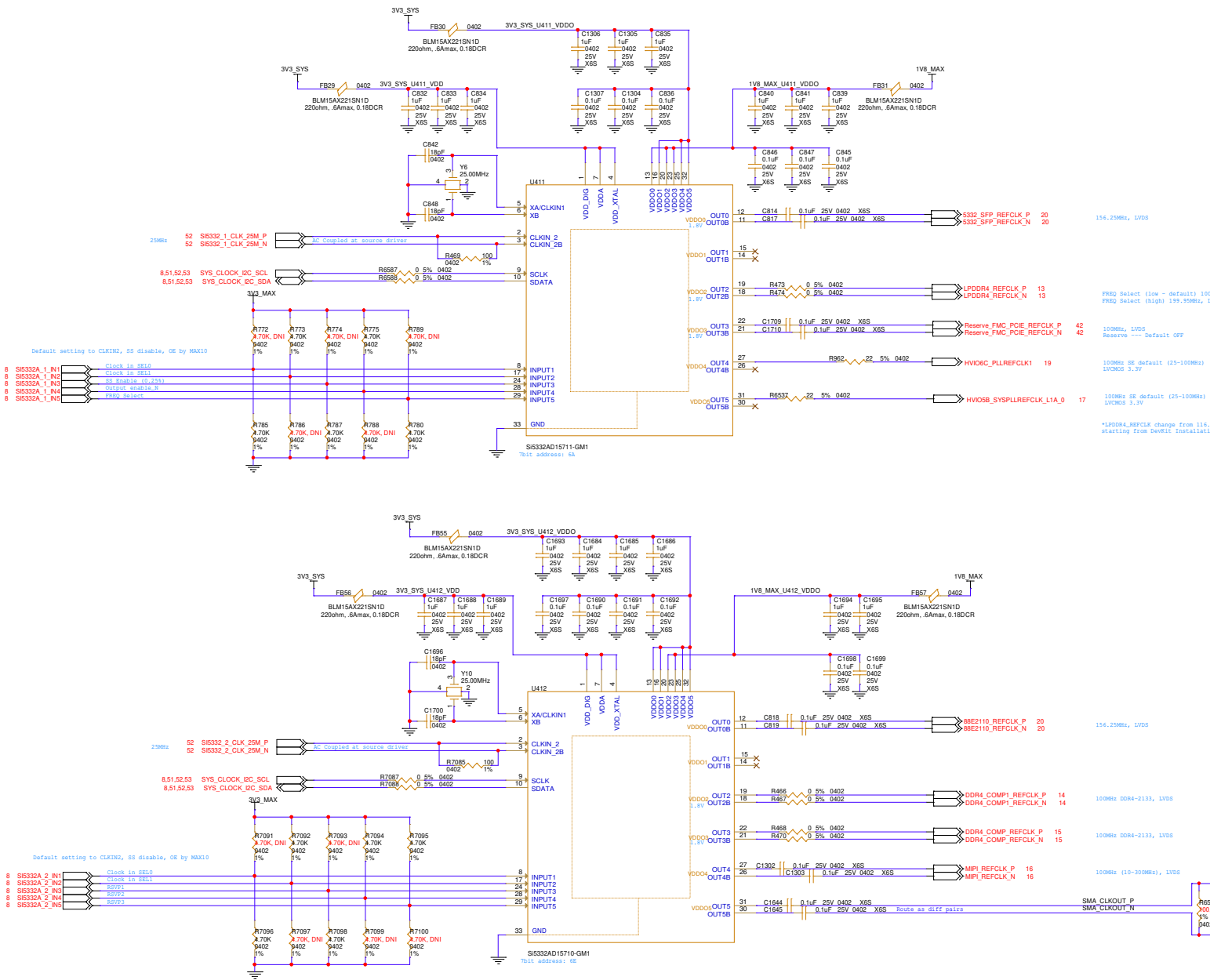
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File	AGILEX 5 E-SERIES 905B PREMIUM DEV KIT (PRODUCTION)		
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C	160-033007-15-A3	A3	
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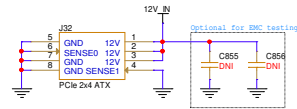


altera

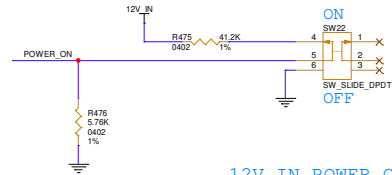
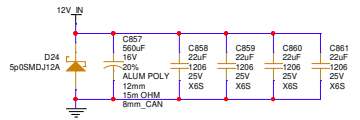
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File	AGILEX 5 E-SERIES 0505 PREMIUM DEV KIT (PRODUCTION)		
Size	Document Number 160-030071-5-A3		
C			
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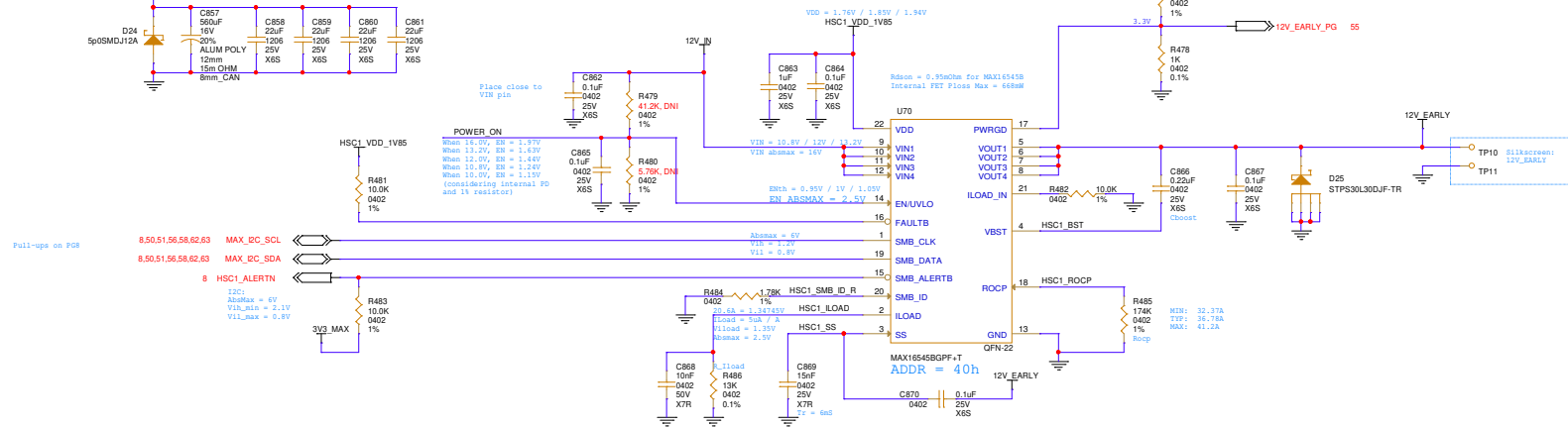
Power On Switch

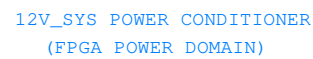


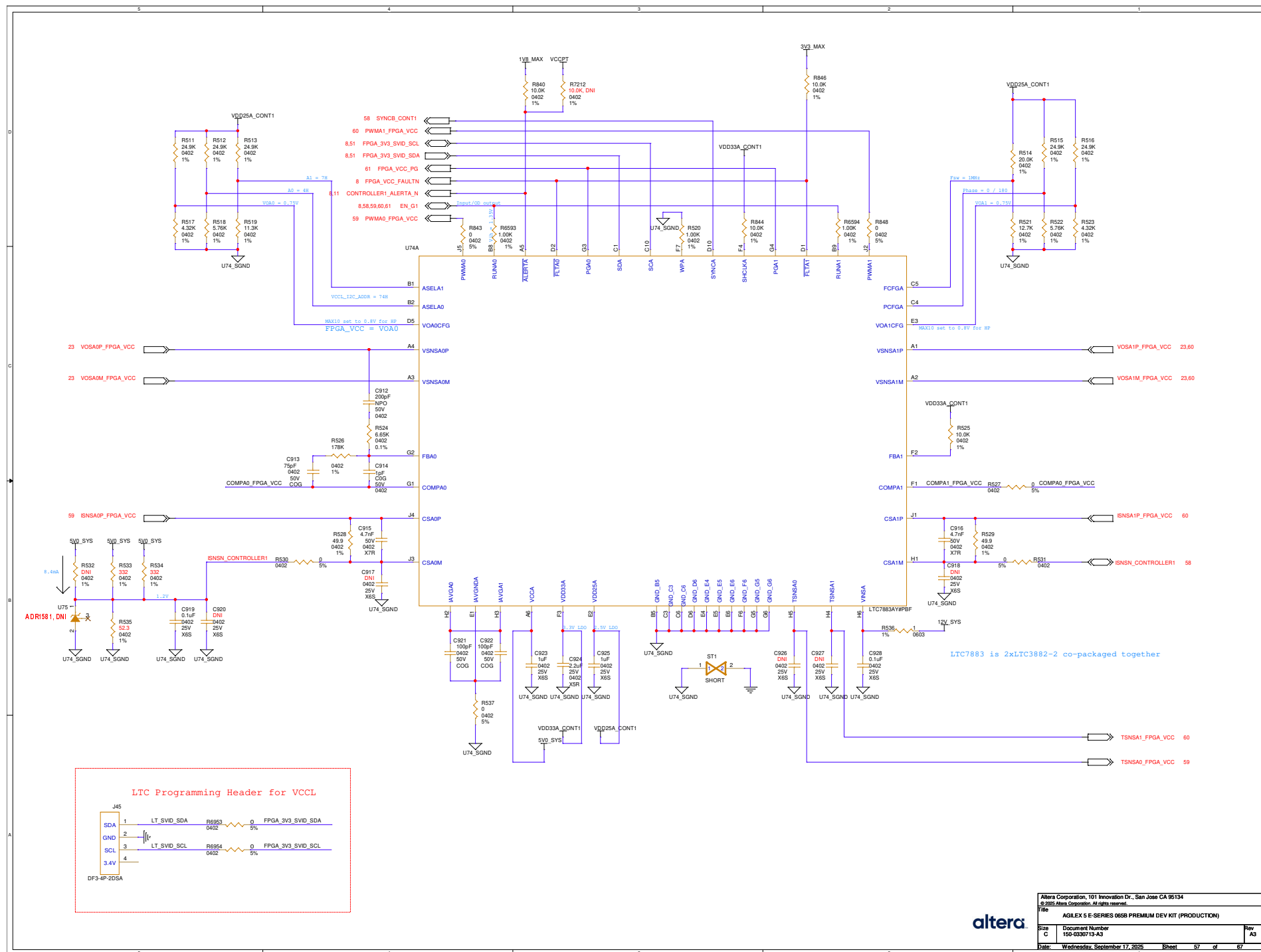
150W 2x4 ATX AUX
INPUT POWER
CONNECTOR

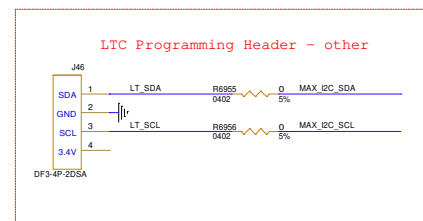


12V_IN POWER CONDITIONER
(MAX10 POWER DOMAIN)





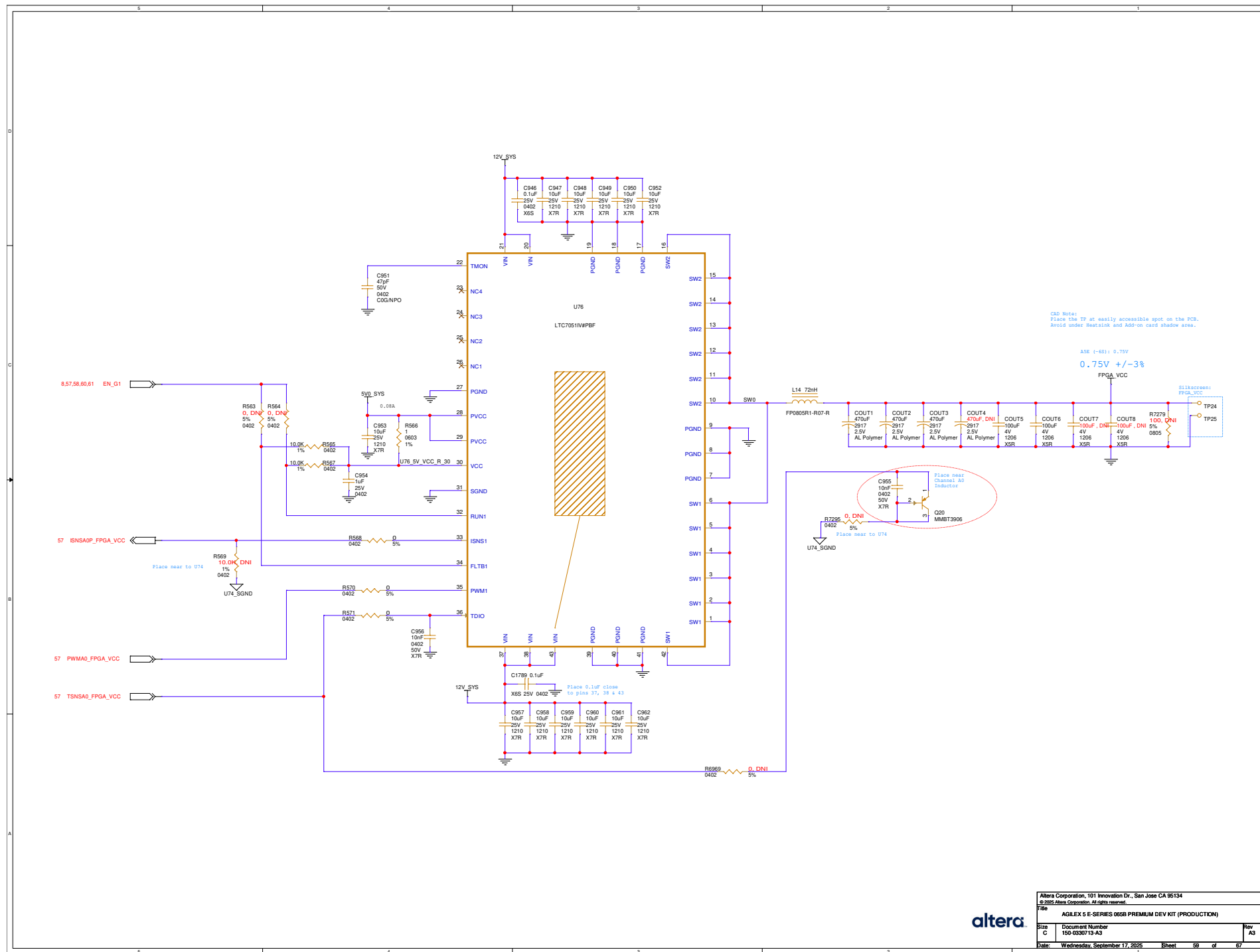




LTC7883 is 2xLTC3882-2 co-packaged together

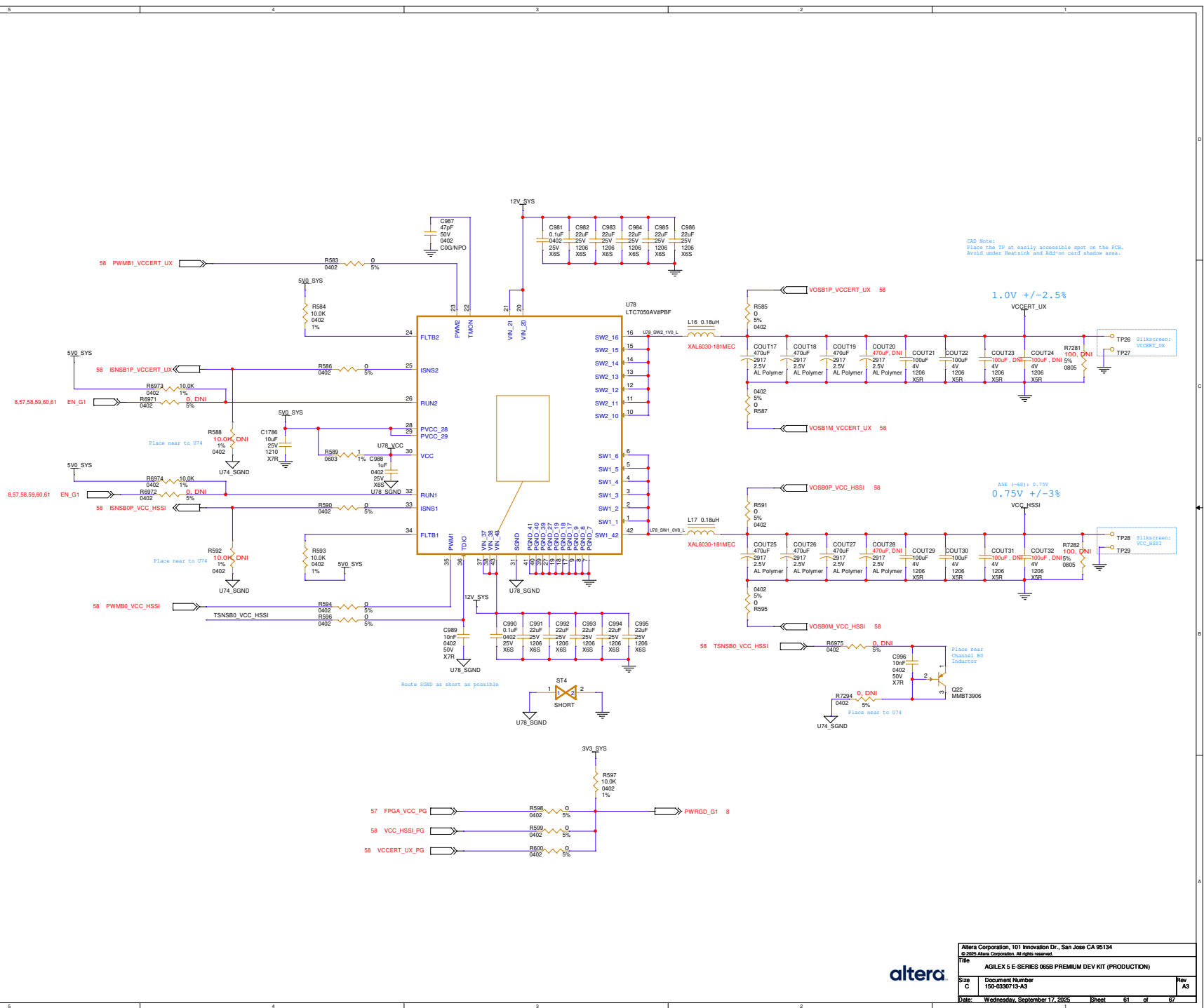
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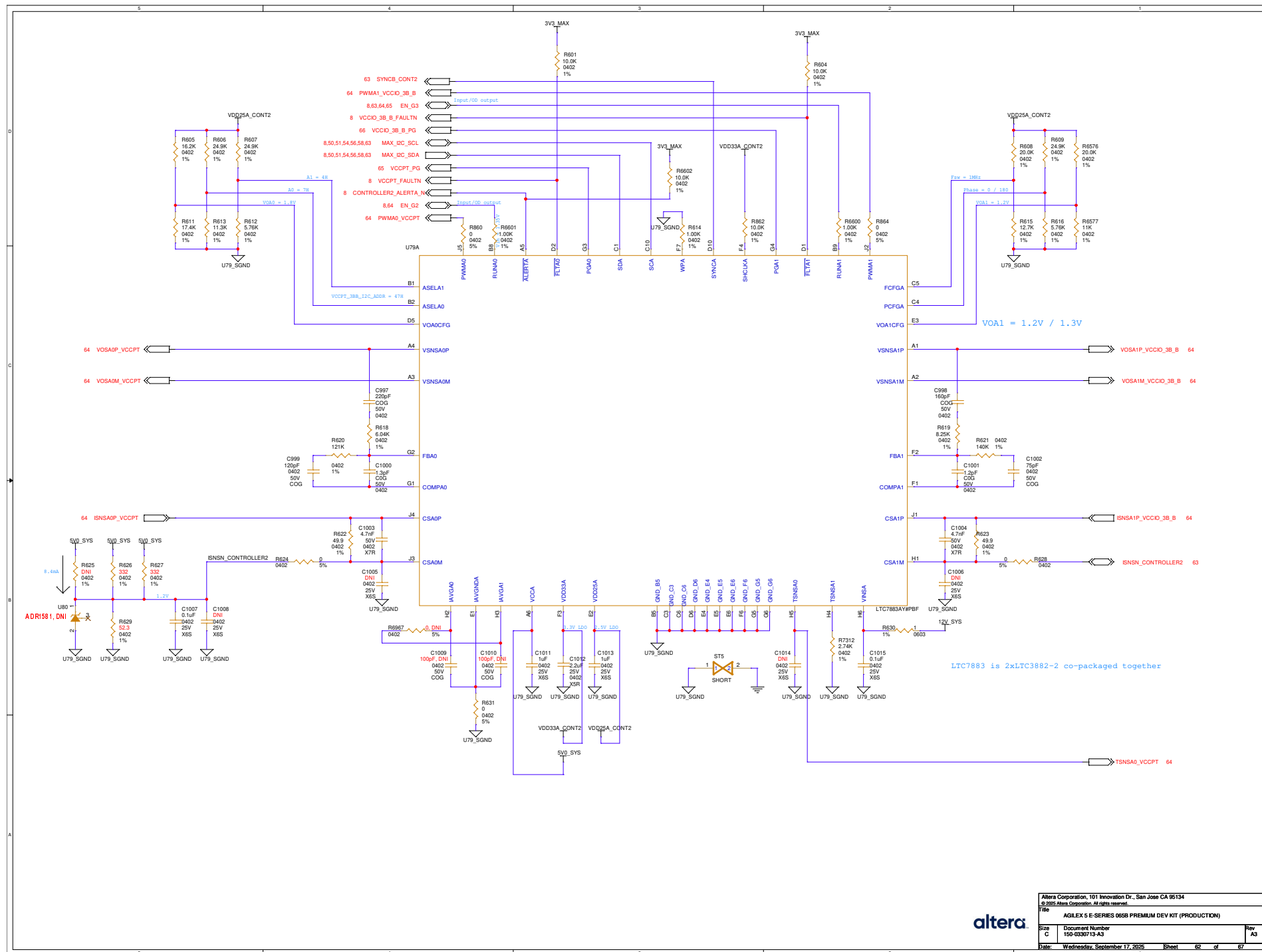
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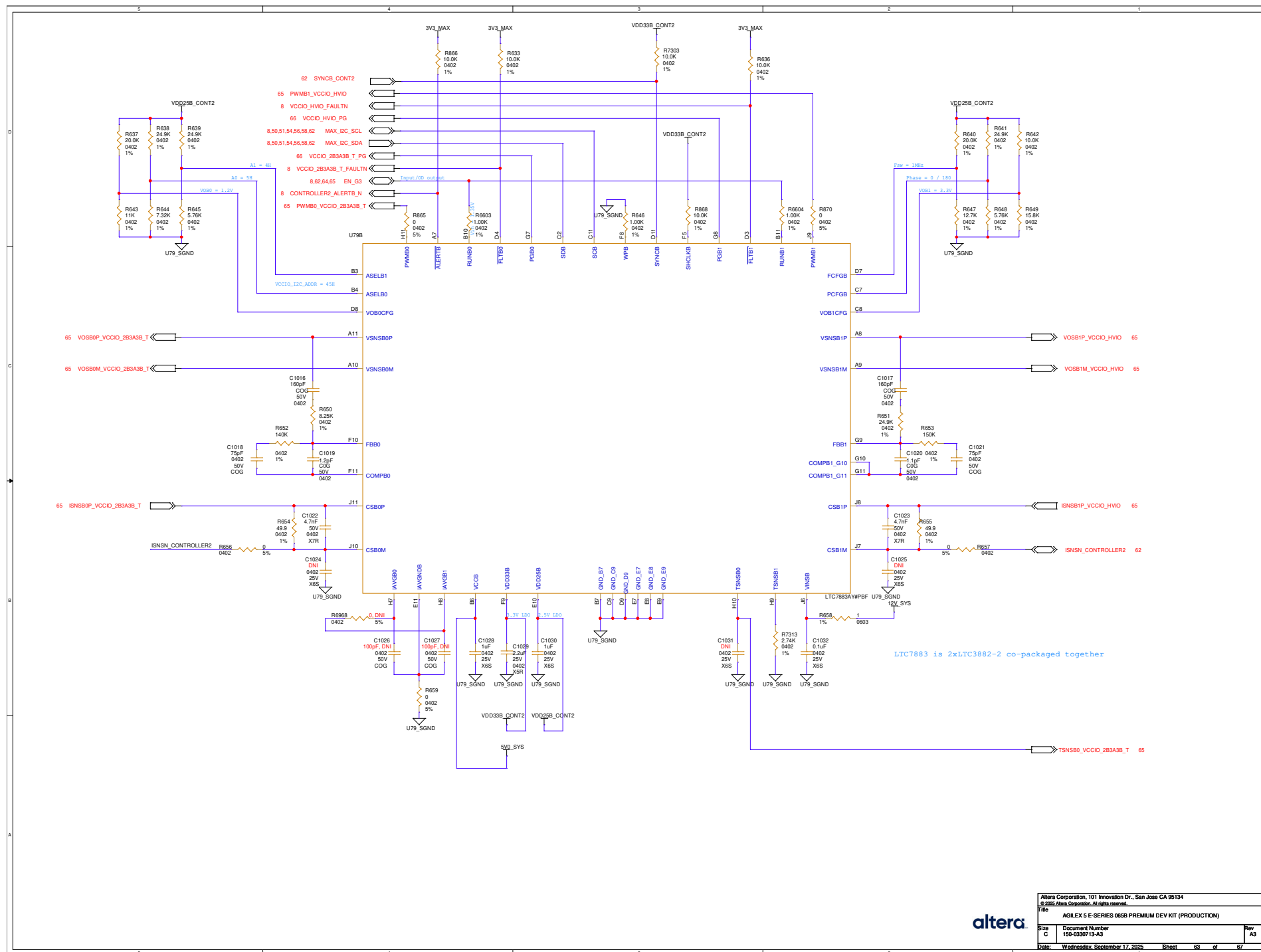


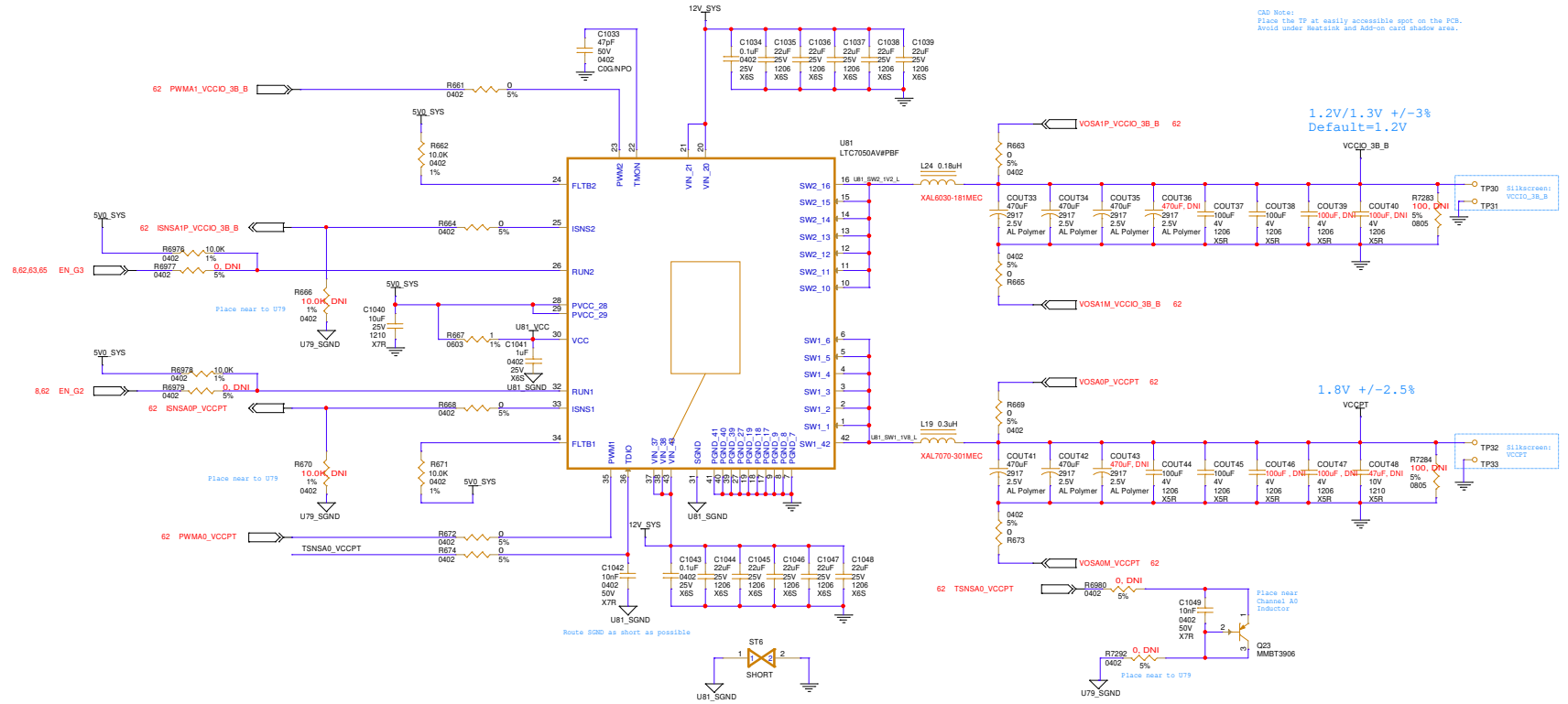
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CAO Note:
Place the TP at easily accessible spot on the PCB.
Avoid under Heatsink and Add-on card shadow area.

1.2V/1.3V +/- 3%
Default=1.2V

1.8V +/- 2.5%



